# Lecture 1: VLSI Overview

## Digital CMOS VLSI Design

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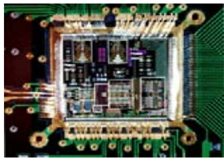
# Lecture Outline

- Historical development of computers
- Introduction to a basic digital computer
- Five classic components of a computer
- Microprocessor
- IC design abstraction level
- Processor Trend
- Developmental trends of ICs
- Moore’s Law





# Introduction to Digital Circuits

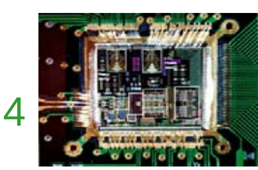
# What is a digital Computer ?

A fast electronic machine that accepts digitized input information, processes it according to a list of internally stored instruction, and produces the resulting output information.

List of instructions → Computer program

Internal storage → Memory

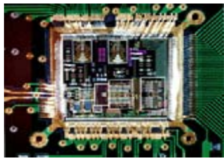




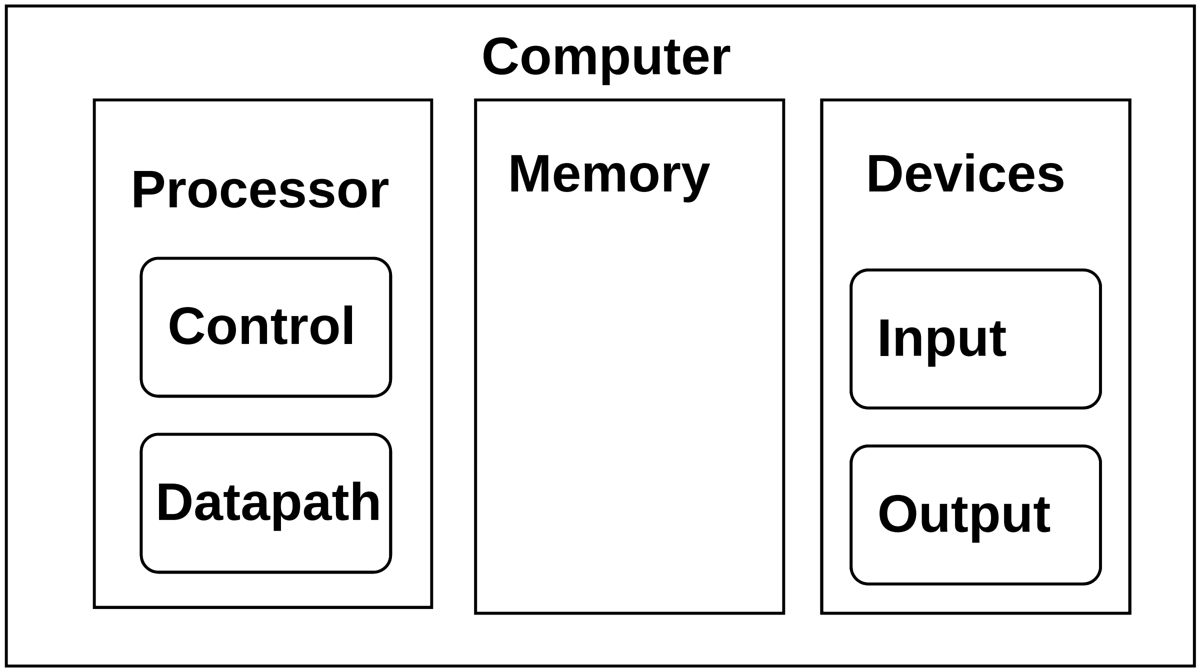
# Different Types and Forms of Computer

- Personal Computers (Desktop PCs)
- Notebook computers (Laptop computers)
- Handheld PCs
- Pocket PCs
- Workstations (SGI, HP, IBM, SUN)
- ATM (Embedded systems)
- Supercomputers





# Five classic components of a Computer




(1) Input, (2) Output, (3) Datapath, (4) Controller, and (5) Memory

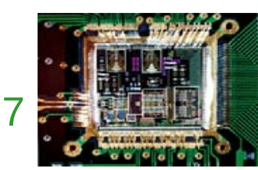
# What is a microprocessor ?

- **A microprocessor is an integrated circuit (IC) built on a tiny piece of silicon.** It contains thousands, or even millions, of transistors, which are interconnected via superfine traces of aluminum. The transistors work together to store and manipulate data so that the microprocessor can perform a wide variety of useful functions. The particular functions a microprocessor performs are dictated by software. (source : Intel)

- Simply speaking, microprocessor  is the CPU on a single chip. CPU stands for “central processing unit” also known as processor.

- Processor can be “general purpose” or “special purpose”. A special purpose processor is also known as “application specific integrated circuit” (ASIC).



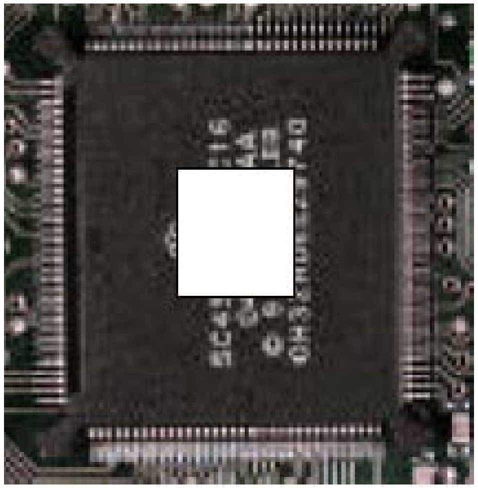


# What is an Integrated Circuit ?

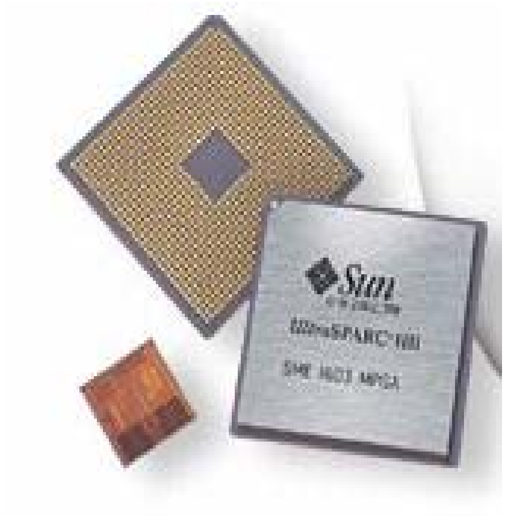
- An integrated circuits is a silicon semiconductor crystal containing the electronic components for digital gates.
- Integrated Circuit is abbreviated as IC.
- The digital gates are interconnected to implement a Boolean function in a IC .
- The crystal is mounted in a ceramic/plastic material and external connections called “pins” are made available.
- ICs are informally called chips.



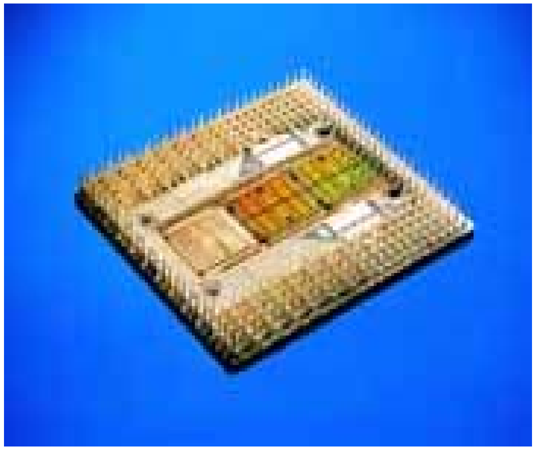
# How does a microprocessor look?



(1) ASIC




(2) Sun UltraSparc



(3) PentiumPro

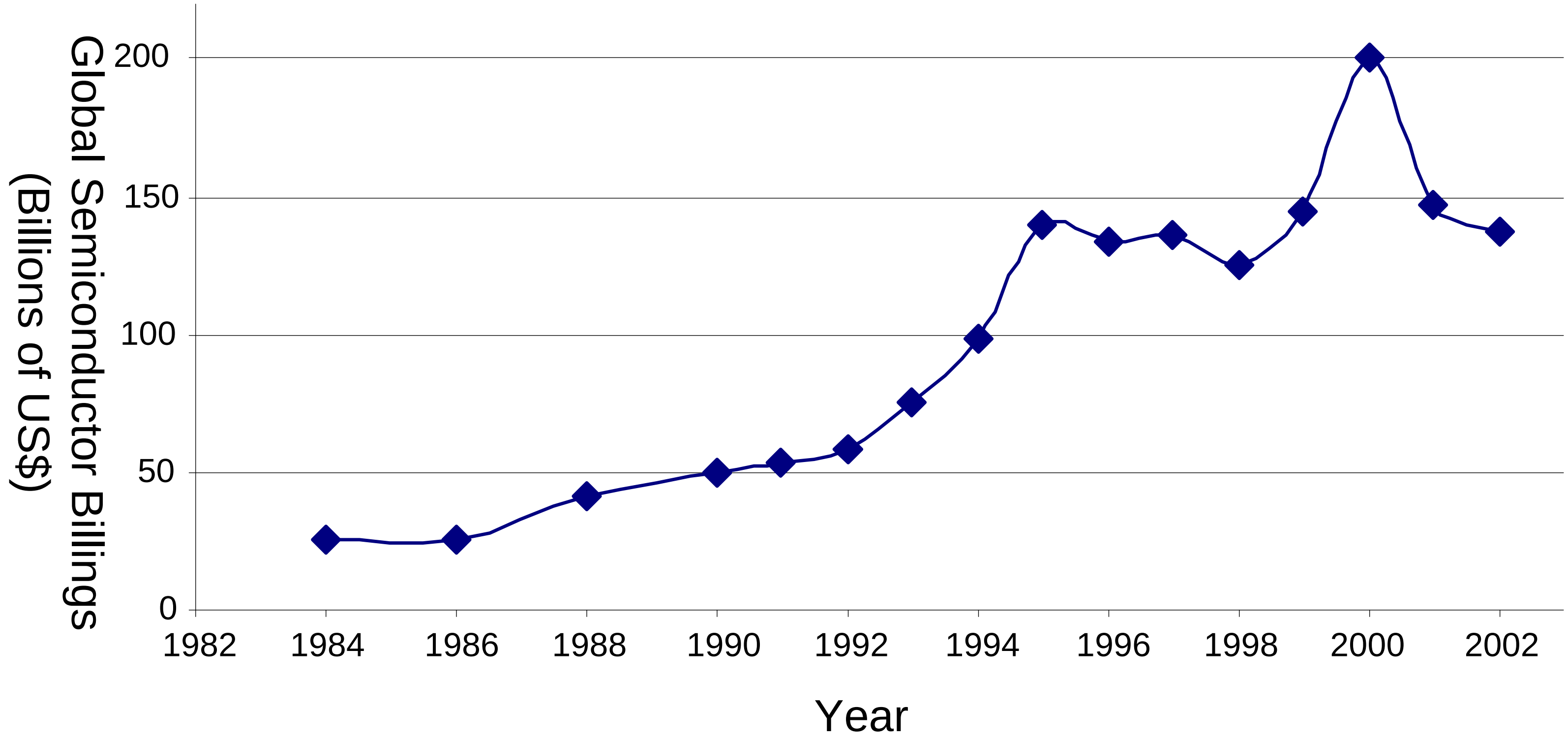
# Historical Development

# VLSI Technology: Highest Growth in History

- 1958: First integrated circuit
  - Flip-flop using two transistors
  - Built by Jack Kilby at Texas Instruments
- 2003
  - Intel Pentium 4 μprocessor (55 million transistors)
  - 512 Mbit DRAM (> 0.5 billion transistors)
- 53% compound annual growth rate over 45 years
  - No other technology has grown so fast so long
- Driven by miniaturization of transistors
  - Smaller is cheaper, faster, lower in power!
  - Revolutionary effects on society

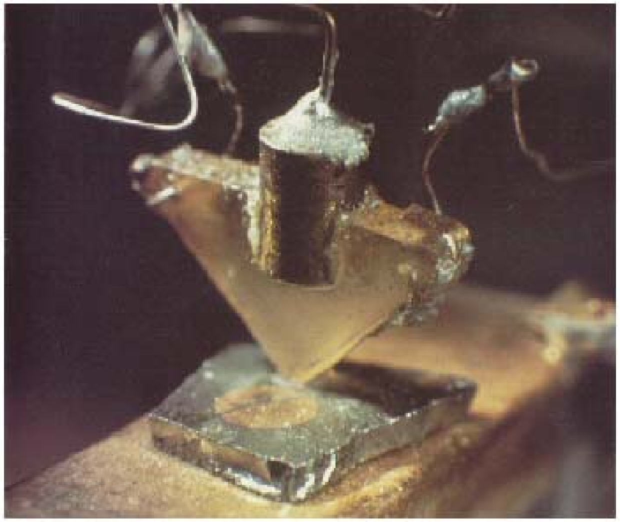
# VLSI Industry : Annual Sales

- $10^{18}$ transistors manufactured in 2003
  - 100 million for every human on the planet
- 340 Billion transistors manufactured in 2006. (World population 6.5 Billion!)



# Invention of the Transistor

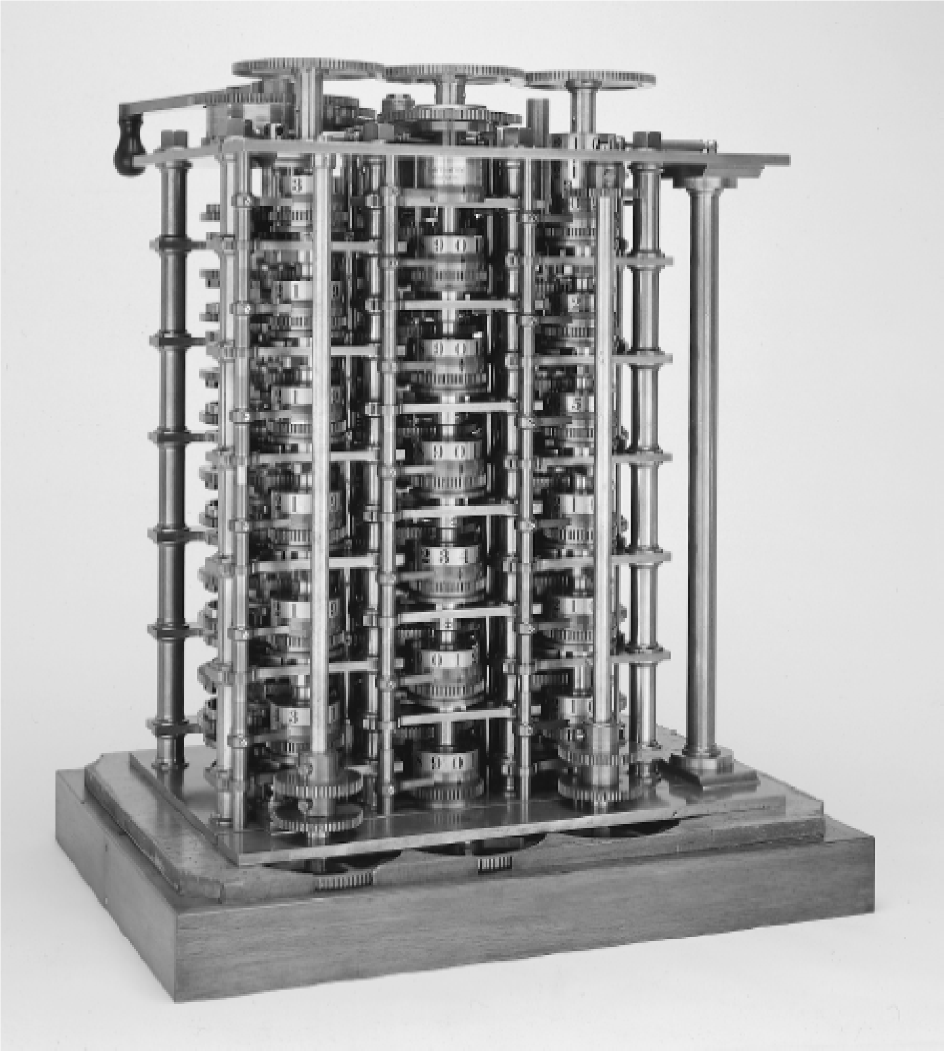
- Invention of transistor is the driving factor of growth of the VLSI technology
- Vacuum tubes ruled in first half of $20^{th}$ century Large, expensive, power-hungry, unreliable
- 1947: first point contact transistor
  - John Bardeen and Walter Brattain at Bell Labs
  - Earned Nobel prize in 1956



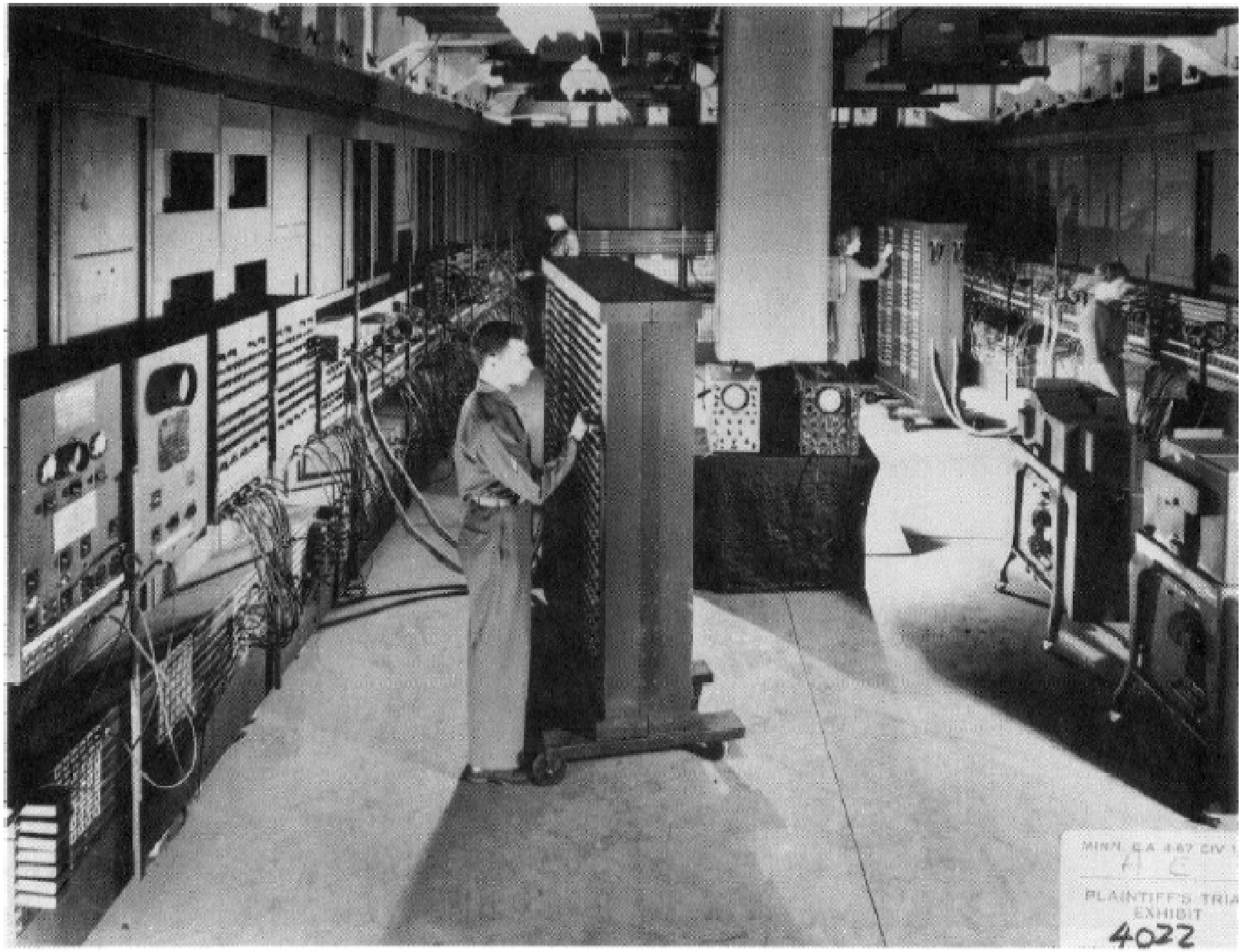
# Transistor Types

- Bipolar transistors
  - n-p-n or p-n-p silicon structure
  - Small current into very thin base layer controls large currents between emitter and collector
  - Base currents limit integration density
- Metal Oxide Semiconductor Field Effect Transistors (MOSFET)
  - nMOS and pMOS MOSFETS
  - Voltage applied to insulated gate controls current between source and drain
  - Low power allows very high integration

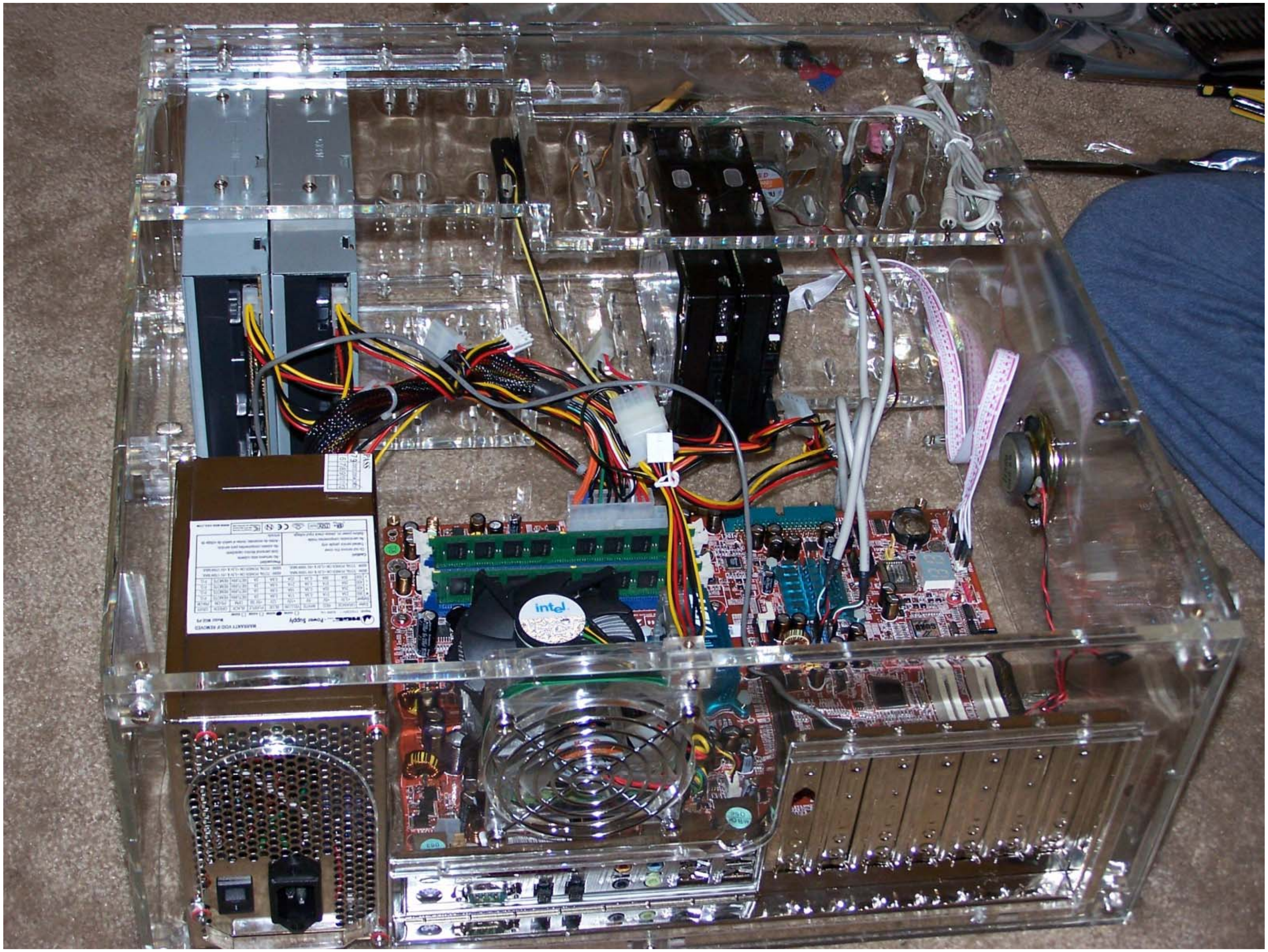
# The Babbage Difference Machine in 1832



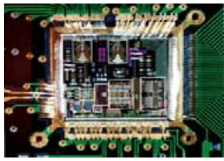
# The First Electronic Computer in 1946 (ENIAC)



# How a Home PC Looks Today??

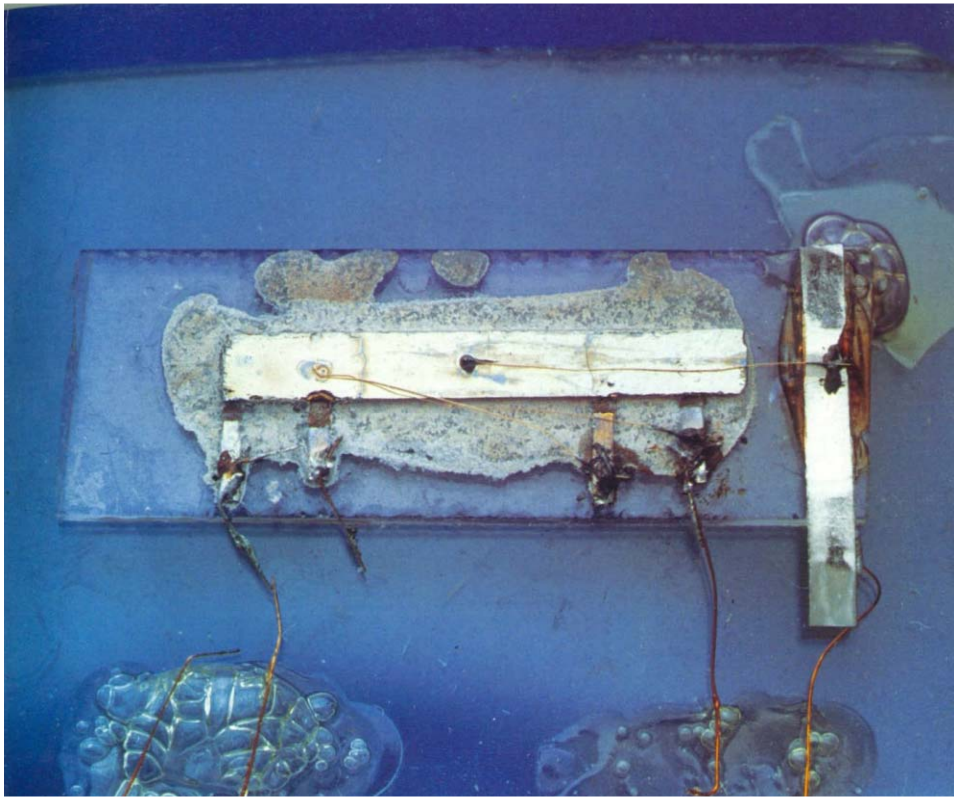




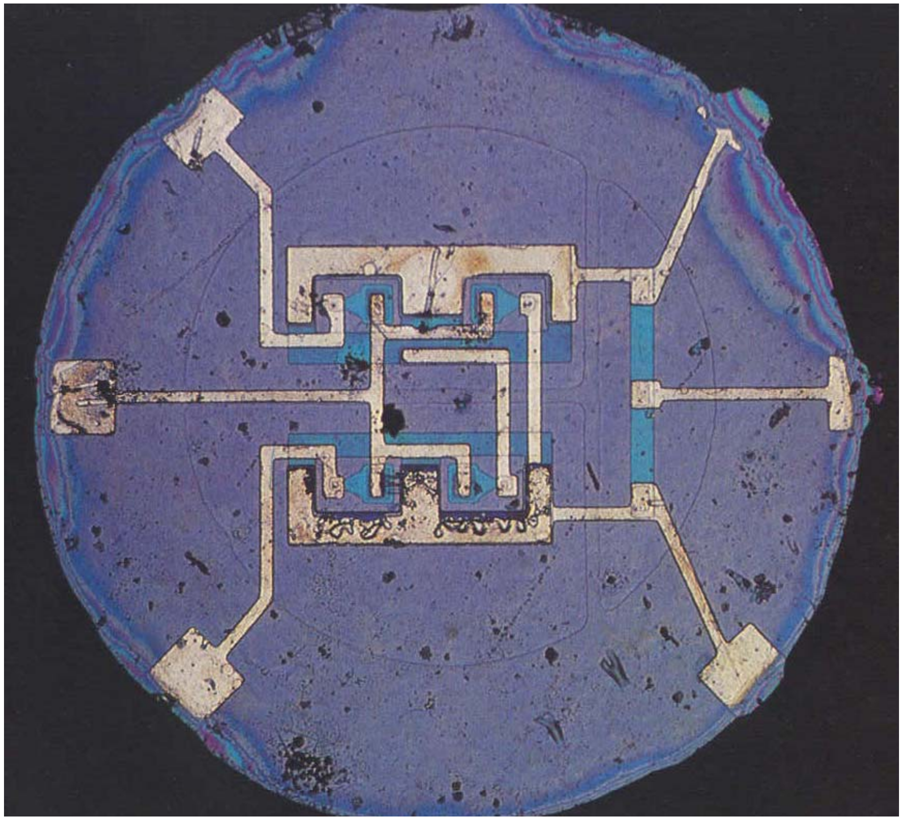
# First Integrated Circuit - 1958

- The First Integrated Circuit – Jack Kilby, Texas Instruments
- 1 Transistor and 4 Other Devices on 1 Chip
- Winner of the 2000 Nobel Prize

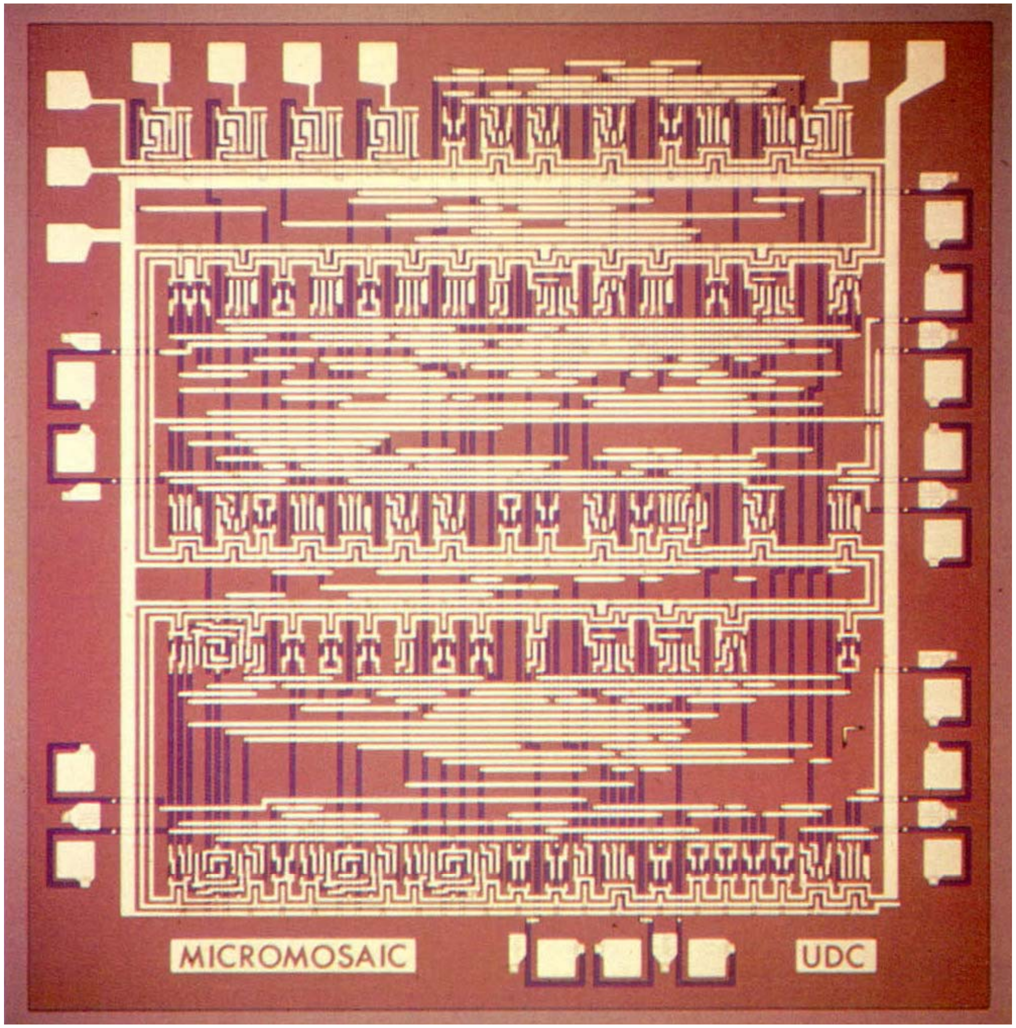


# First Commercial Planar IC - 1960

- Fairchild -- One Binary Digital (Bit) Memory Device on a Chip
- 4 Transistors and 5 Resistors
- Start of Small Scale Integration (SSI)!! We are in VLSI!!

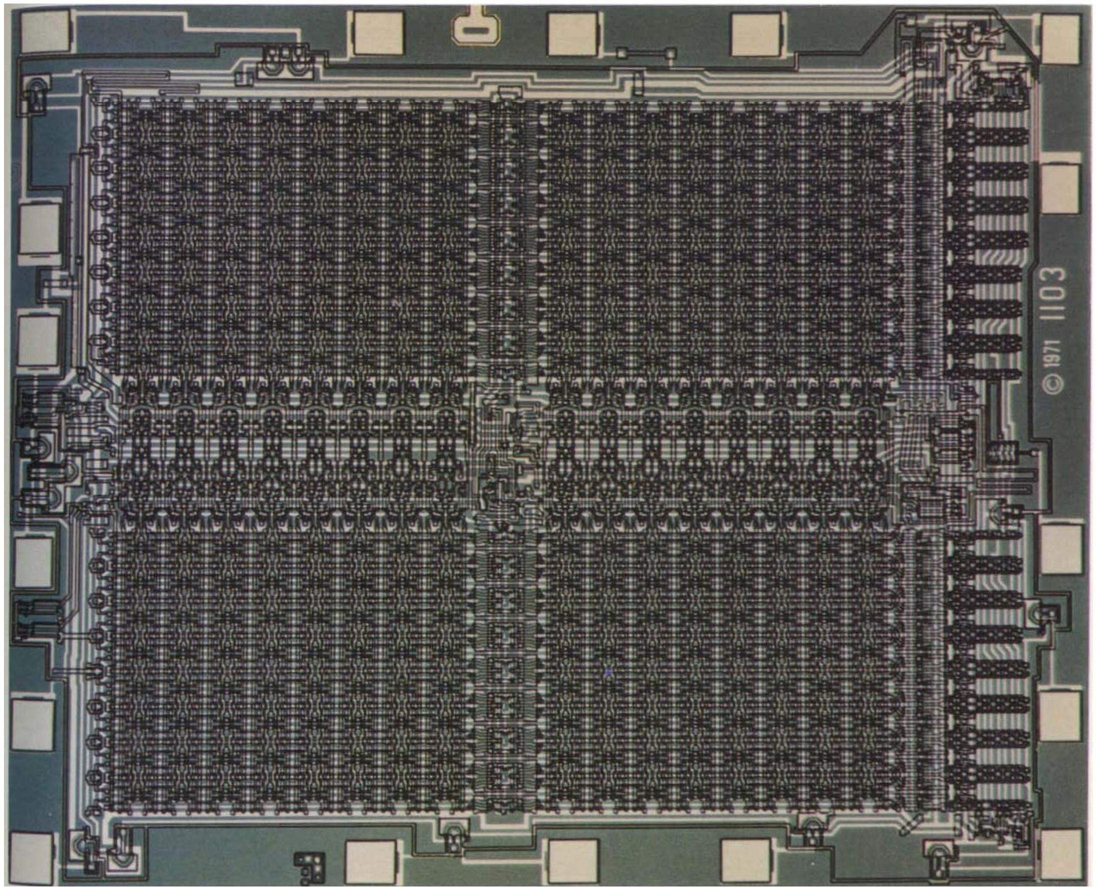


# First IC Created with Computer-Aided Design Tools -- 1967




μMOSAIC – Fairchild

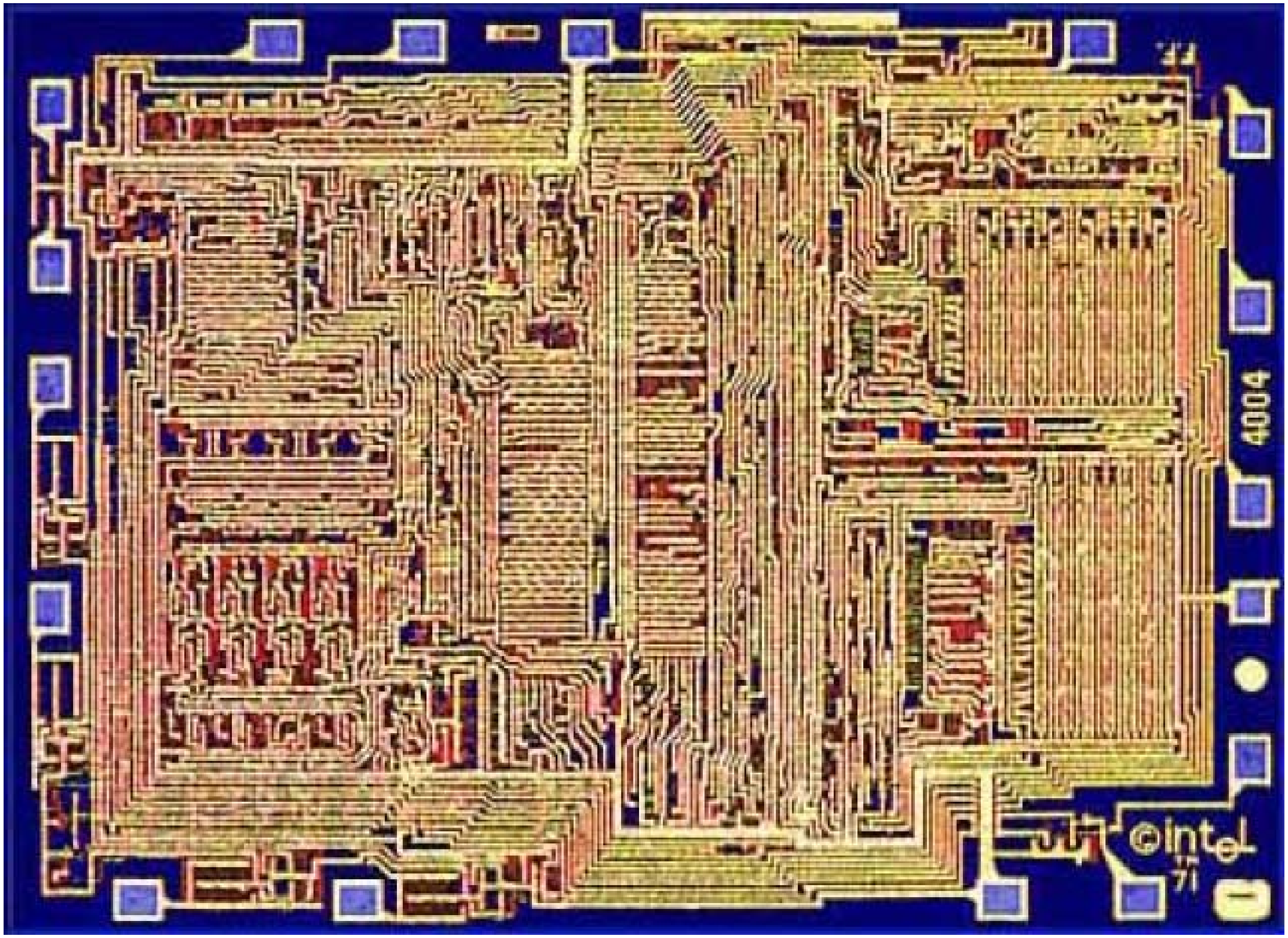
# First 1,024 Bit Memory Chip -- 1970



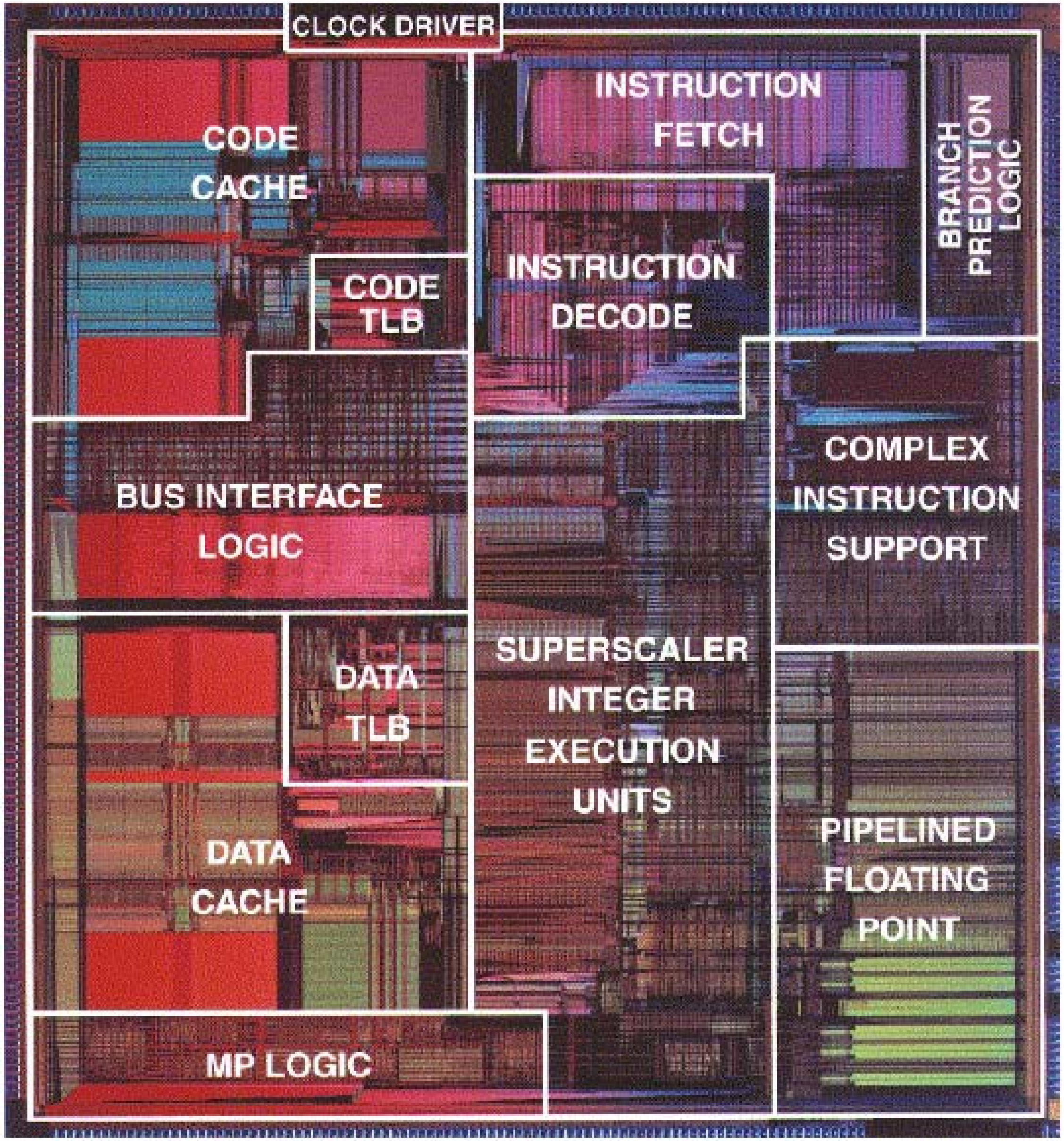

Intel Corporation DRAM

- 1970's processes usually had only nMOS transistors
  - *Inexpensive, but consume power while idle.*
- 1980s-present: CMOS processes for low idle power

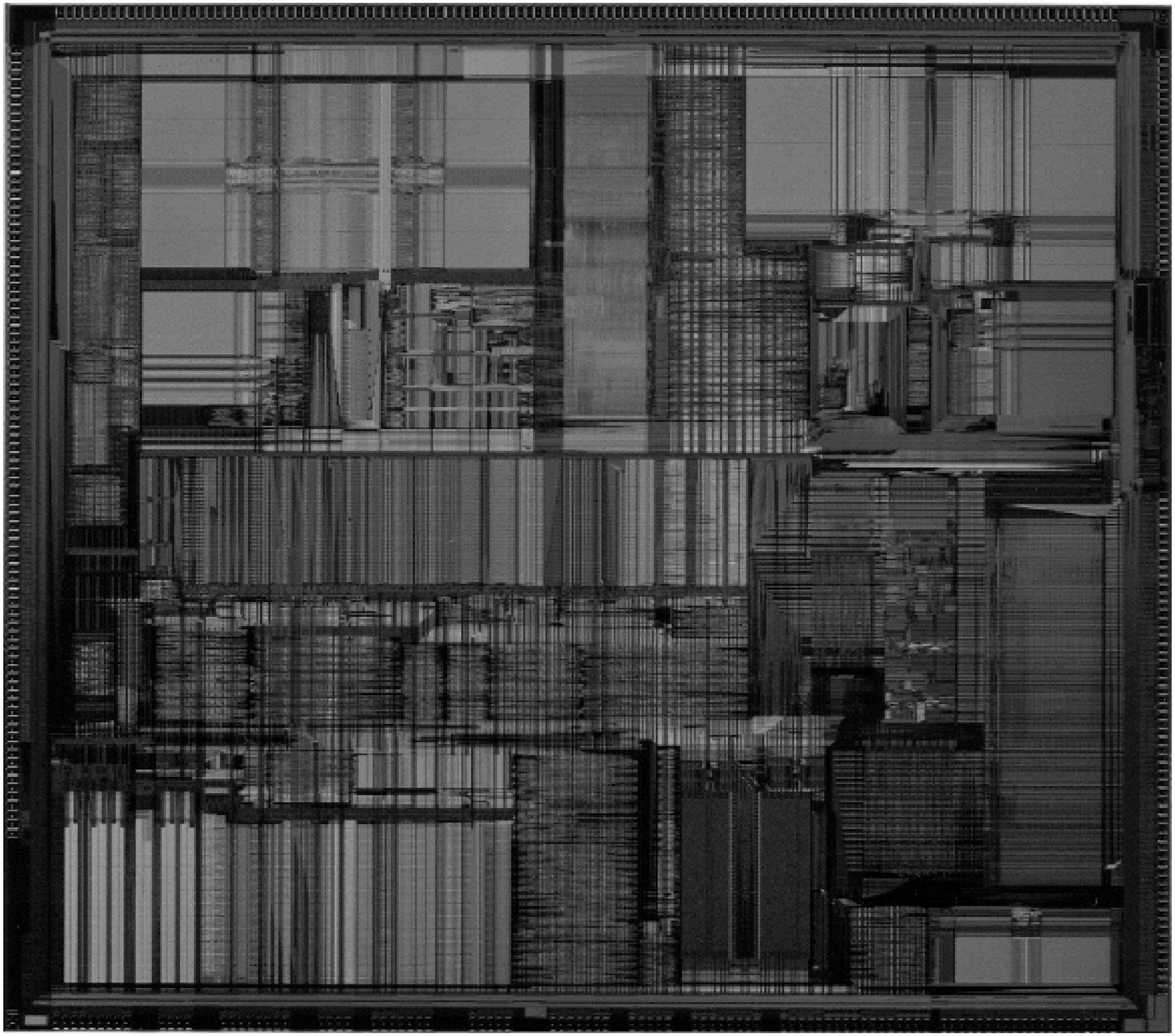
# Intel 4004 : 2.3K Transistors (1971)



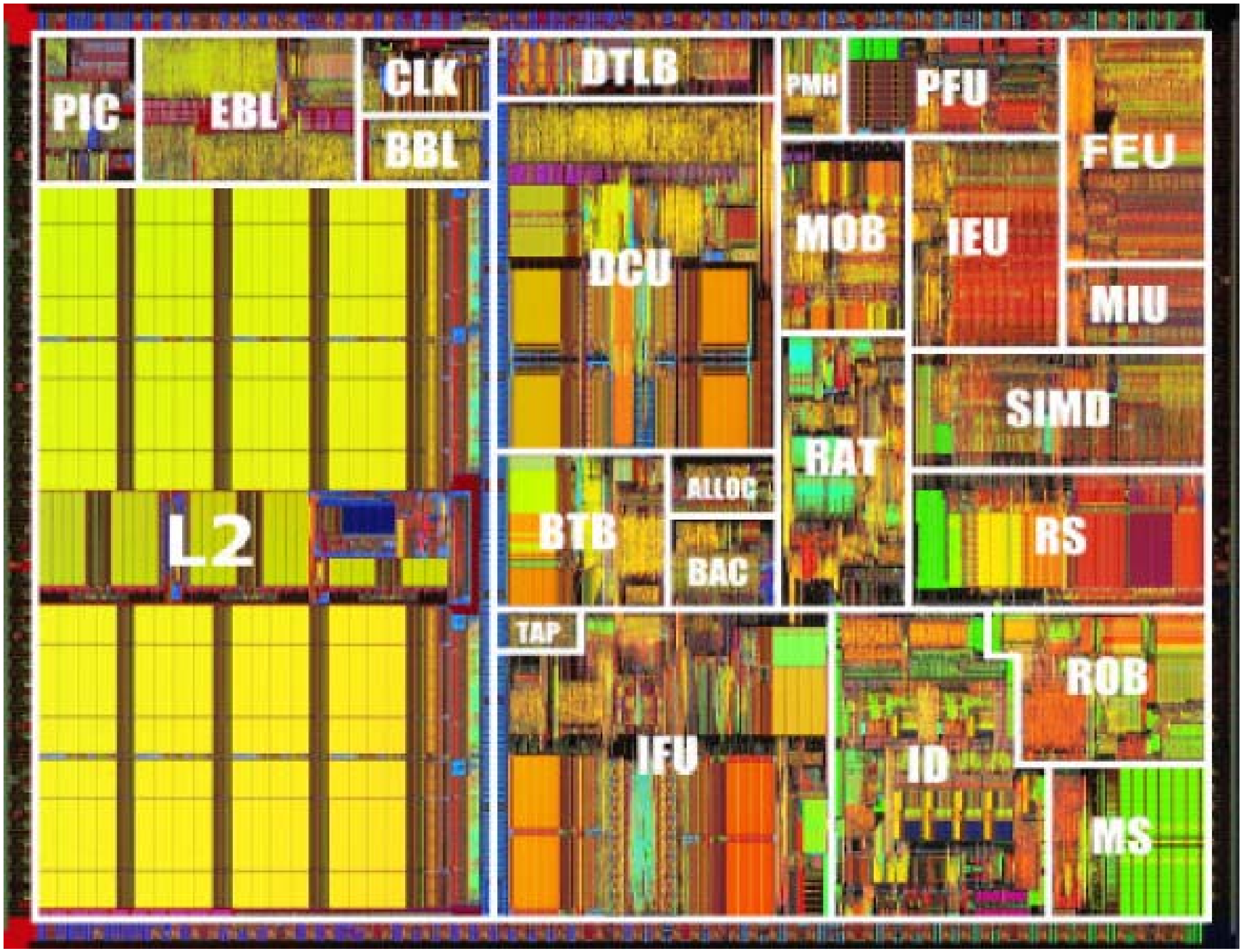
# Pentium : 3.1M Transistors (1993)



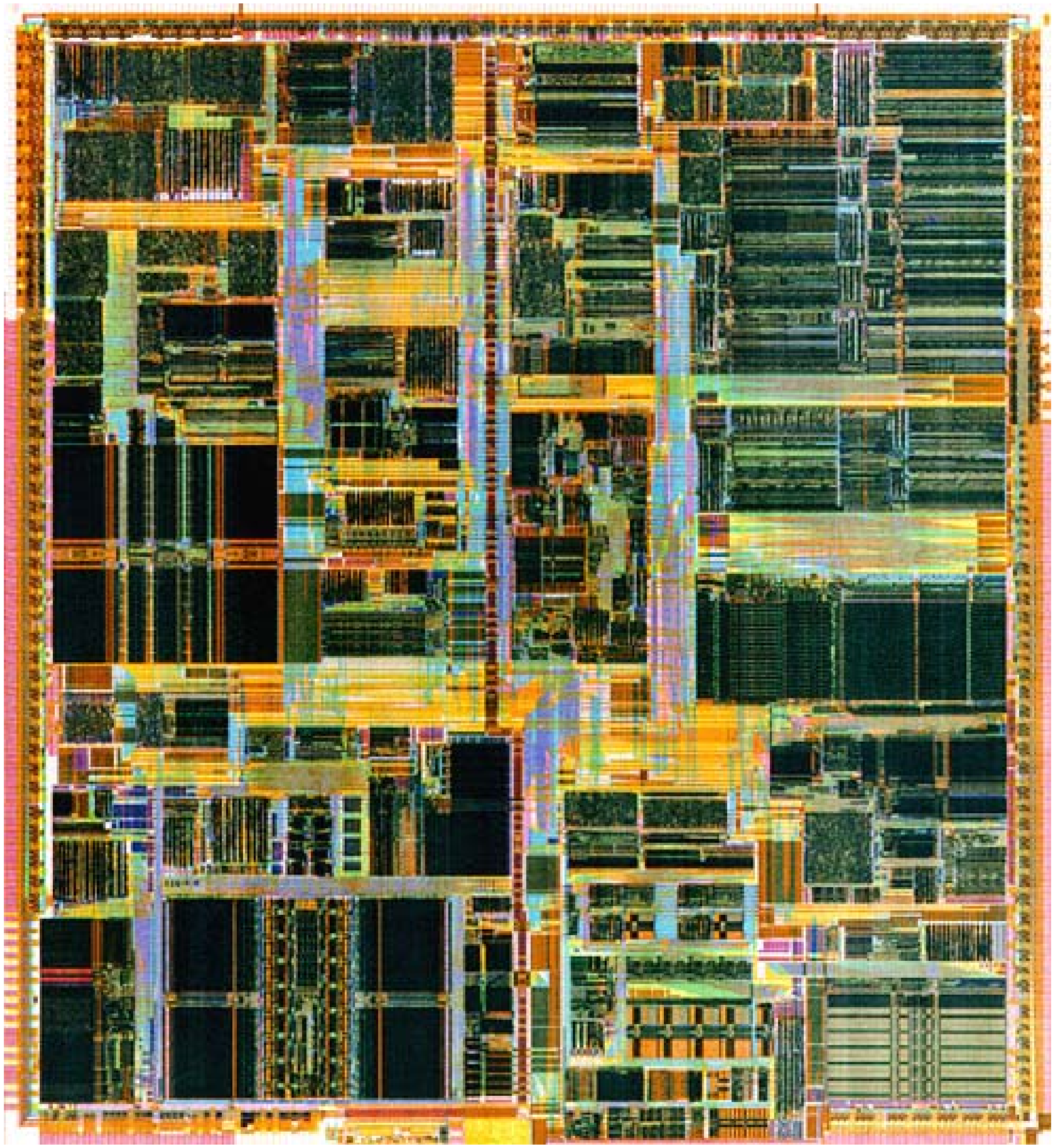
# Pentium II : 7.5M Transistors (1997)



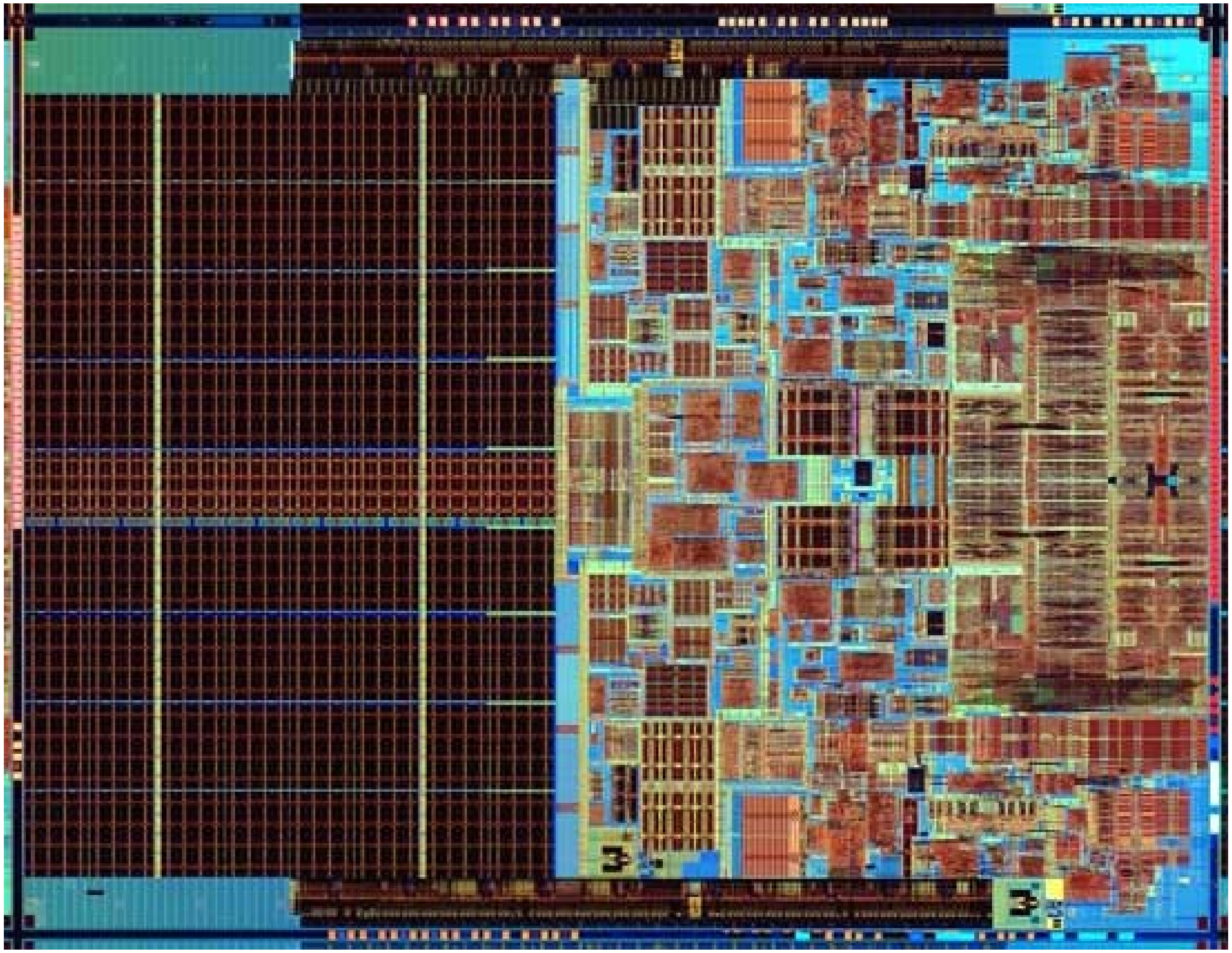
# Pentium III : 28.1M Transistors (1999)



# Pentium IV : 52M Transistors (2001)

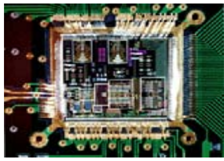


# Core 2 Duo: 291M Transistors (2006)



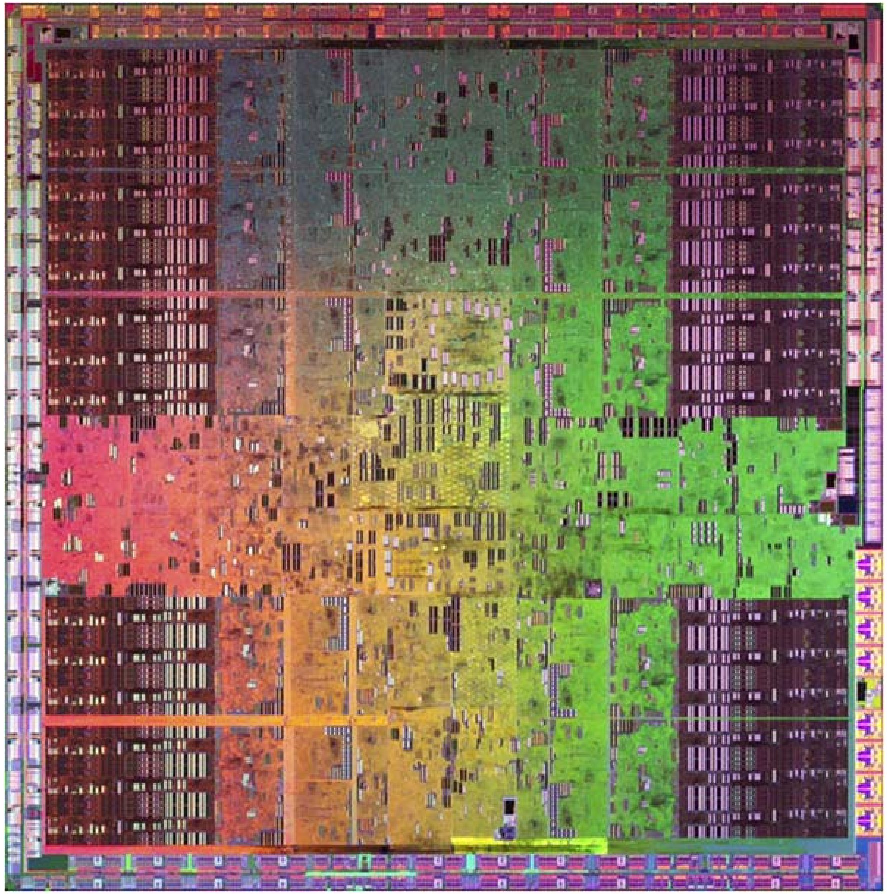
Core 2 Duo T5000/T7000 series mobile processors, called Penryn uses 800M of 45 nanometer devices (2007).



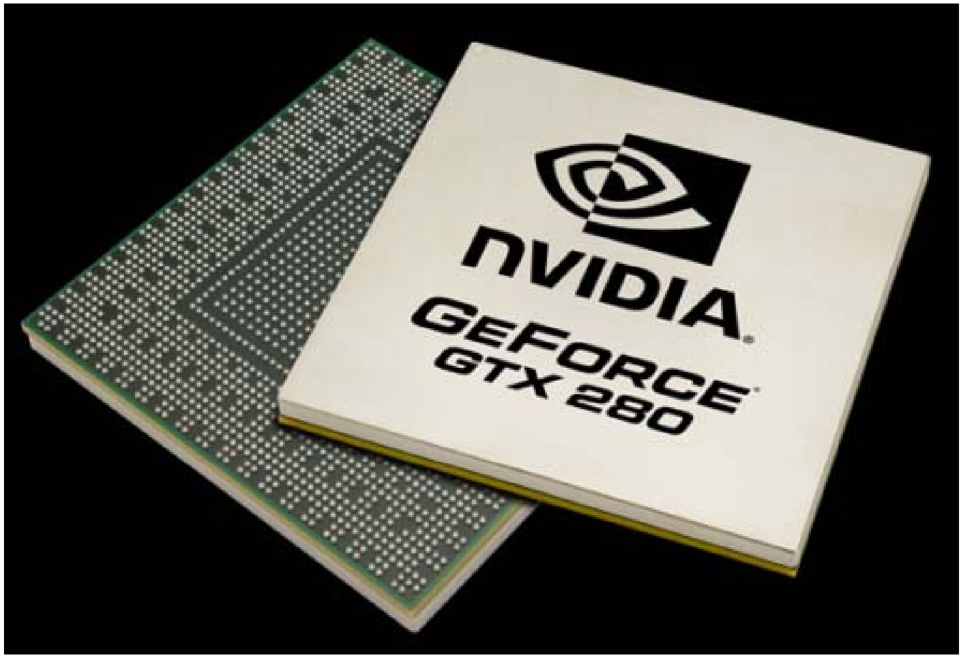


# Nvidia GT200 Graphics Processing Unit

- This GPU contains 1.4 billion transistors.
- This uses a 65 nm CMOS fabrication process.

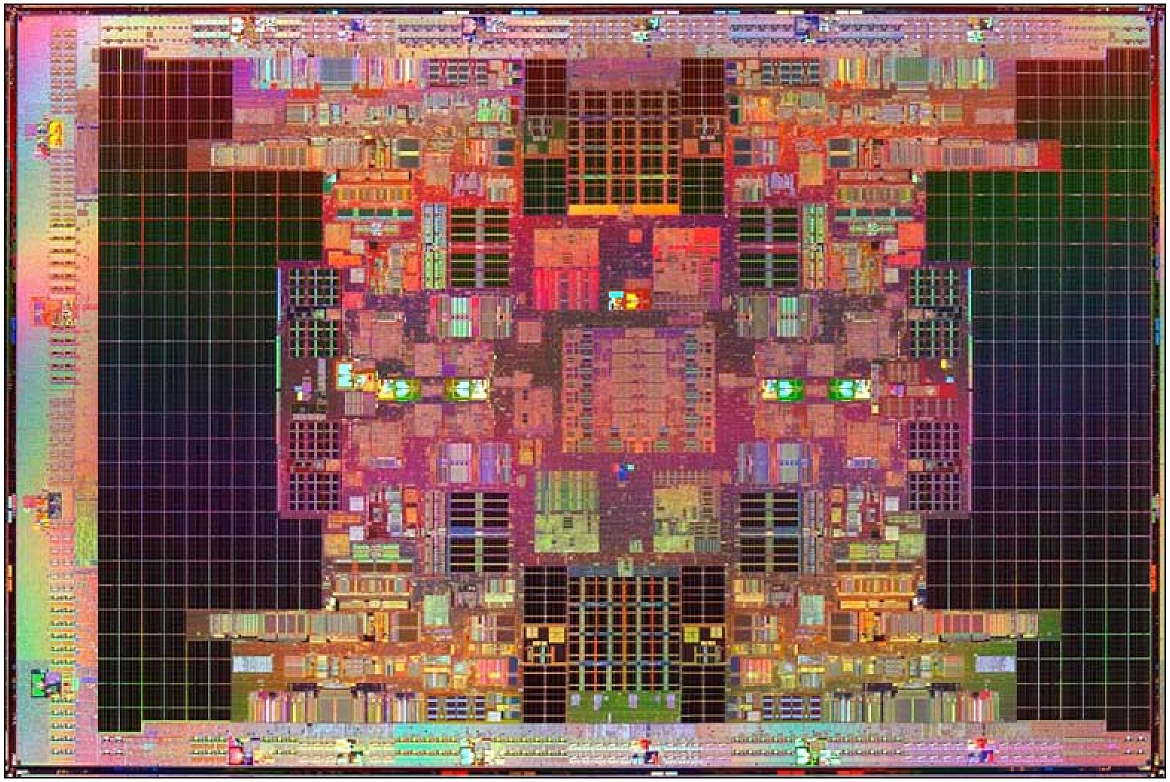


Source: http://www.gdiamos.net



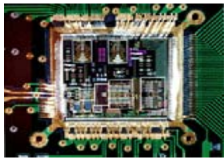

Source:
http://nvidiathepoweroffuture.files.wordpress.com/

# Intel's Tukwila – 2B Transistors



- Quad core i.e. 4 cores per die.
- 30 MB of cache.
- 2 billion transistors on the die.
- 64-bit Itanium family.
- 65nm CMOS technology.
- Release in early 2010.





# Circuit Design Flow

# Integrated Circuits Categories

There are many different types of ICs as listed below.

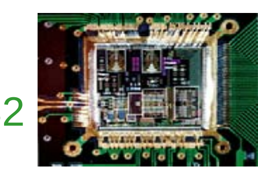
| IC Categories | Functions |
|---|---|
| Analog ICs | Amplifiers |
| | Filters |
| Digital ICs | Boolean Gates |
| | Encoders/Decoders |
| | Multiplexers / Demultiplexers |
| | Flip-flops |
| | Counters |
| | Shift Registers |
| Hybrid ICs | Mixed Signal Processors |
| Interface ICs | Analog-Digital Converters |
| | Digital-Analog Converters |



# Levels of Integration (Chip Complexity)

Categorized by the number of gates contained in the chip.

| IC Complexity | Number of Gates | Functional Complexity | Examples |
|---|---|---|---|
| SSI | <10 | Basic gates | Inverters, AND gates, OR gates, NAND gates, NOR gates |
| | | | |
| MSI | 10-100 | Basic gates | Exclusive OR/NOR |
| | | Sub-modules | Adders, subtractors, encoders, decoders, multiplexers, demultiplexers, counters, flip-flops |
| LSI | 100-1000s | Functional modules | Shift registers, stacks |
| VLSI | 1000s-100,000 | Major building blocks | Microprocessors, memories |
| ULSI | >100,000 | Complete systems | Single chip computers, digital signal processors |
| WSI | >10,000,000 | Distributed systems | Microprocessor systems |

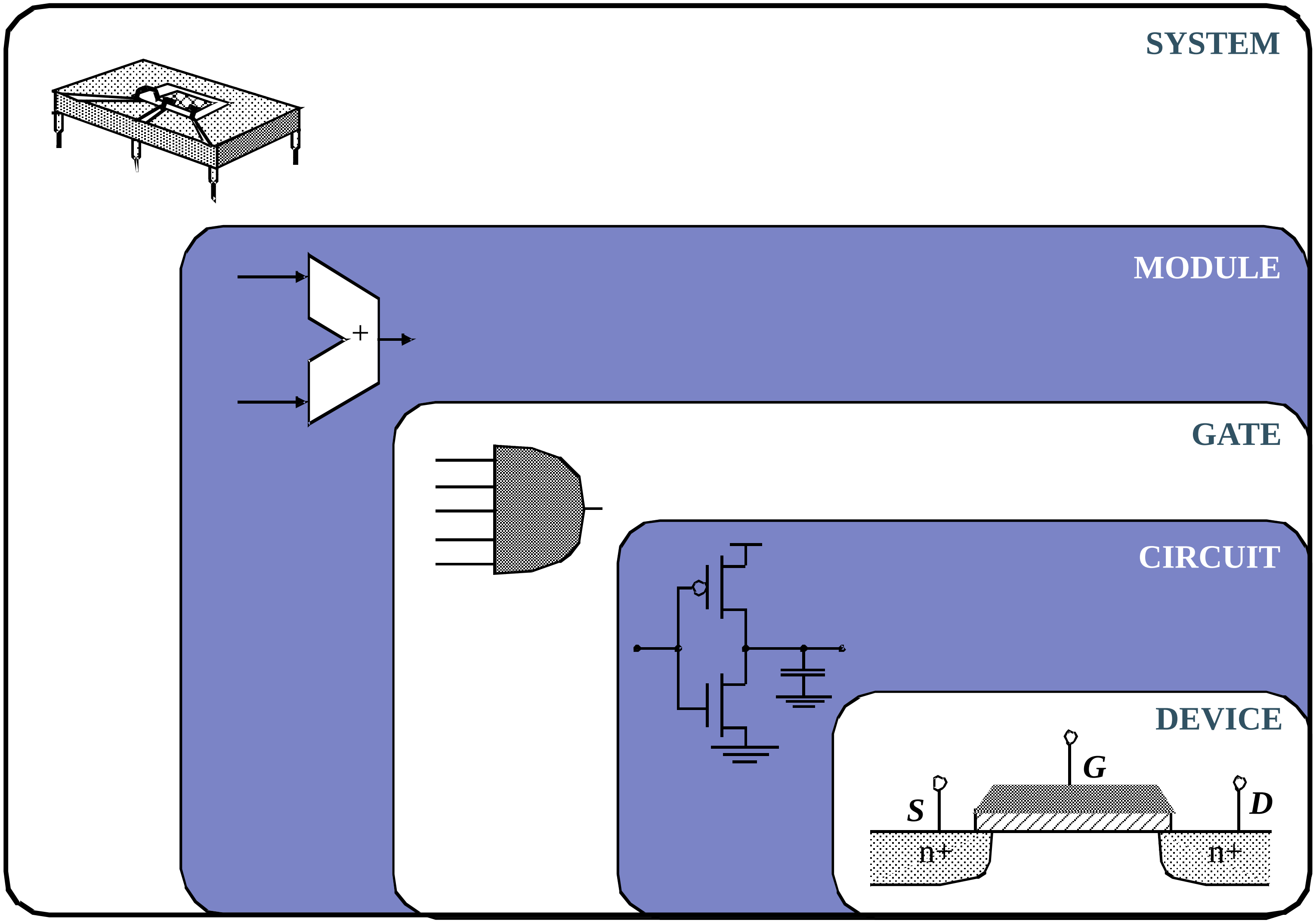


# Digital Logic Families

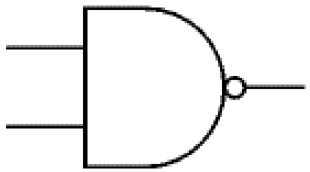
- Various circuit technology used to implement an IC at lower level of abstraction.
- The circuit technology is referred to as a digital logic family.

| | |
|---|---|
| RTL - Resistor-transistor Logic | obsolete |
| DTL - Diode-transistor logic | obsolete |
| TTL - Transistor-transistor logic | not much used |
| ECL - Emitter-coupled logic | high-speed ICs |
| MOS - Metal-oxide semiconductor | high-component density |
| CMOS - Complementary Metal-oxide semiconductor | widely used, low-power high-performance and high-packing density IC |
| BiCMOS - Bipolar Complementary Metal-oxide semiconductor | high current and high-speed |
| GaAs - Gallium-Arsenide | very high speed circuits |

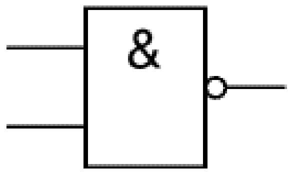
# Design Abstraction Levels



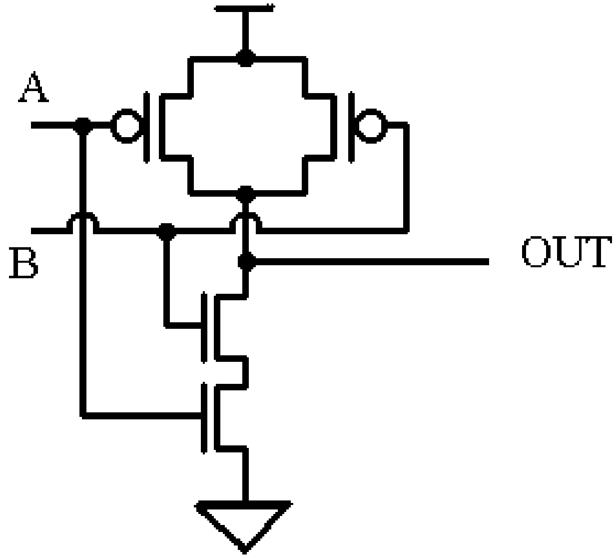
# Digital Circuits : Logic to Device



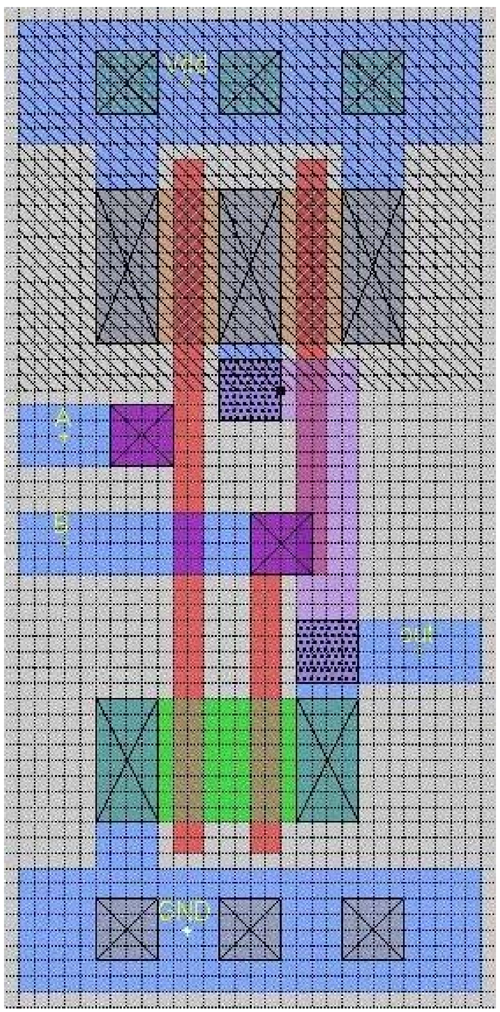
(NAND Gate)




(IEC Symbol)

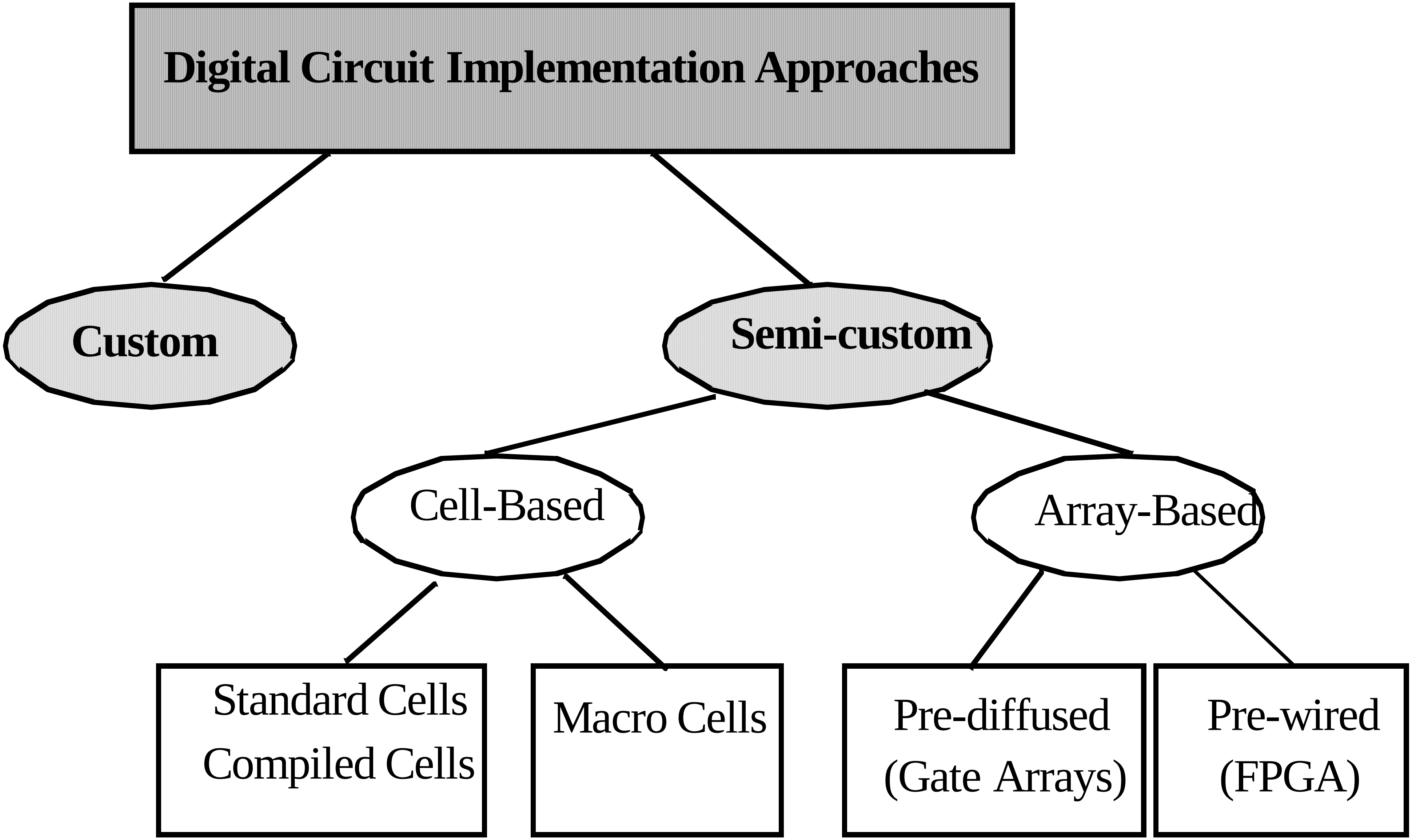



(Transistor Diagram)



(Layout Diagram)

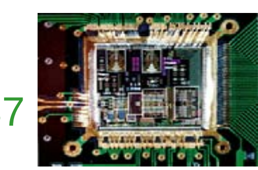
# Implementation Approaches for Digital ICs



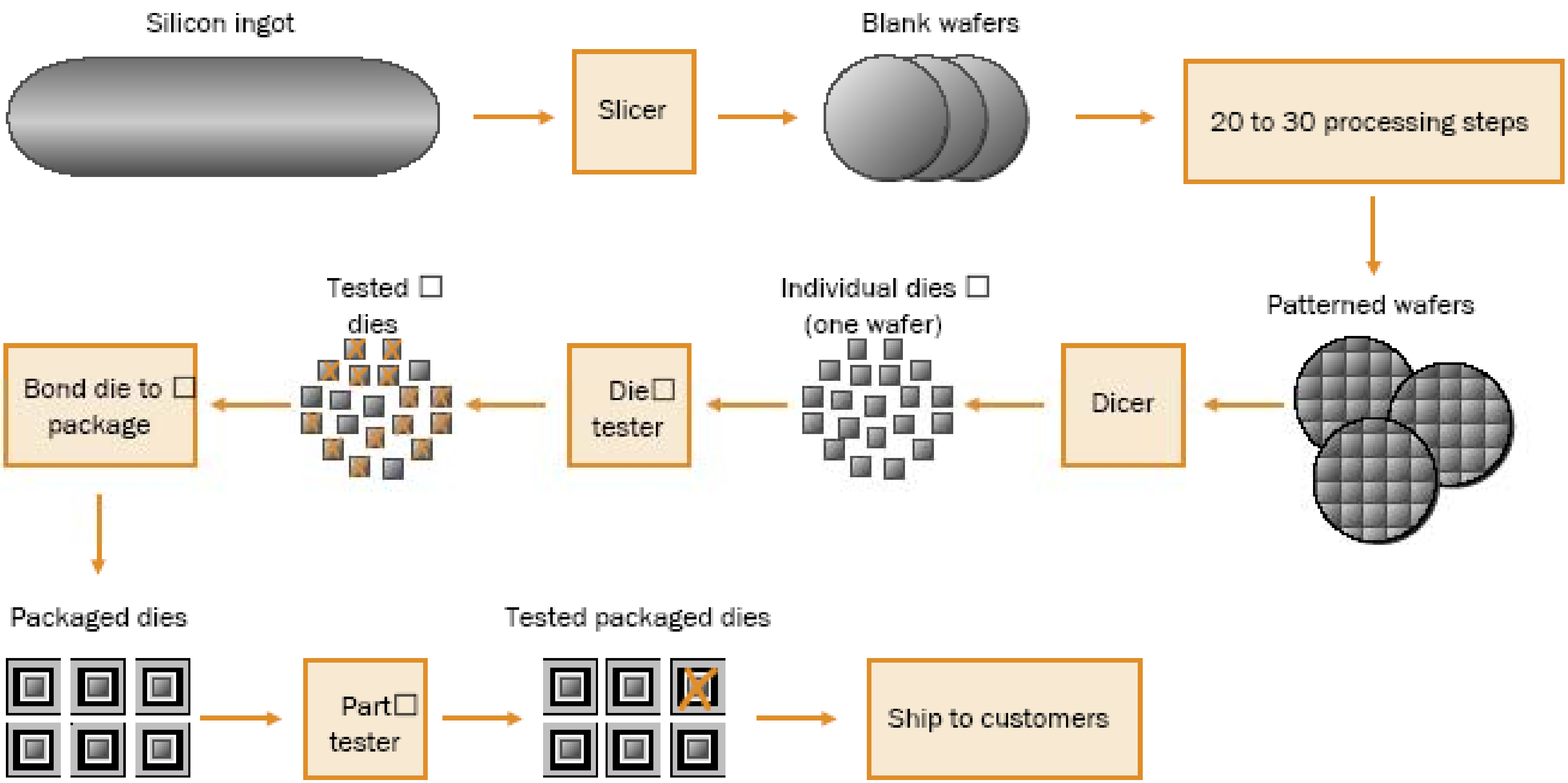
# Implementation Approaches for Digital ICs

- Full-custom: all logic cells are customized. A general purpose microprocessor is designed this way.
- Semi-custom: all of the logic cells are from predesigned cell libraries (reduces the manufacture lead time of the IC)
- Standard-cell based IC uses predesigned logic cells such as AND gates, OR gates, MUXs, FFs,.., etc.
- Macrocells (also called megacells) are larger predesigned cells, such as microcontrollers, even microprocessors, etc.
- Gate-Array, Sea-of-Gates or prediffused arrays contains array of transistors or gates which can be connected by wires to implement the chip.
- Programmable-Logic-Array (PLA) is an example of fuse-based FPGA design. (NOTE: Fuse-based, nonvolatile and volatile are three types of FPGAs)





# Digital IC Fabrication Flow



# Technology Growth and Moore's Law

# Different Attributes of an IC or chip

We will briefly discuss the VLSI technological growth based on these attributes.

- Transistor count of a chip
- Operating frequency of a chip
- Power consumption of a chip
- Power density in a chip
- Size of a device used in chip

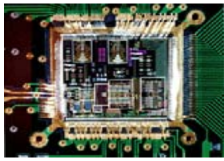
NOTE: Chip is informal name for IC.



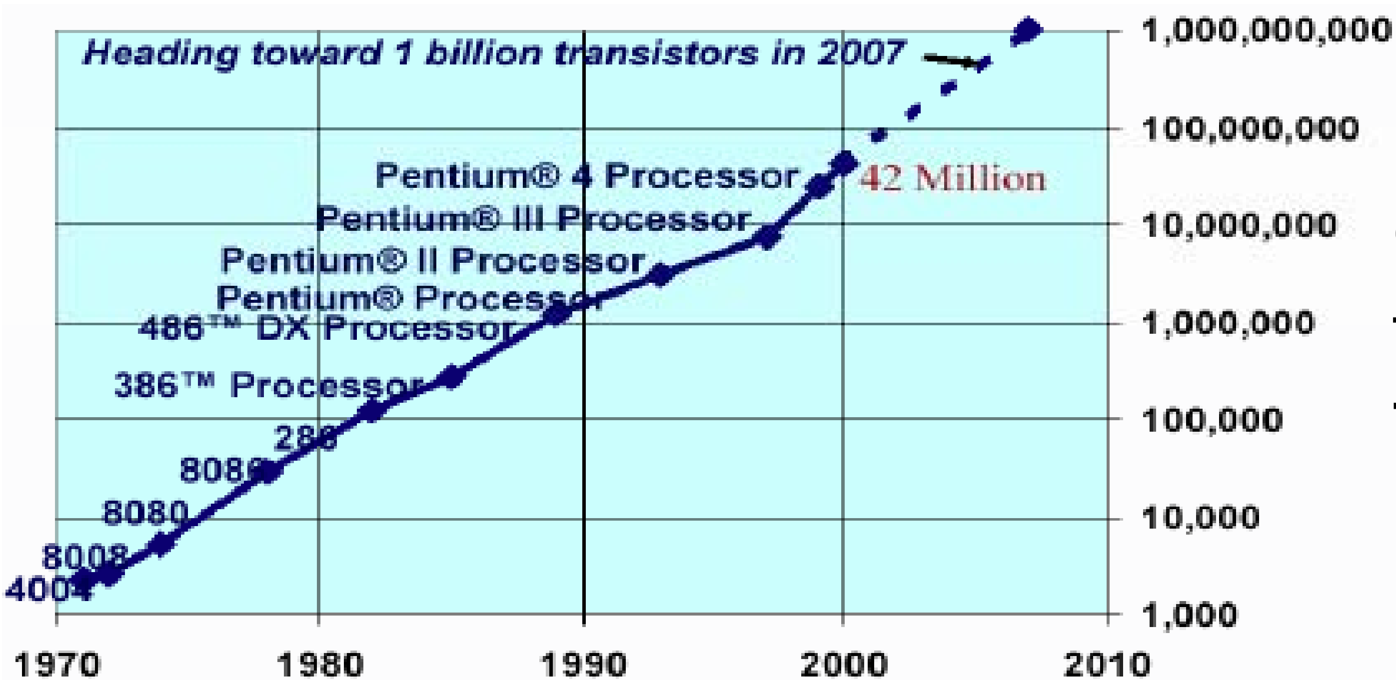
# Moore's Law

- 1965: Gordon Moore plotted transistor on each chip
  - Transistor counts have doubled every 26 months
- Many other factors grow exponentially
  - clock frequency
  - processor performance

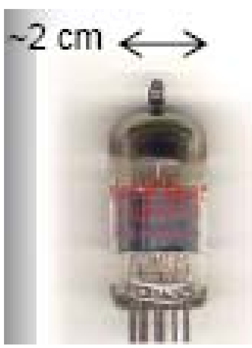


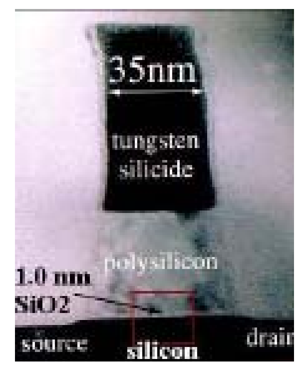


# VLSI Trend



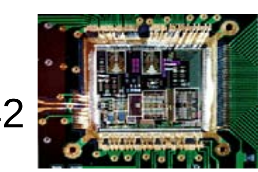

Power, Operating frequency, and Throughput have increased.



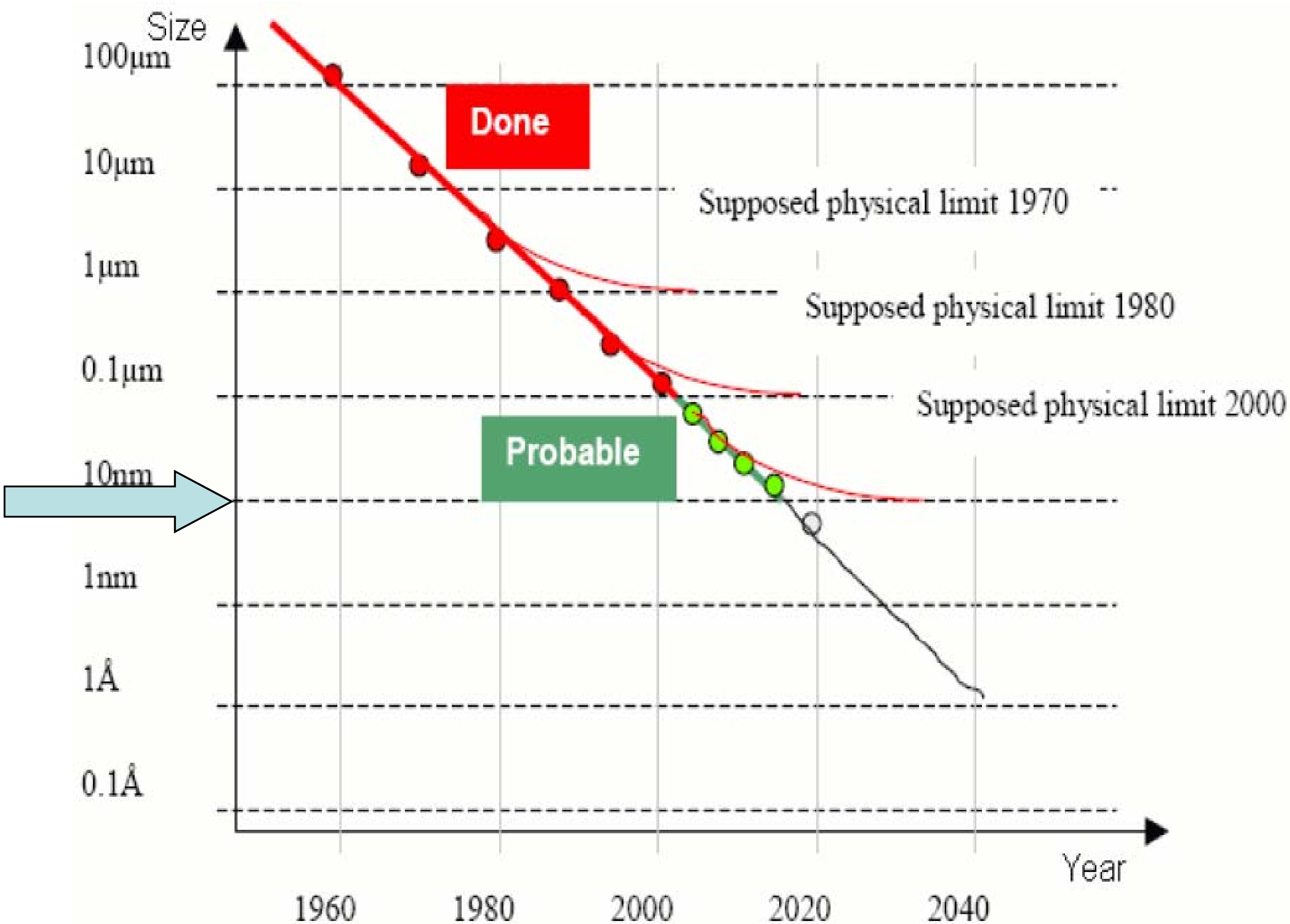




**VLSI technology is the fastest growing technology in human history.**



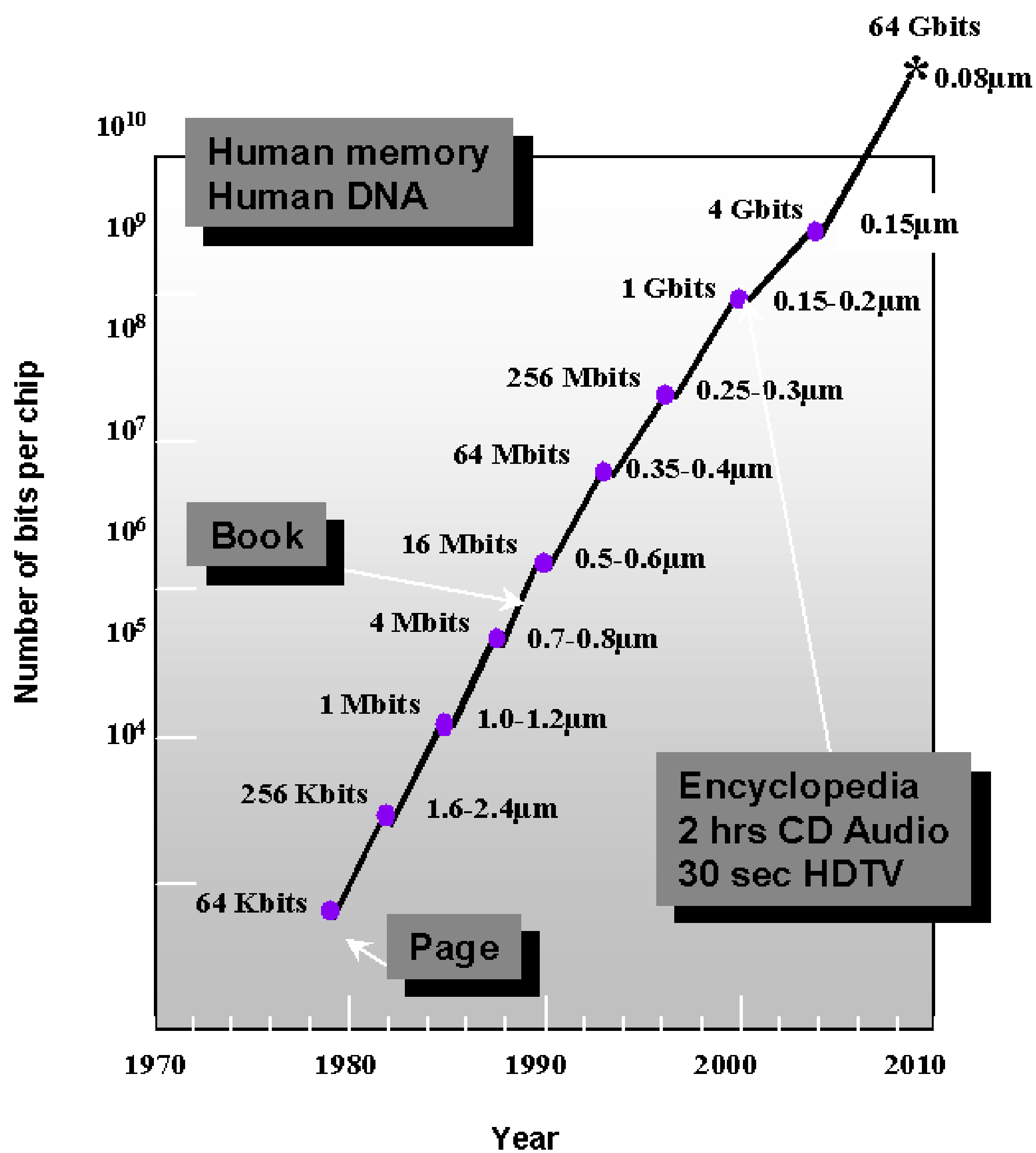


# Technology Scaling Trend




Source: Bendhia 2003

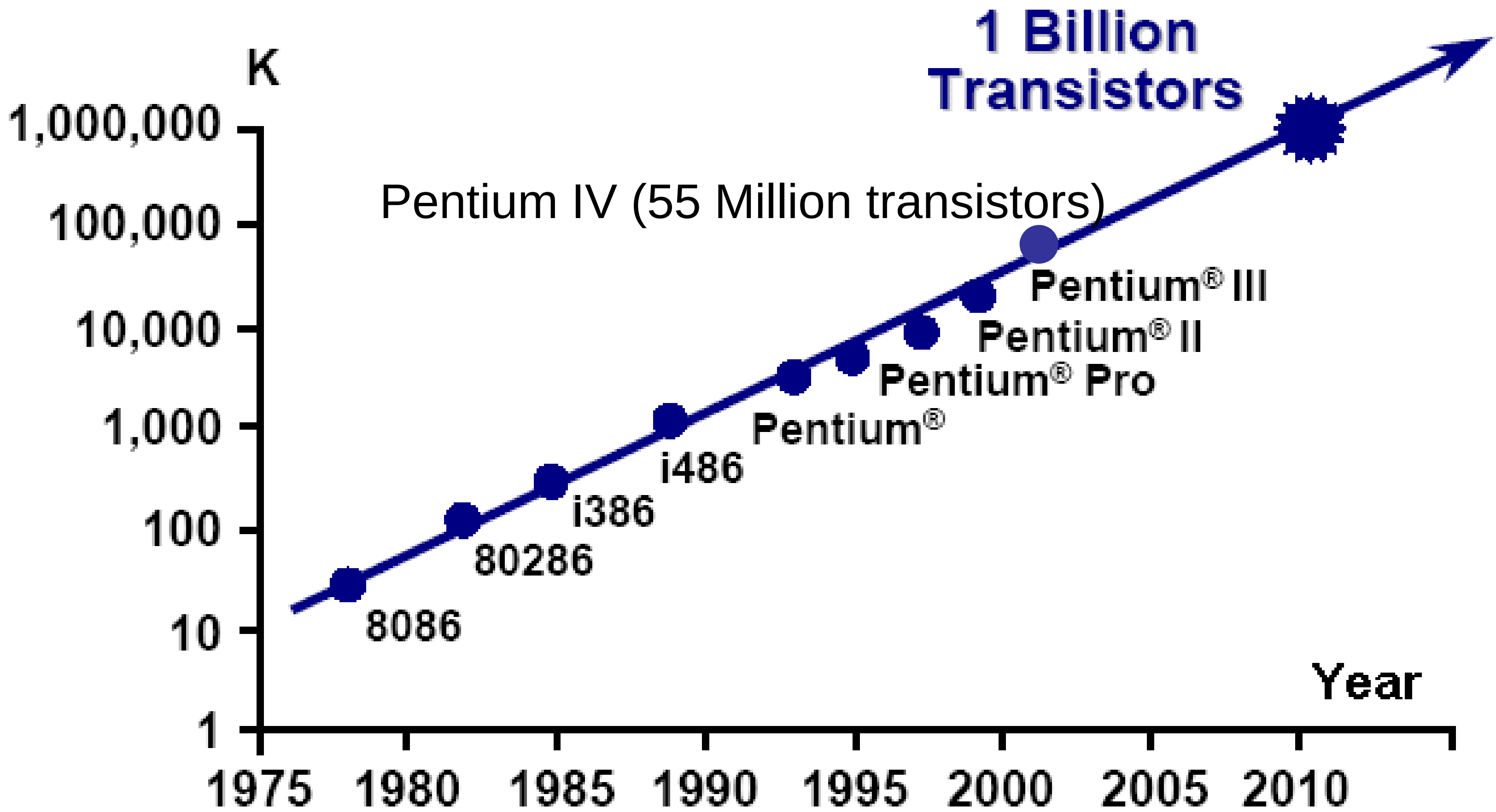
# Evolution in Complexity



# Why Scaling?

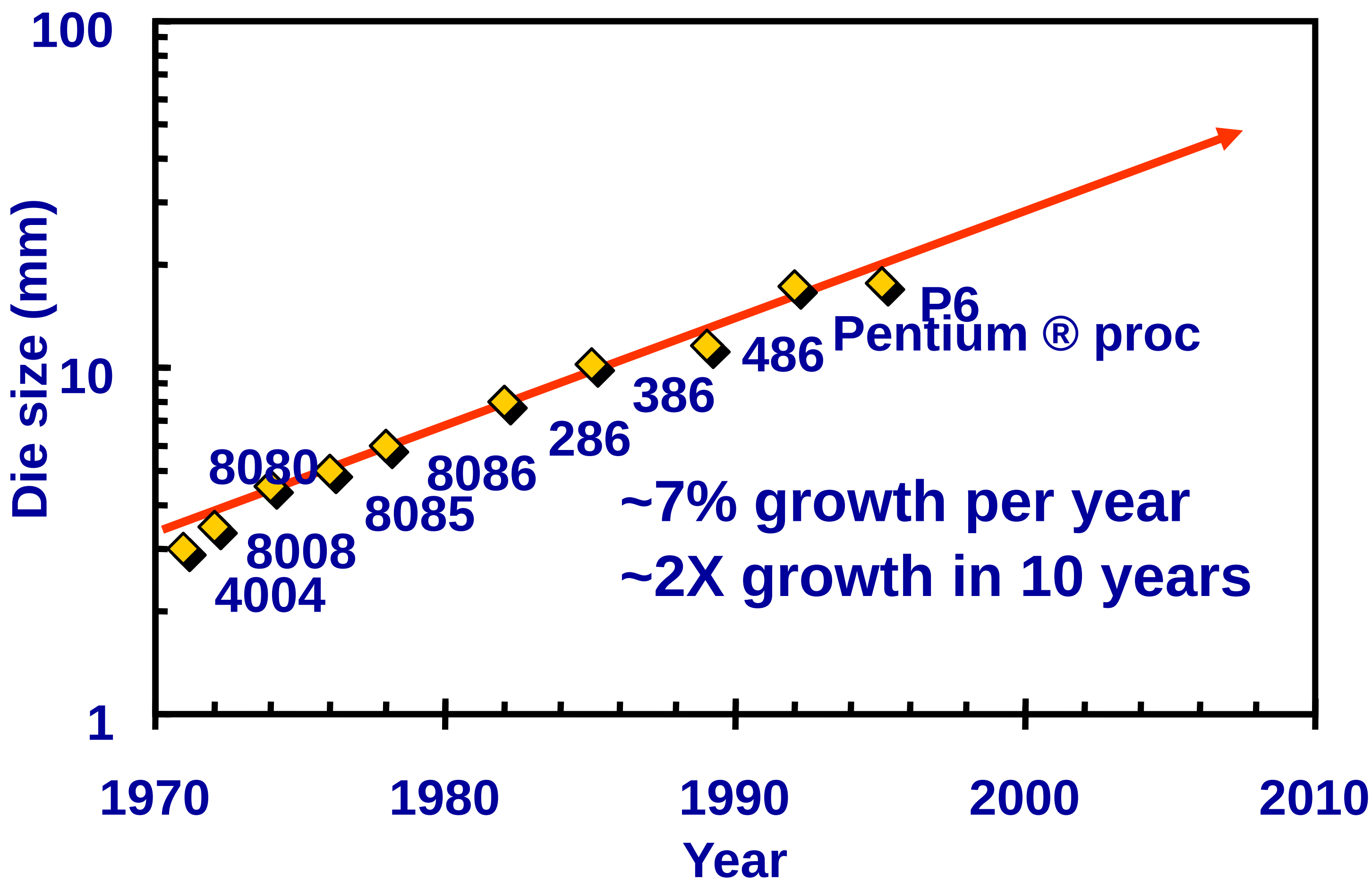
- Technology shrinks by 0.7/generation
- With every generation can integrate 2x more functions per chip; chip cost does not increase significantly
- Cost of a function decreases by 2x
- But …
  - How to design chips with more and more functions?
  - Design engineering population does not double every two years…
- Hence, a need for more efficient design methods
  - Exploit different levels of abstraction

# Increase in Transistor Count



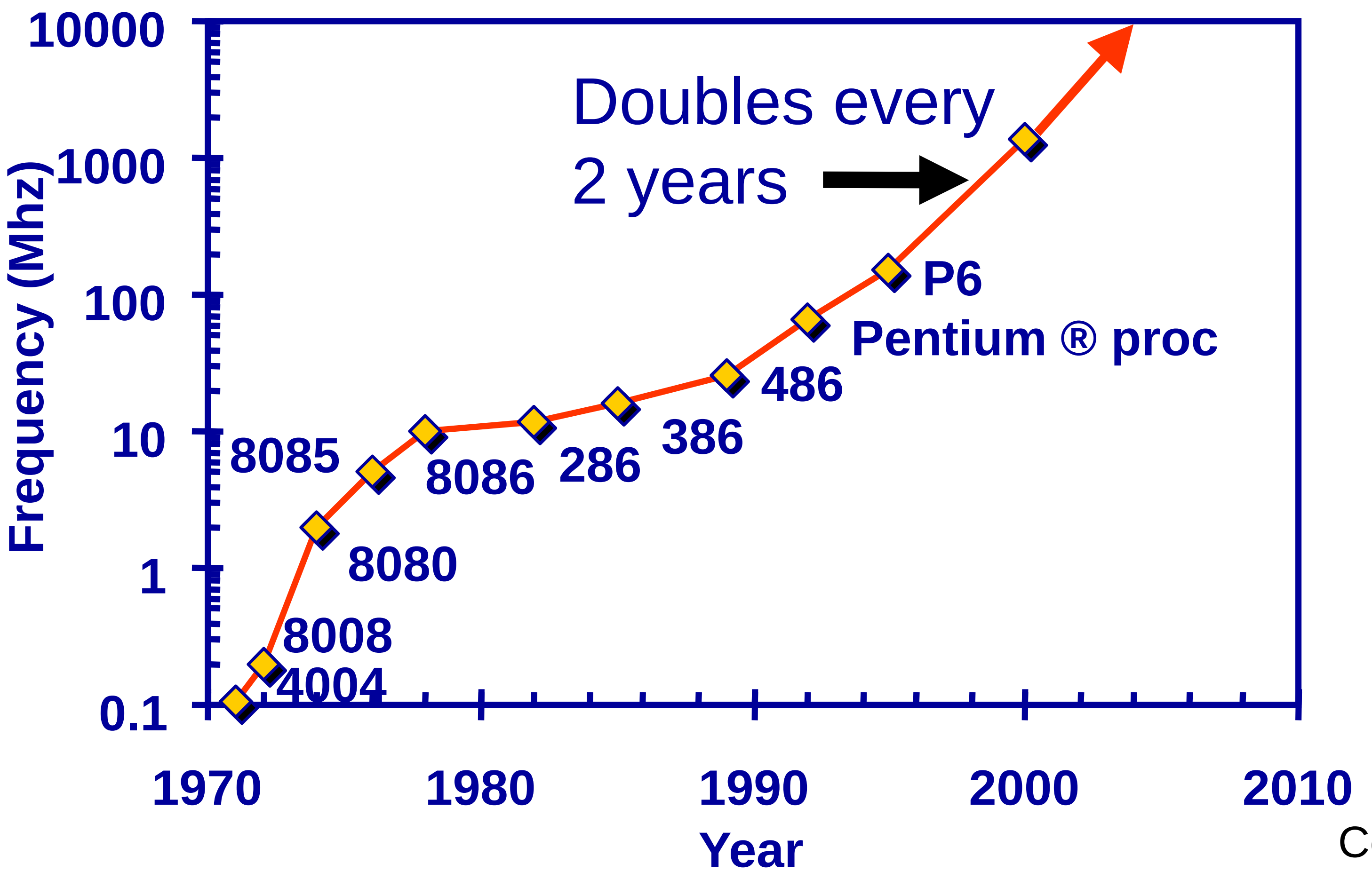

**Transistors on Lead Microprocessors double every 2 years**

# Die Size Growth




**Die size grows by 14% to satisfy Moore's Law**

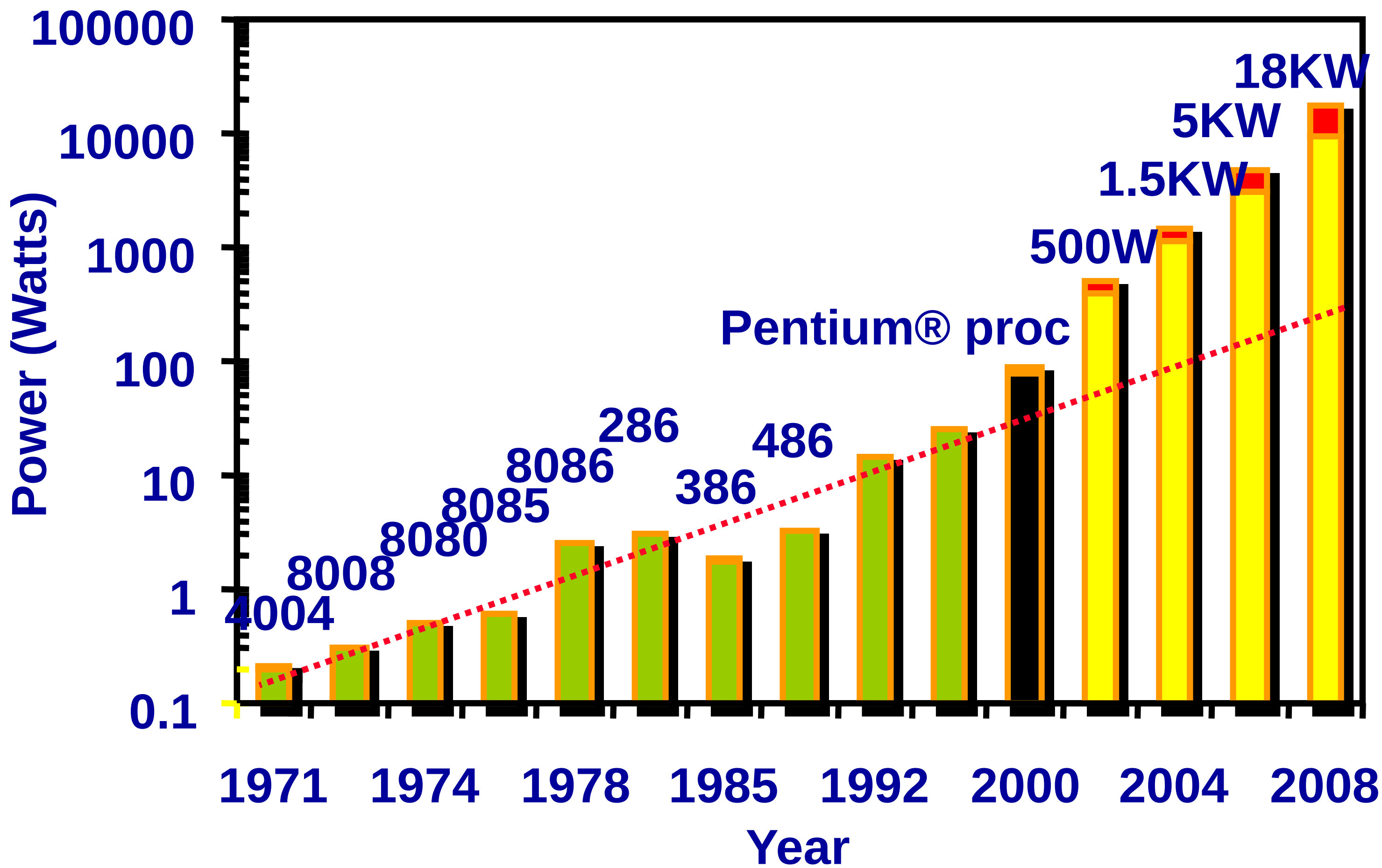
# Increase in Operating Frequency




Courtesy, Intel

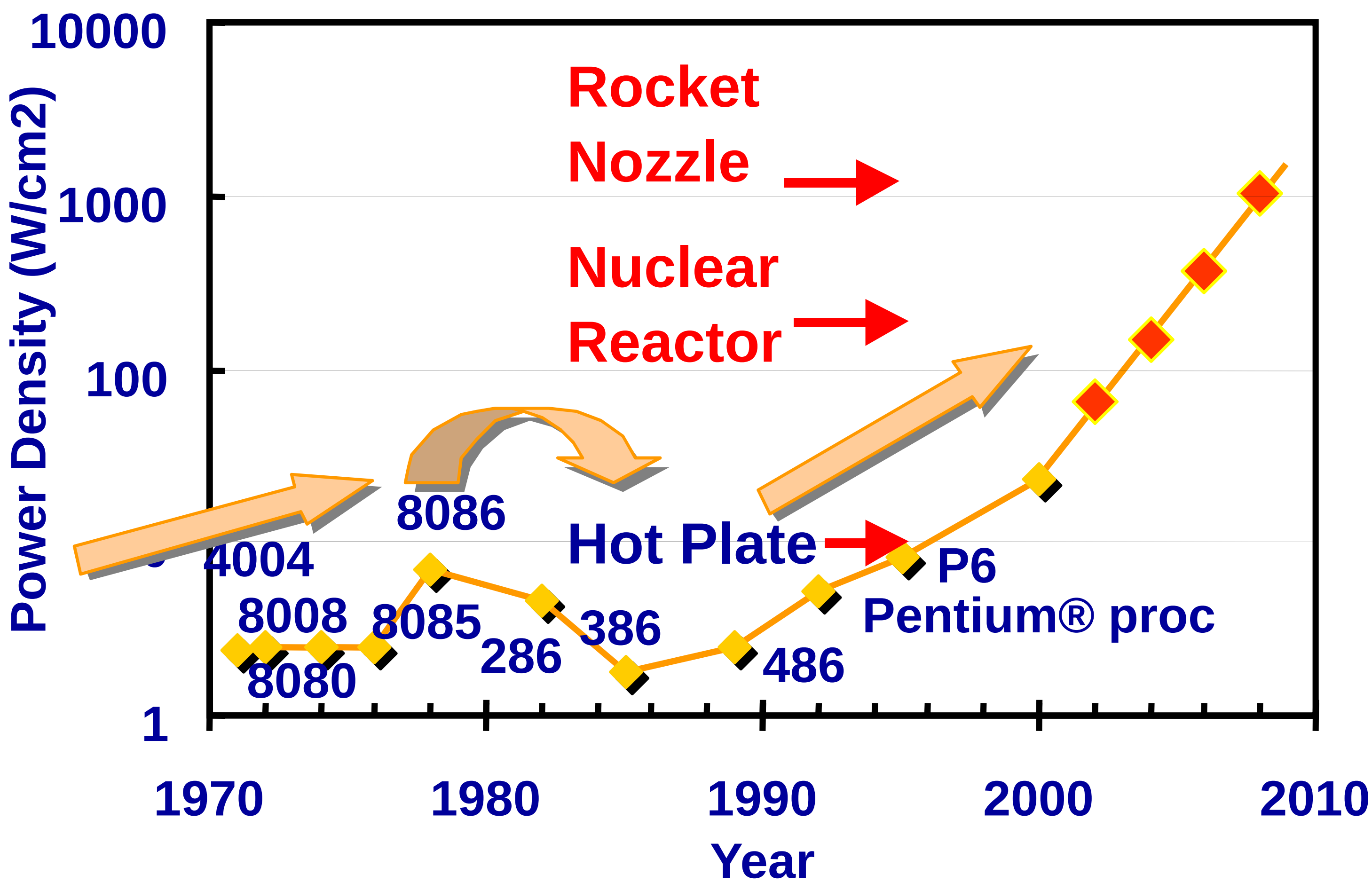
**Lead Microprocessors frequency doubles every 2 years**

# Power will be a major problem




**Power delivery and dissipation will be prohibitive**

# Power density




**Power density too high to keep junctions at low temp**

# Challenges in Digital Design

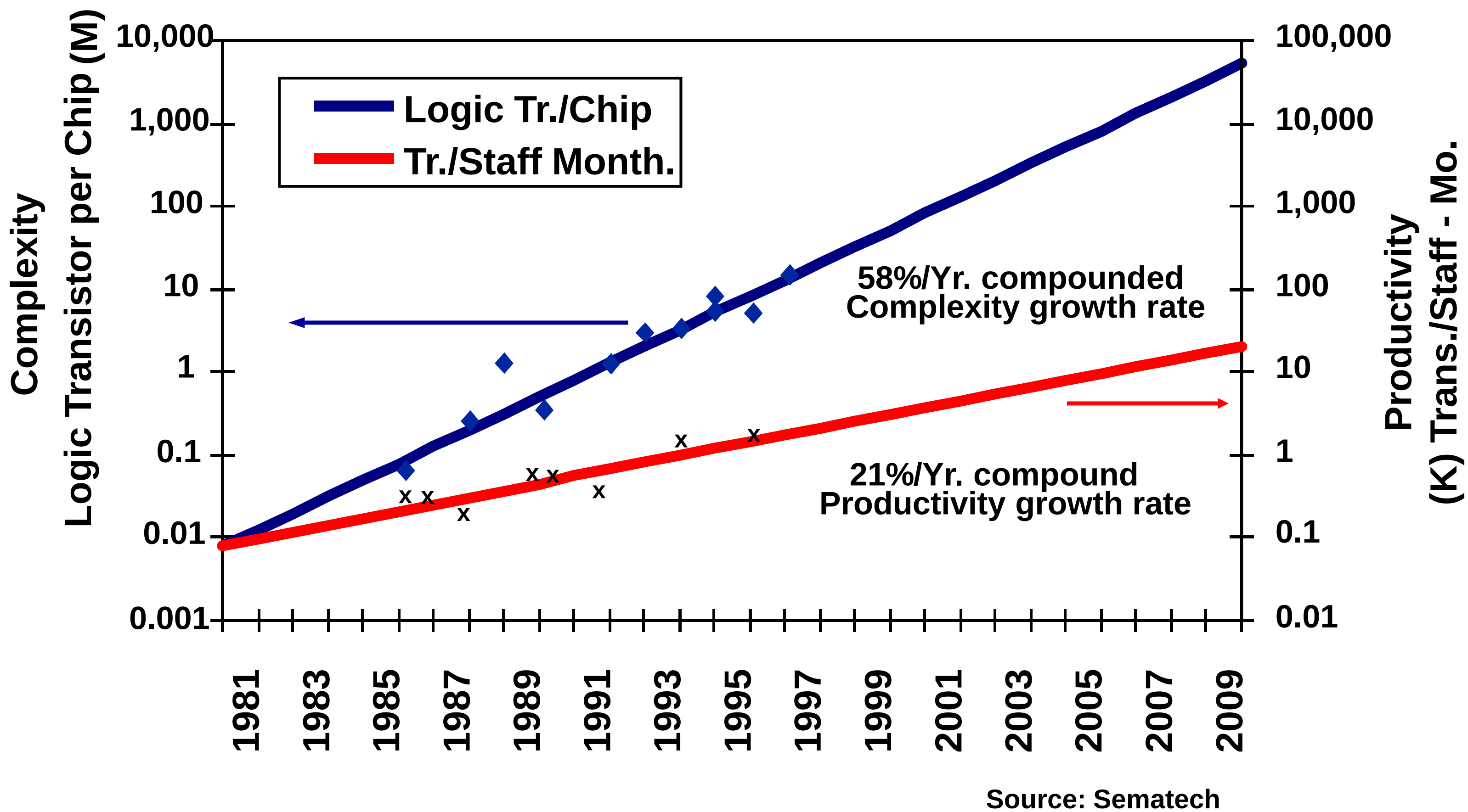
**"Microscopic Problems"**
- Ultra-high speed design
- Interconnect
- Noise, Crosstalk
- Reliability, Manufacturability
- Power Dissipation
- Clock distribution.


**"Macroscopic Issues"**
- Time-to-Market
- Millions of Gates
- High-Level Abstractions
- Reuse & IP: Portability
- Predictability
- etc.

**Everything Looks a Little Different**

**…and There's a Lot of Them!**

# Productivity Trends




**Complexity outpaces design productivity**

Courtesy, ITRS Roadmap

# Circuit Design Metrics

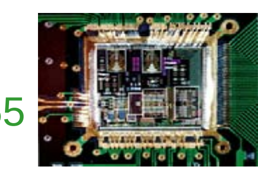
# Design Metrics

- How to evaluate performance of a digital circuit (gate, block, …)?
  - Cost
  - Reliability
  - Scalability
  - Speed (delay, operating frequency)
  - Power dissipation
  - Energy to perform a function

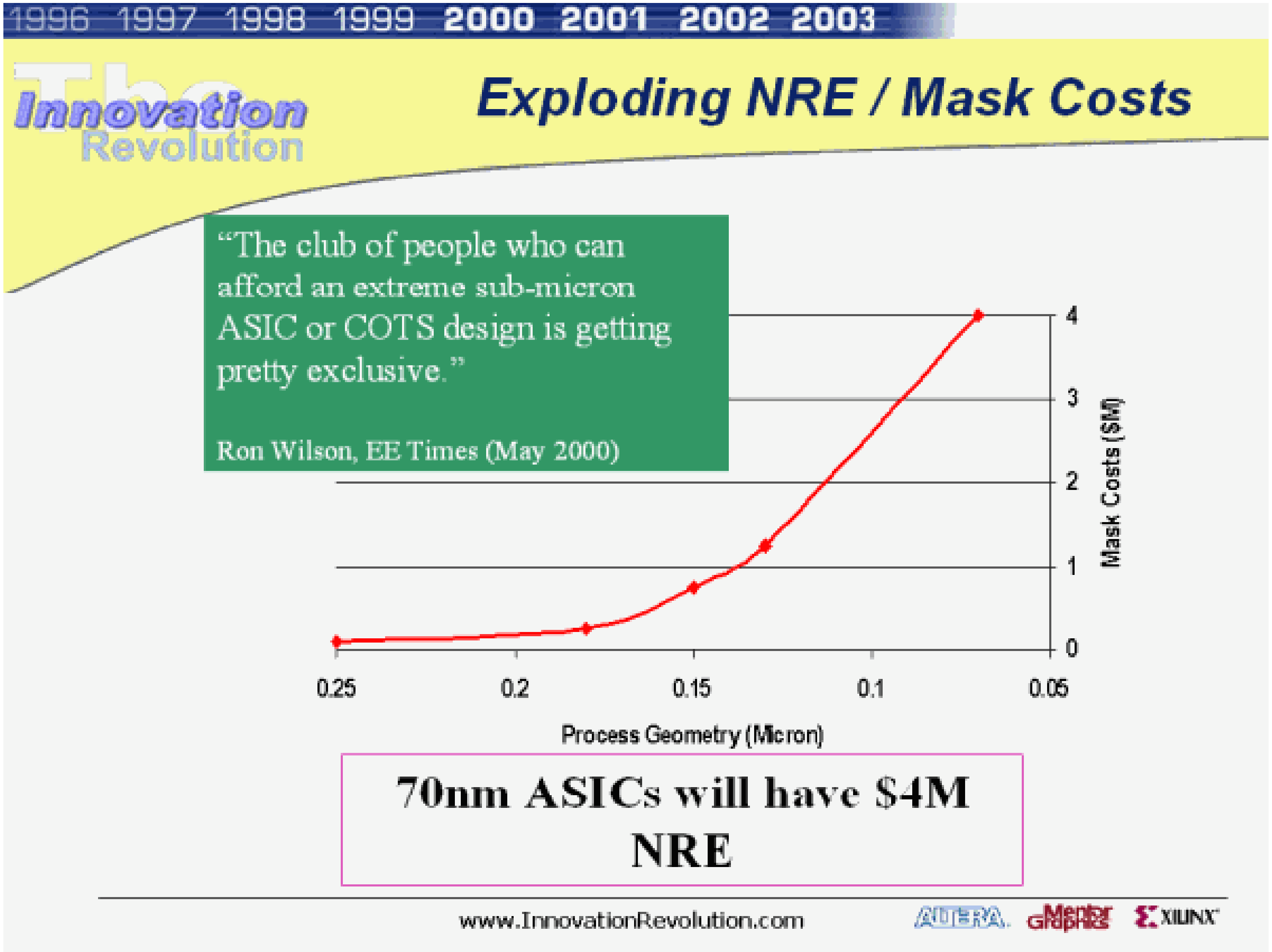
# Cost of Integrated Circuits

- NRE (non-recurrent engineering) costs
  - design time and effort, mask generation
  - one-time cost factor
- Recurrent costs
  - silicon processing, packaging, test
  - proportional to volume
  - proportional to chip area

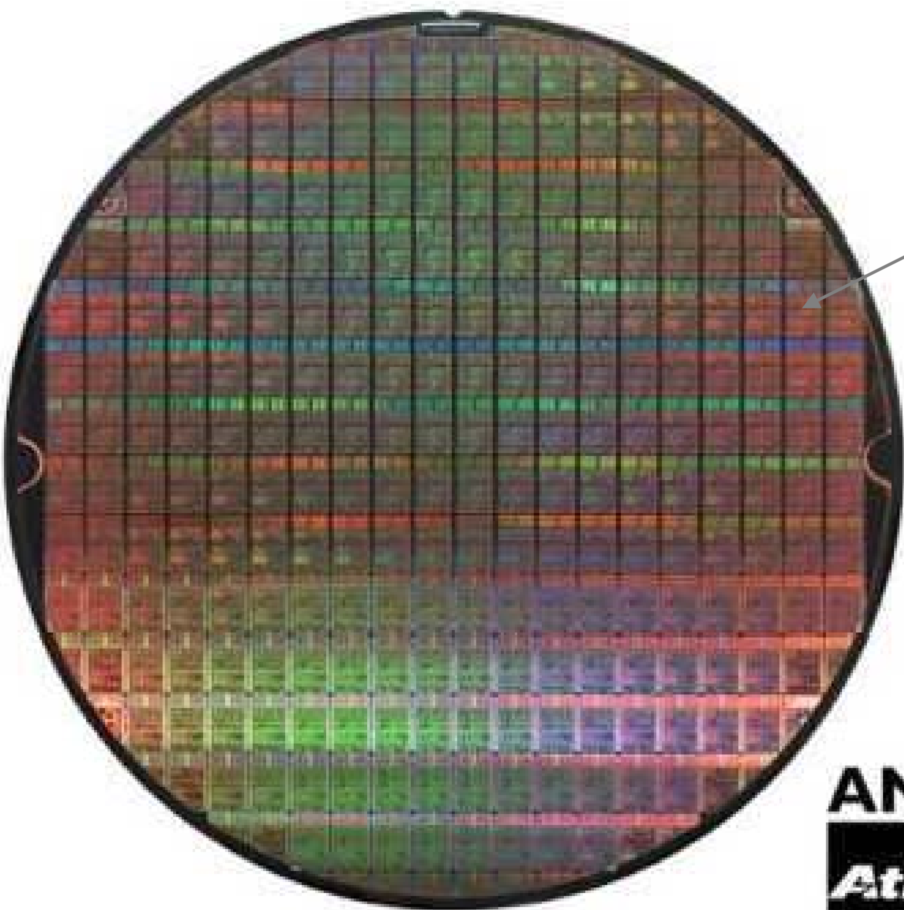




# NRE Cost is Increasing



# Die Cost

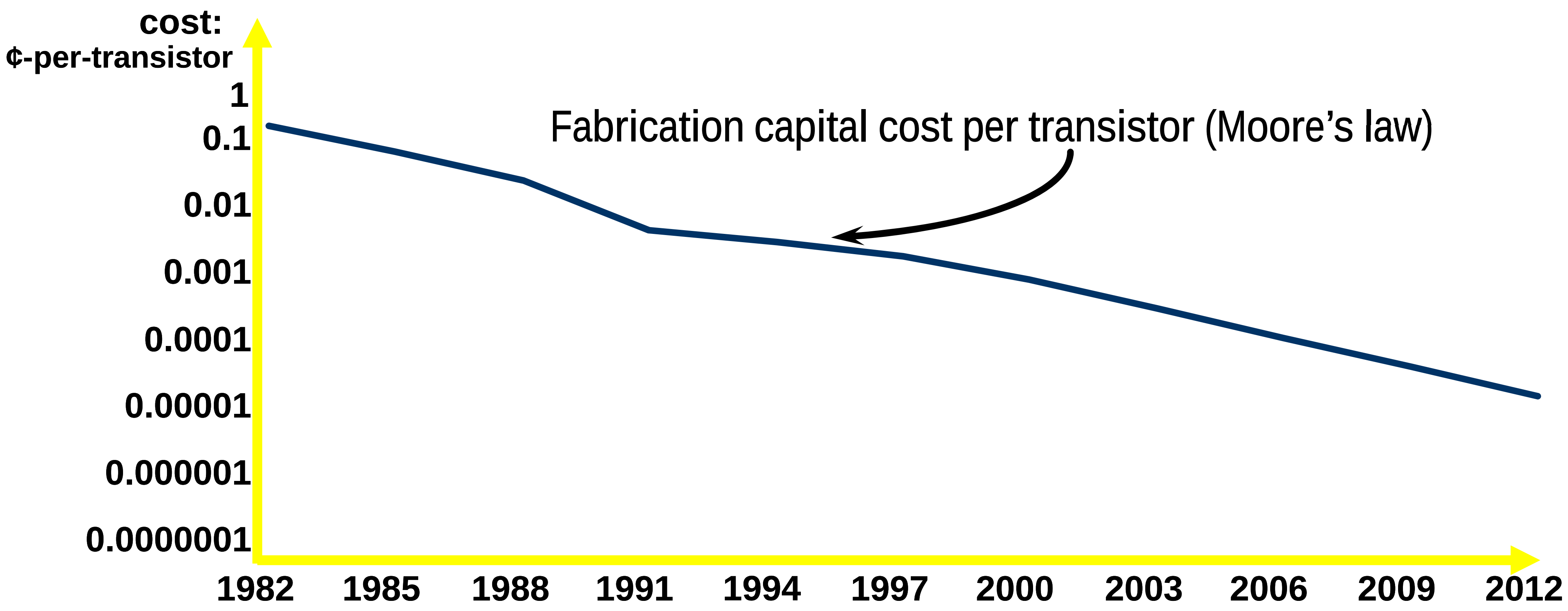


Single die

Wafer

Going up to 12” (30cm)

# Cost per Transistor

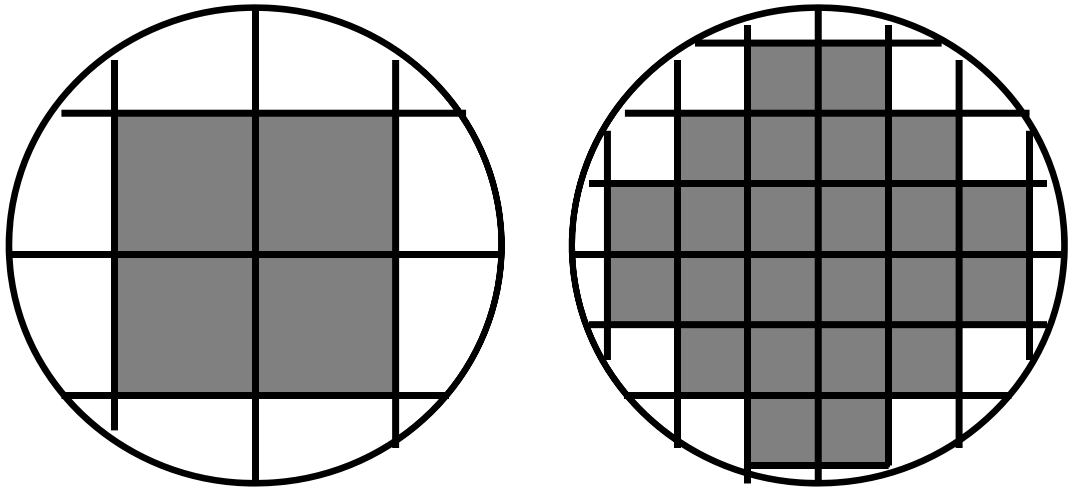


# Die Yield

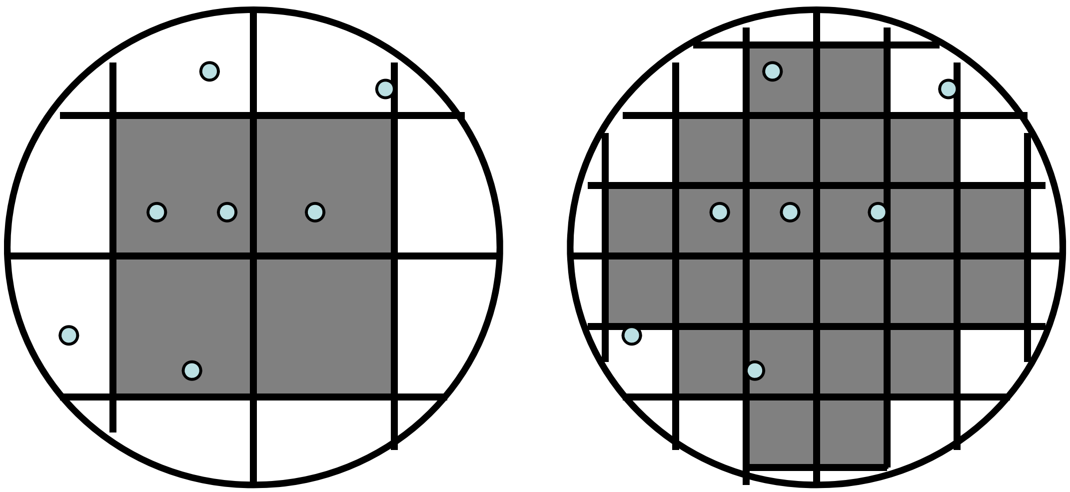
$$Y = \frac{\text{No. of good chips per wafer}}{\text{Total number of chips per wafer}} \times 100\%$$

$$\text{Die cost} = \frac{\text{Wafer cost}}{\text{Dies per wafer} \times \text{Die yield}}$$

$$\text{Dies per wafer} = \frac{\pi \times (\text{wafer diameter}/2)^2}{\text{die area}} - \frac{\pi \times \text{wafer diameter}}{\sqrt{2 \times \text{die area}}}$$



# Die Defects



$$\text{die yield} = \left(1 + \frac{\text{defects per unit area} \times \text{die area}}{\alpha}\right)^{-\alpha}$$

$\alpha$ is approximately 3

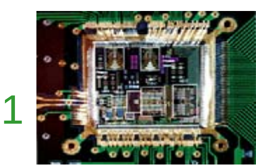
$$\text{die cost} = f\,(\text{die area})^4$$

NOTE: Solve Example 1.3 , page-18 of Rabaey text book.

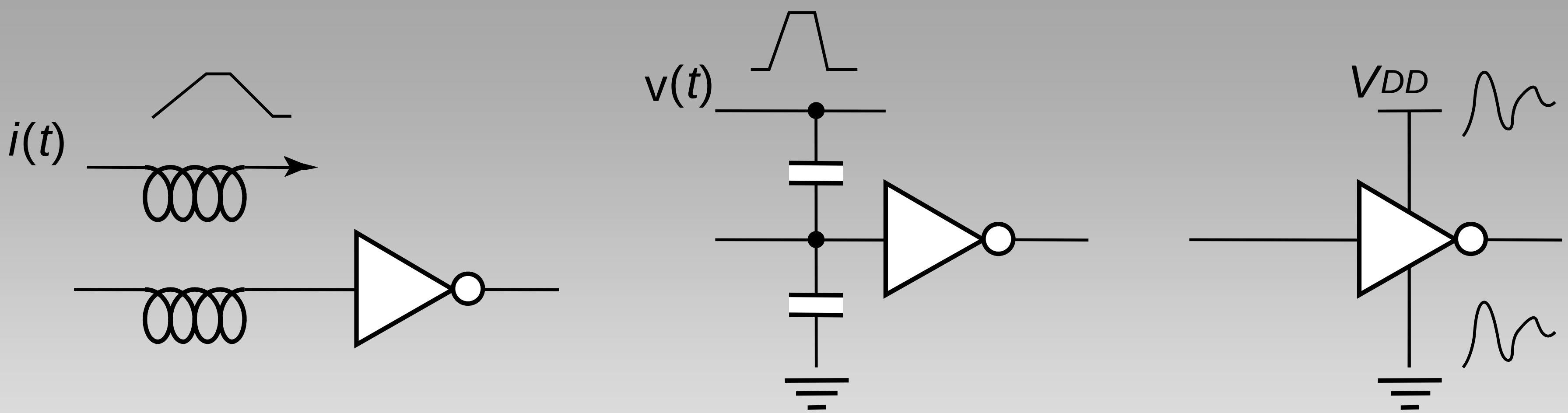
# Some Examples (1994)

| Chip | Metal layers | Line width | Wafer cost | Def./ $cm^2$ | Area $mm^2$ | Dies/ wafer | Yield | Die cost |
|---|---|---|---|---|---|---|---|---|
| 386DX | 2 | 0.90 | $900 | 1.0 | 43 | 360 | 71% | $4 |
| 486 DX2 | 3 | 0.80 | $1200 | 1.0 | 81 | 181 | 54% | $12 |
| Power PC 601 | 4 | 0.80 | $1700 | 1.3 | 121 | 115 | 28% | $53 |
| HP PA 7100 | 3 | 0.80 | $1300 | 1.0 | 196 | 66 | 27% | $73 |
| DEC Alpha | 3 | 0.70 | $1500 | 1.2 | 234 | 53 | 19% | $149 |
| Super Sparc | 3 | 0.70 | $1700 | 1.6 | 256 | 48 | 13% | $272 |
| Pentium | 3 | 0.80 | $1500 | 1.5 | 296 | 40 | 9% | $417 |



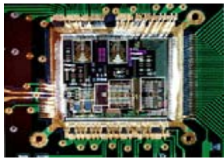


# Reliability—
# Noise in Digital Integrated Circuits

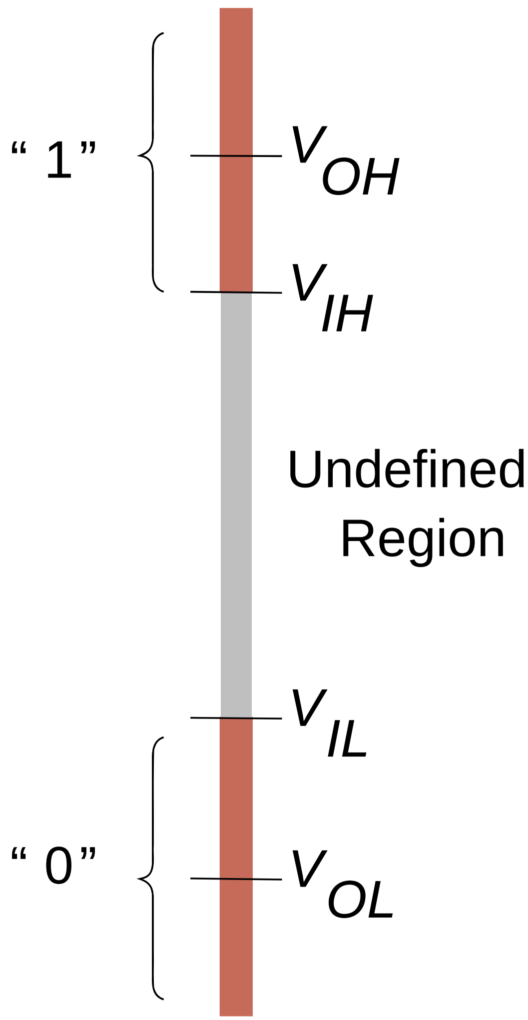


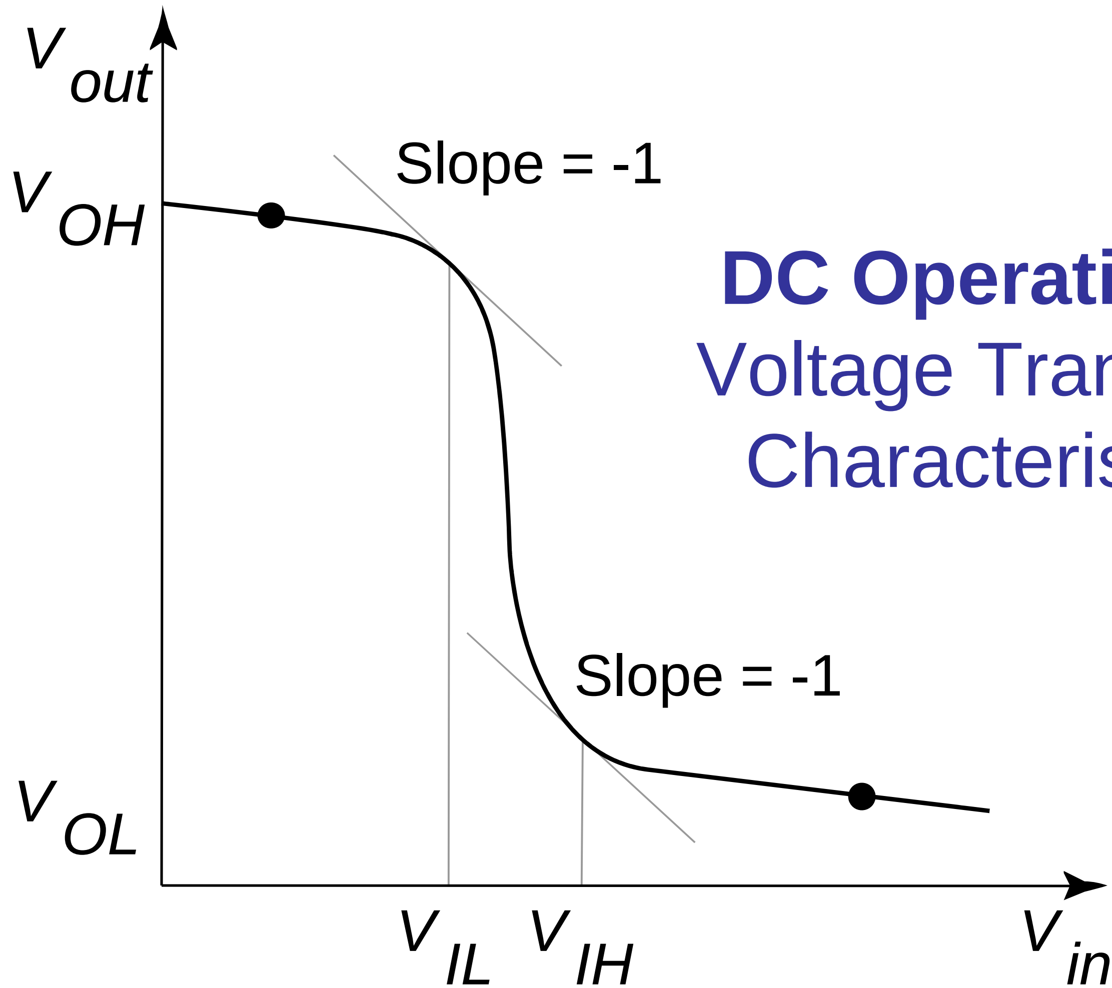

**Inductive coupling** **Capacitive coupling** **Power and ground noise**





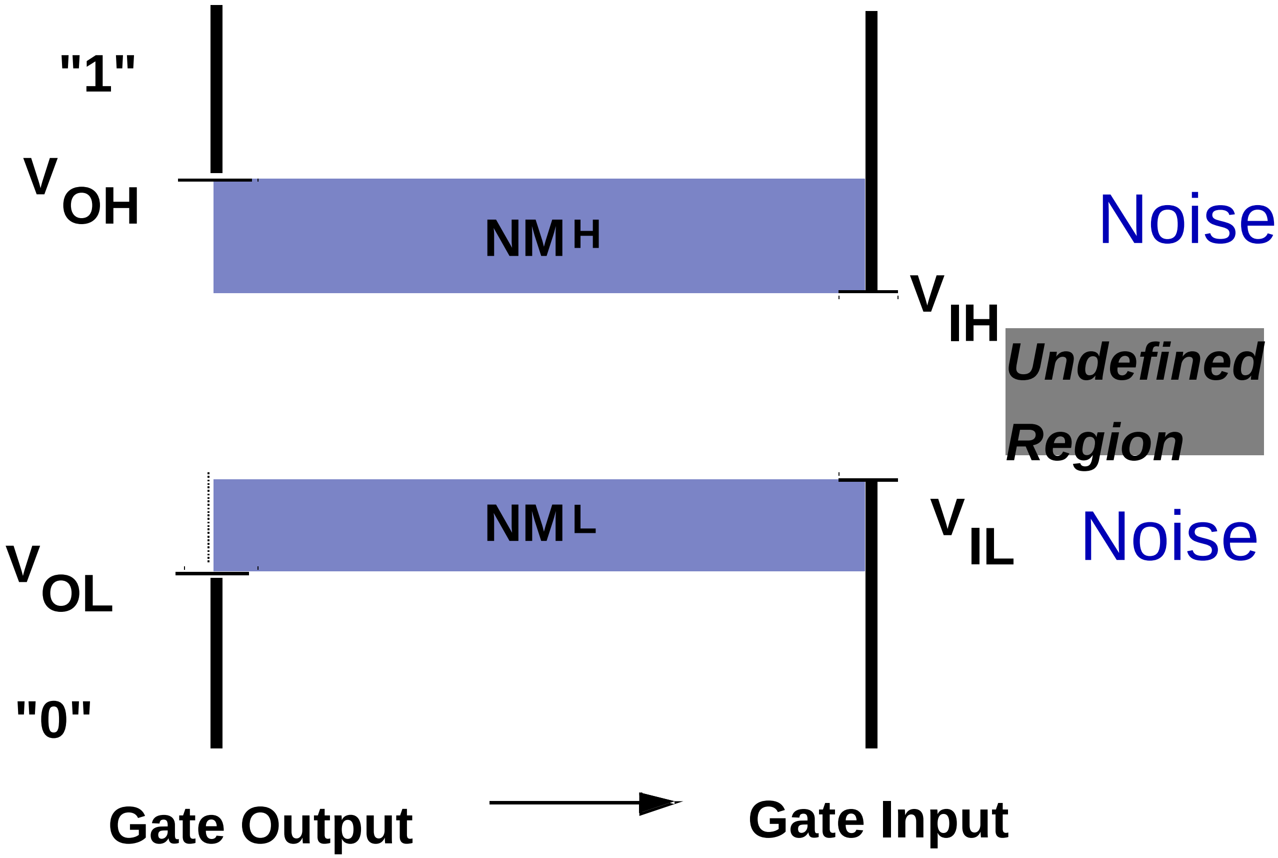
# Mapping between analog and digital signals




**DC Operation:**
Voltage Transfer Characteristic

# Definition of Noise Margins




Noise margin high

Noise margin low

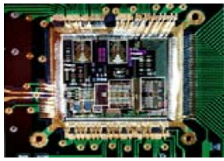
# Noise Budget

- Allocates gross noise margin to expected sources of noise
- Sources: supply noise, cross talk, interference, offset
- Differentiate between fixed and proportional noise sources

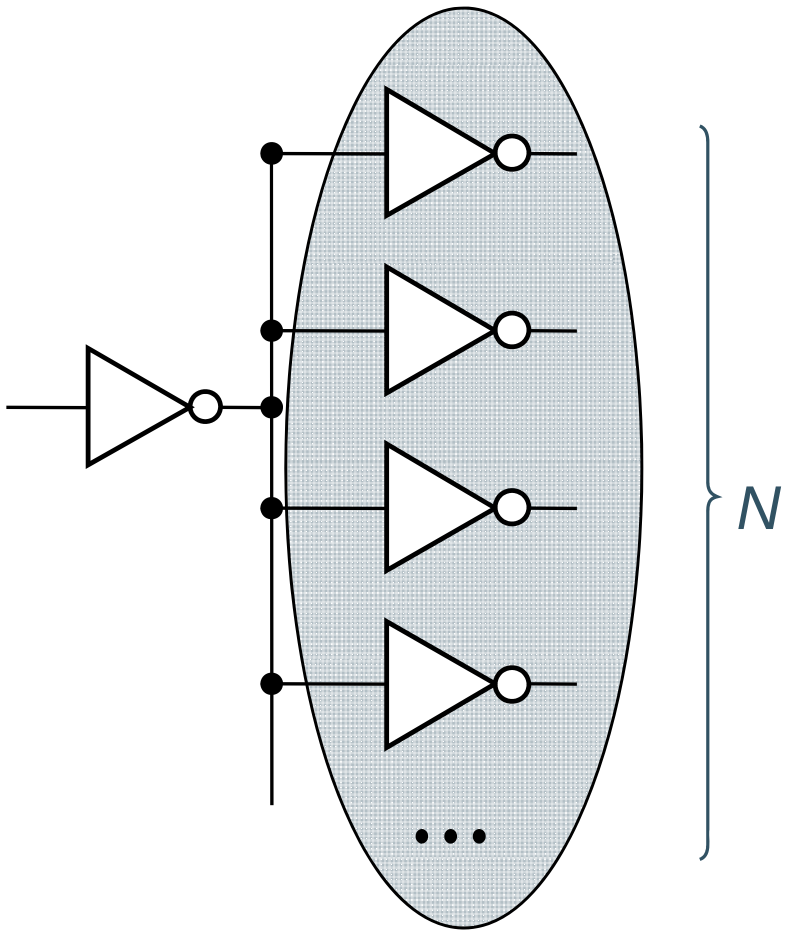
# Key Reliability Properties

- Absolute noise margin values are deceptive
  - a floating node is more easily disturbed than a node driven by a low impedance (in terms of voltage)
- Noise immunity is the more important metric – the capability to suppress noise sources
- Key metrics: Noise transfer functions, Output impedance of the driver and input impedance of the receiver;

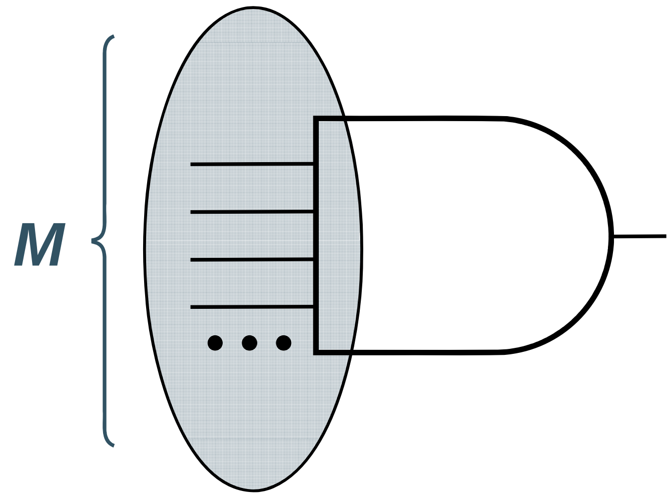




# Fan-in and Fan-out

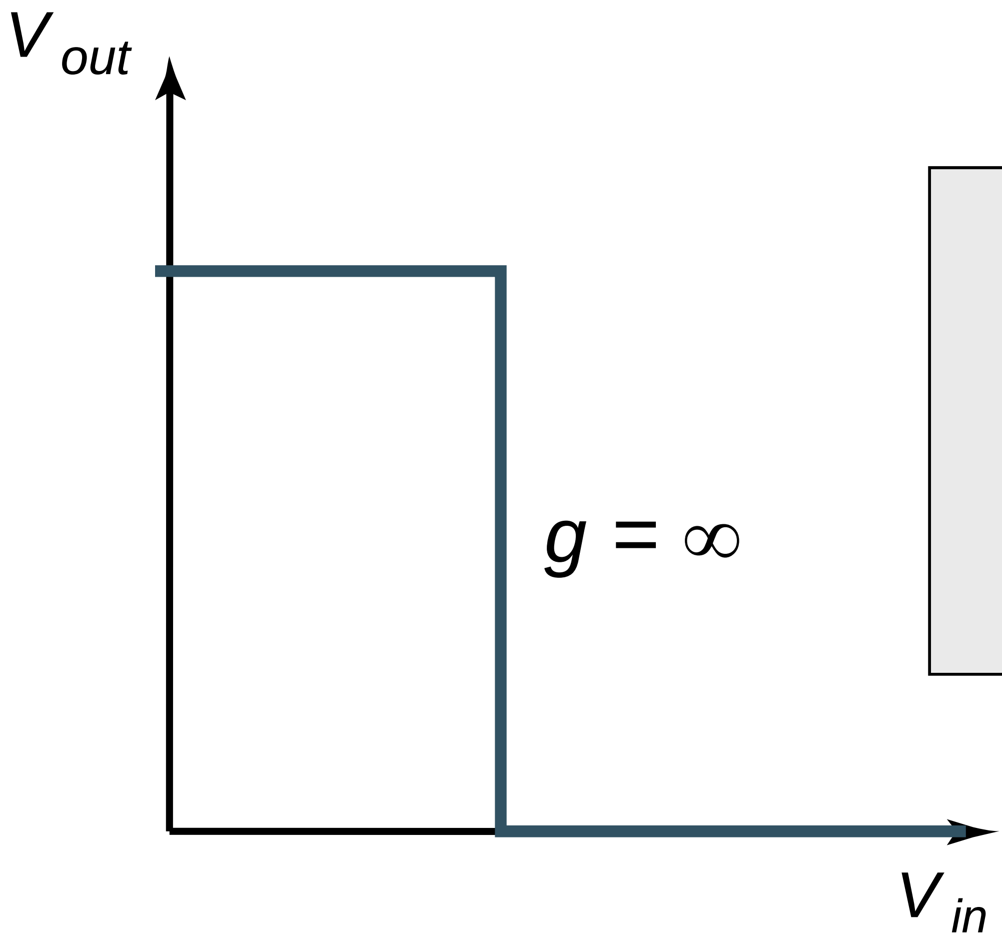



Fan-out *N*




Fan-in *M*

# The Ideal Gate



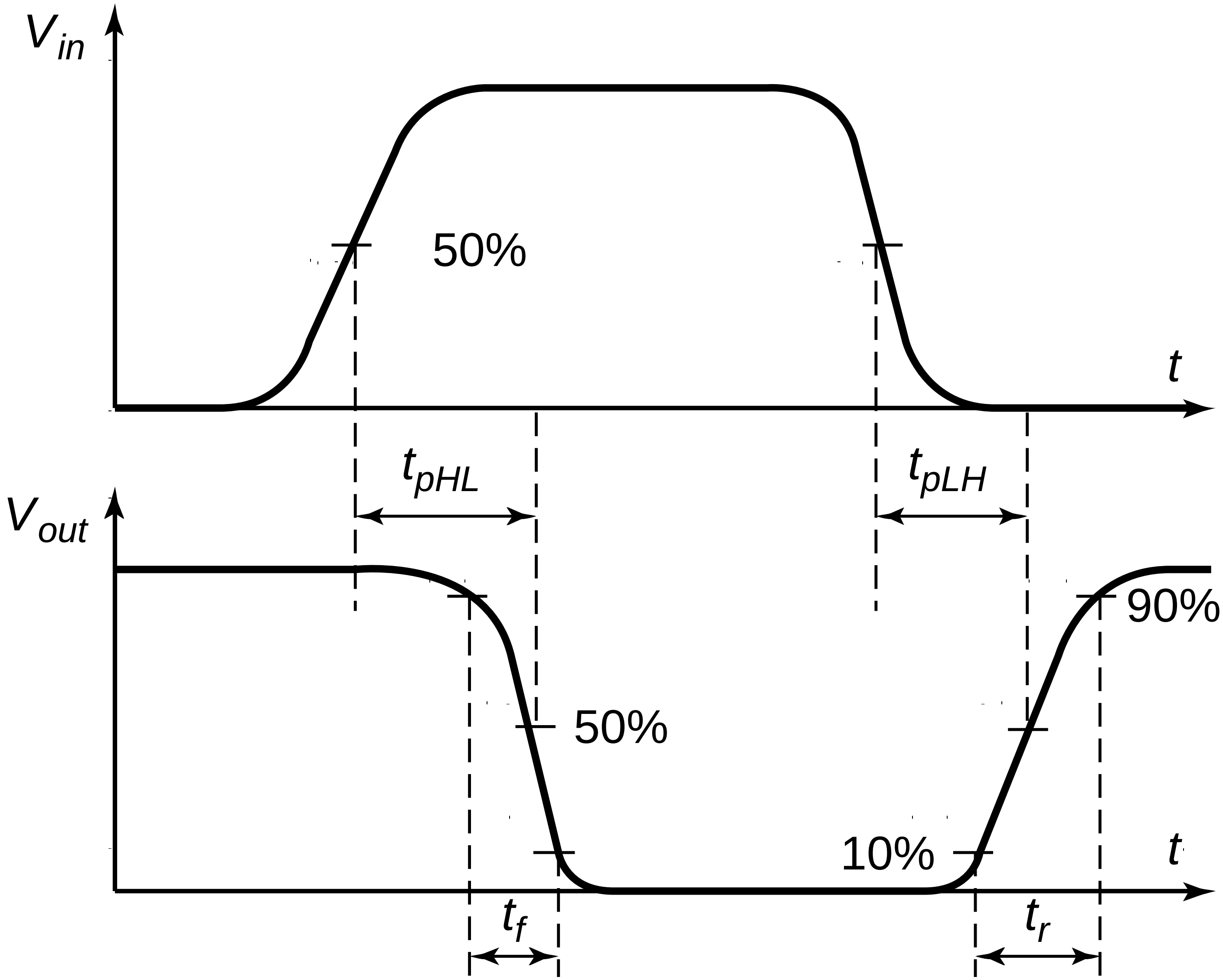

$R_i = \infty$

$R_o = 0$

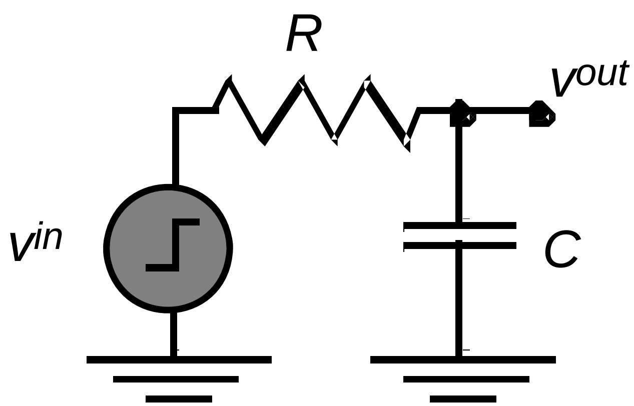
Fanout $= \infty$

$NM_H = NM_L = V_{DD}/2$

# Delay Definitions



# A First-Order RC Network




$$v_{out}(t) = (1 - e^{-t/\tau})\, V$$

$t_p = \ln(2)\, t = 0.69\, RC$

Important model – matches delay of inverter

# Power Dissipation

Instantaneous power:

$$p(t) = v(t)i(t) = V_{supply}i(t)$$

Peak power:

$$P_{peak} = V_{supply}i_{peak}$$

Average power:

$$P_{ave} = \frac{1}{T}\int_{t}^{t+T} p(t)dt = \frac{V_{supply}}{T}\int_{t}^{t+T} i_{supply}(t)dt$$

# Energy and Energy-Delay

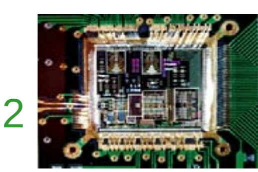
Power-Delay Product (PDP) =

E = Energy per operation = $P_{av} \times t_p$

Energy-Delay Product (EDP) =

quality metric of gate = $E \times t_p$





# Summary

- Digital integrated circuits have come a long way and still have quite some potential left for the coming decades
- Some interesting challenges ahead
  - Getting a clear perspective on the challenges and potential solutions is the purpose of this book
- Understanding the design metrics that govern digital design is crucial
  - Cost, reliability, speed, power and energy dissipation