CSCE 5730/4730: Digital CMOS VLSI Design

Assignment # 2, Total Points = 4*25 = 100.
Assigned Date: 22nd Sep 2010 (Wed), Due Date: 29th Sep 2010 (Wed)
Instructor: Dr. Saraju P. Mohanty

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1. Using LTspice simulate the "inverter" logic gate circuit discussed in the class for functional verification.
2. Using LTspice simulate the "NAND" logic gate circuit discussed in the class for functional verification.
3. Assume a wafer size of 12inches, a die size of 3.6cm^2, 1.6$defects/cm^2$, and α=3. Determine the die yield of this CMOS process run.
4. Consider design of a JPEG chip. Explain different levels of digital design abstraction through this chip. Do some quick reading on JPEG standard to explain design decisions.