CSCE 5730/4730: Digital CMOS VLSI Design

Assignment # 3, Total Marks = 100 points.
Assigned Date: 11th Mar 2009 (Wed), Due Date: 23rd Mar 2009 (Mon)
Instructor: Dr. Saraju P. Mohanty

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1. Using microwind perform the physical design (i.e. layout) of static CMOS realization of basic logic gates (Inverter/NAND/NOR/AND/OR). Perform their simulation to verify the truth tables. (20 points for each gate)