CSCE 5730/4730: Digital CMOS VLSI Design

Assignment # 1, Total Marks = 5*20 = 100.
Assigned Date: 11th Feb 2009 (Wed), Due Date: 18th Feb 2009 (Wed)
Instructor: Dr. Saraju P. Mohanty

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1. Give a list of five leading journals in the area of VLSI, VLSI design automation. Provide their publishers name and also their homepage URL from publishers or editors.
2. Give a list of five leading conferences in the area of VLSI, VLSI design automation. Provide their native homepage URL and last two years (2008 and 2007) venue.
3. Give a list of five free and/or commercial CAD tools. Explain the capabilities of each one of them.
4. Assume a wafer size of 14inches, a die size of 3.8cm^2, 1.8defects/cm^2, and α=3. Determine the die yield of this CMOS process run.
5. Consider design of a JPEG chip. Explain different levels of digital design abstraction through this chip. Do some quick reading on JPEG standard to explain design decisions, particularly at system level.