CSCE 5730: Digital CMOS VLSI Design

Assignment # 4, Total Marks = 5*20 = 100.
Assigned Date: 3rd Nov 2008 (Mon), Due Date: 12th Nov 2008 (Wed)
Instructor: Dr. Saraju P. Mohanty

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1. Design a 4:1 mux using transmission gates and simulate it using LTspice.
2. Design a D flip-slop using transmission gates and simulate using LTspice.
3. Simulate the above flip-flop for non-overlapping clocks using LTspice.
4. Using NMOS models produce its current-voltage characteristics. Use a spreadsheet or MATLAB for the purpose. Assume the parameters from any text book.