CSCE 5730: Digital CMOS VLSI Design

Assignment # 3, Total Marks = (5x20) = 100.
Assigned Date: 15th Oct 2008 (Wednesday), Due Date: 22nd Oct 2008 (Wednesday)
Instructor: Dr. Saraju P. Mohanty

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1. Using microwind tool perform layout design of the following 5 logic gates. Perform their simulations to verify the truth tables.
    (1) Inverter
    (2) NAND
    (3) NOR
    (4) AND
    (5) OR