



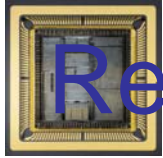
Lecture 8: Static CMOS Logic

CSCE 6651

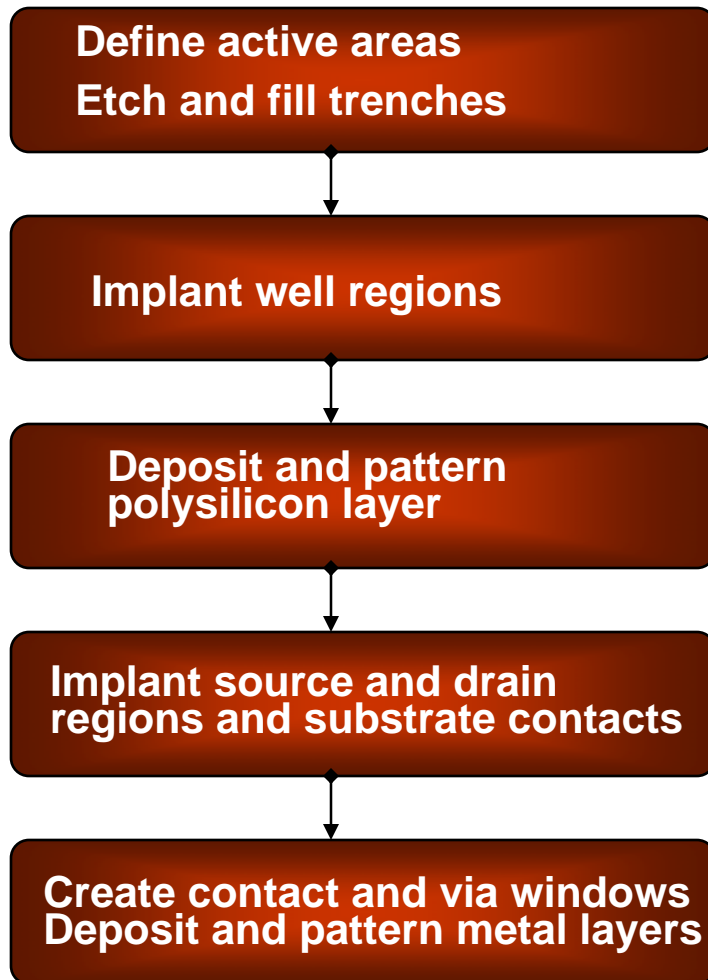
Advanced VLSI Systems

Instructor: Saraju P. Mohanty, Ph. D.

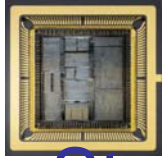
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Review: CMOS Process at a Glance



- One full photolithography sequence per layer (mask)
 - Built (roughly) from the bottom up
 - 1 tubs (aka wells, active areas)
 - 2 polysilicon
 - 3 source and drain diffusions
 - 4 metal
- exception!



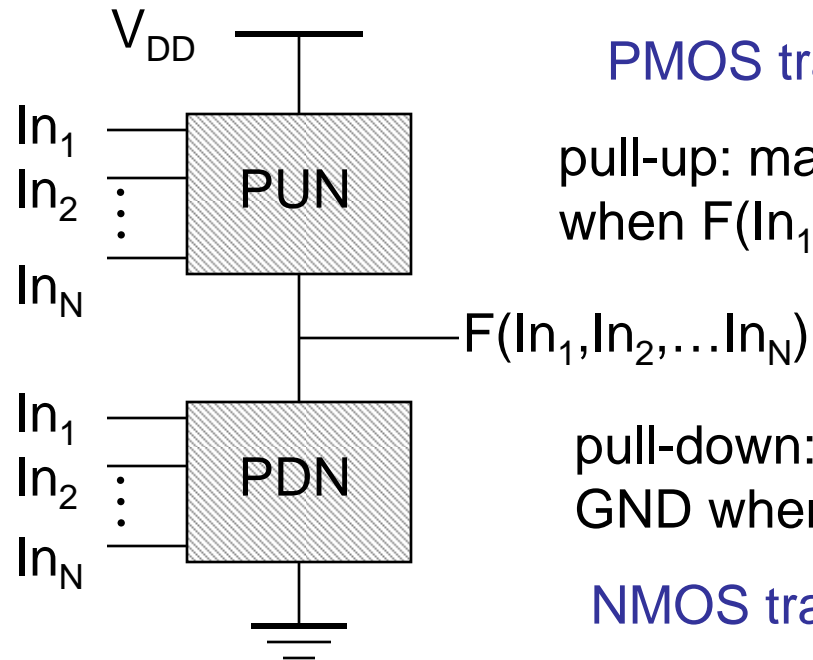
CMOS Circuit Styles

- **Static complementary CMOS** - except during switching, output connected to either V_{DD} or GND via a low-resistance path
 - high noise margins
 - full rail to rail swing
 - V_{OH} and V_{OL} are at V_{DD} and GND, respectively
 - low output impedance, high input impedance
 - no steady state path between V_{DD} and GND (**no** static power consumption)
 - delay a function of load capacitance and transistor resistance
 - comparable rise and fall times (under the appropriate transistor sizing conditions)
- **Dynamic CMOS** - relies on temporary storage of signal values on the capacitance of high-impedance circuit nodes
 - simpler, faster gates
 - increased sensitivity to noise



Static Complementary CMOS

- Pull-up network (PUN) and pull-down network (PDN)



PMOS transistors only

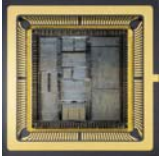
pull-up: make a connection from V_{DD} to F when $F(In_1, In_2, \dots, In_N) = 1$

pull-down: make a connection from F to GND when $F(In_1, In_2, \dots, In_N) = 0$

NMOS transistors only

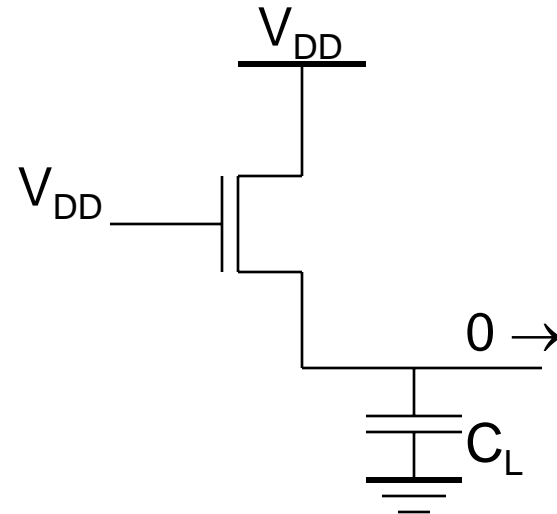
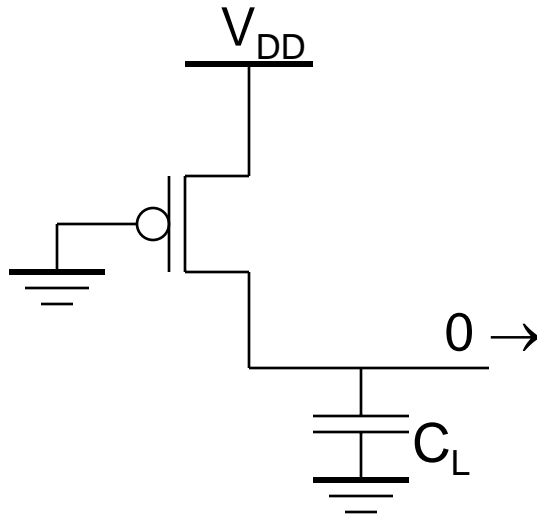
PUN and PDN are **dual** logic networks

One and only one of the networks (PUN or PDN) is conducting in steady state (output node is always a low-impedance node in steady state)

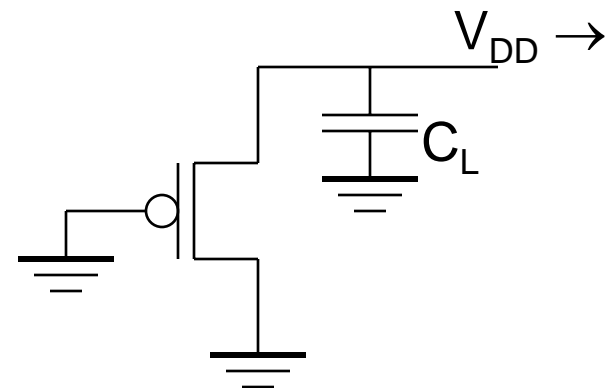
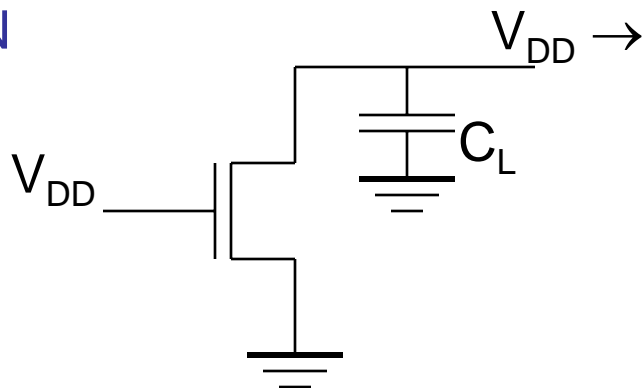


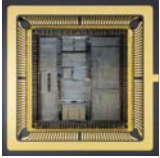
Threshold Drops

PUN

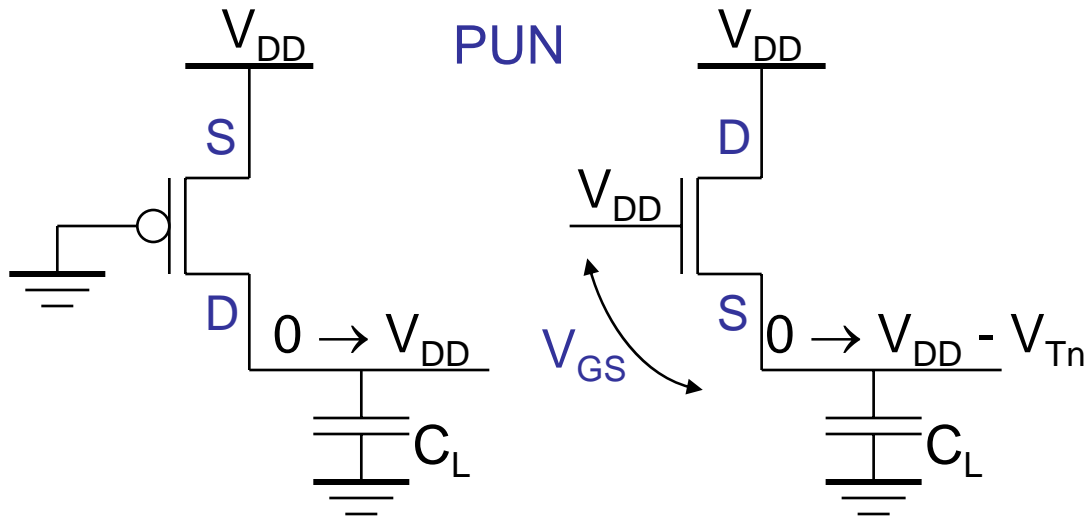


PDN



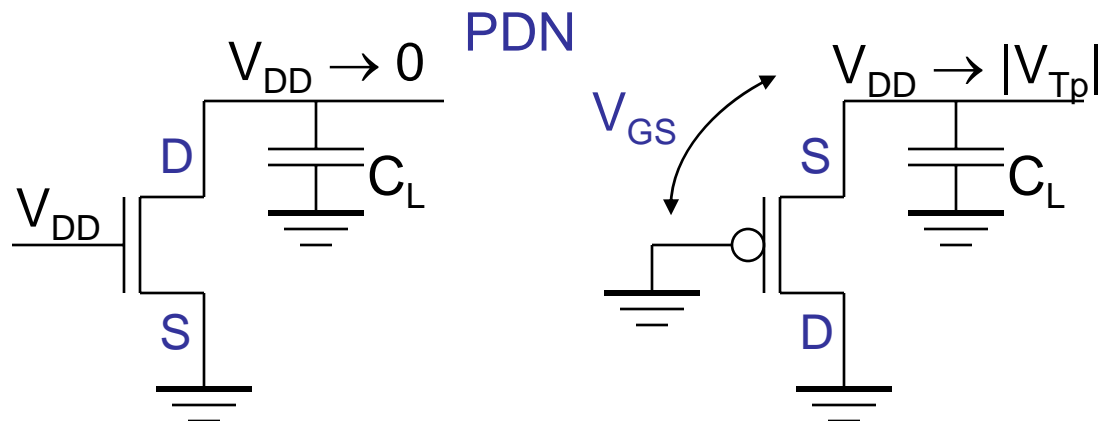


Threshold Drops



Why PMOS in PUN and NMOS in PDN ... threshold drop

NMOS produce strong zeros; PMOS generate strong ones

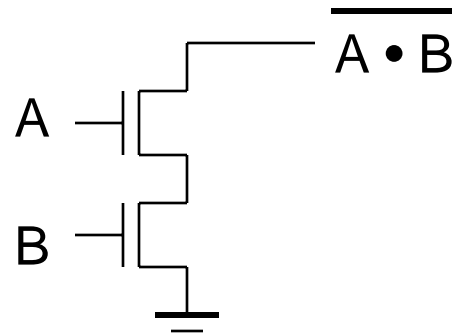


Two circuits on the right cut-off before the ideal voltage level is reached (when $V_{GS} < V_T$)

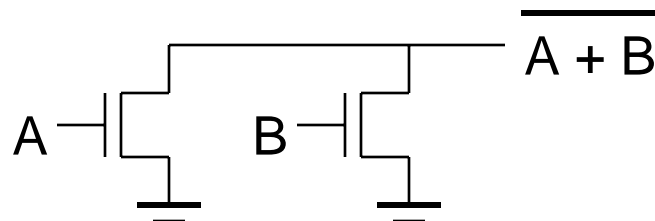


Construction of PDN

- NMOS devices in **series** implement a NAND function



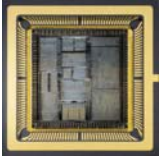
- NMOS devices in **parallel** implement a NOR function



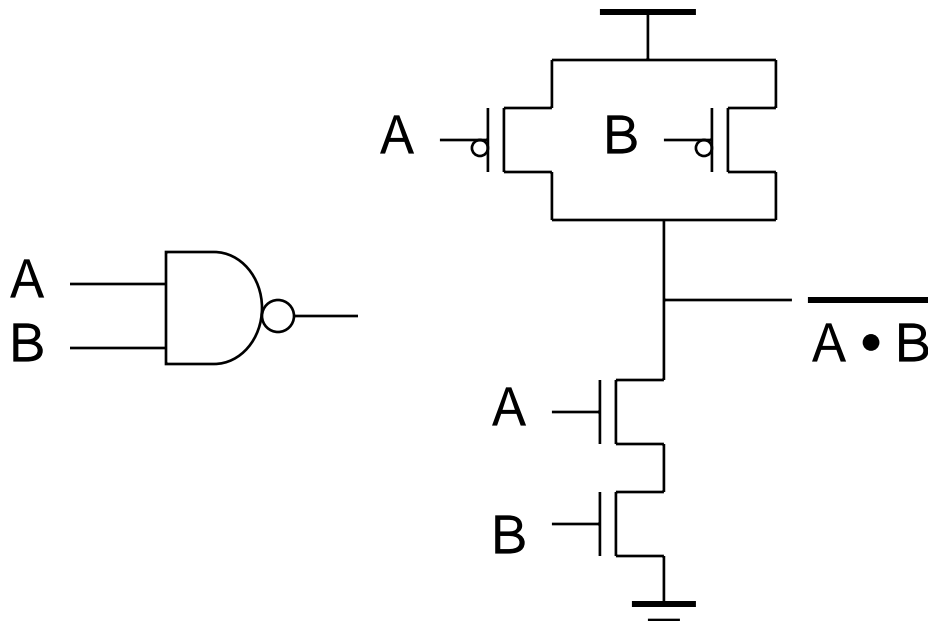


Dual PUN and PDN

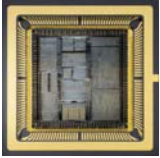
- PUN and PDN are dual networks
 - DeMorgan's theorems
$$\overline{A + B} = \overline{A} \cdot \overline{B} \quad [!(A + B) = !A \cdot !B \text{ or } !(A | B) = !A \& !B]$$
$$\overline{A \cdot B} = \overline{A} + \overline{B} \quad [!(A \cdot B) = !A + !B \text{ or } !(A \& B) = !A | !B]$$
 - a **parallel** connection of transistors in the PUN corresponds to a **series** connection of the PDN
- Complementary gate is naturally **inverting** (NAND, NOR, AOI, OAI)
- Number of transistors for an N-input logic gate is **2N**



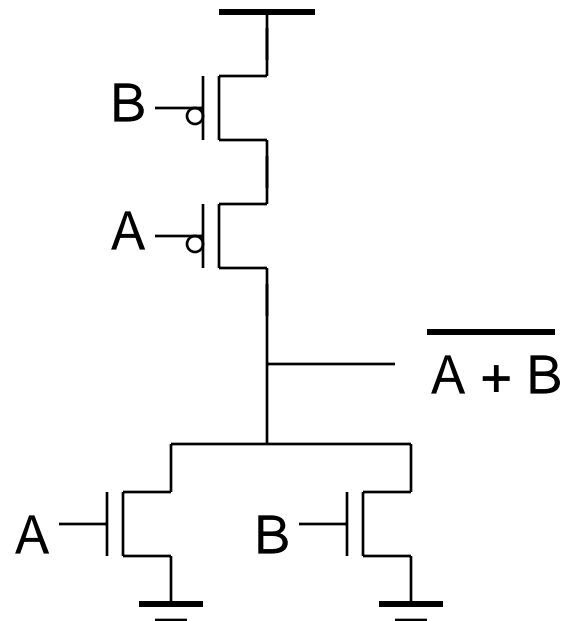
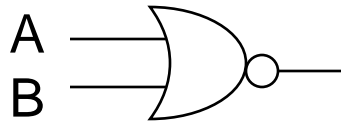
CMOS NAND



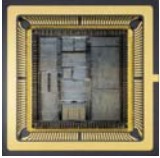
A	B	F
0	0	1
0	1	1
1	0	1
1	1	0



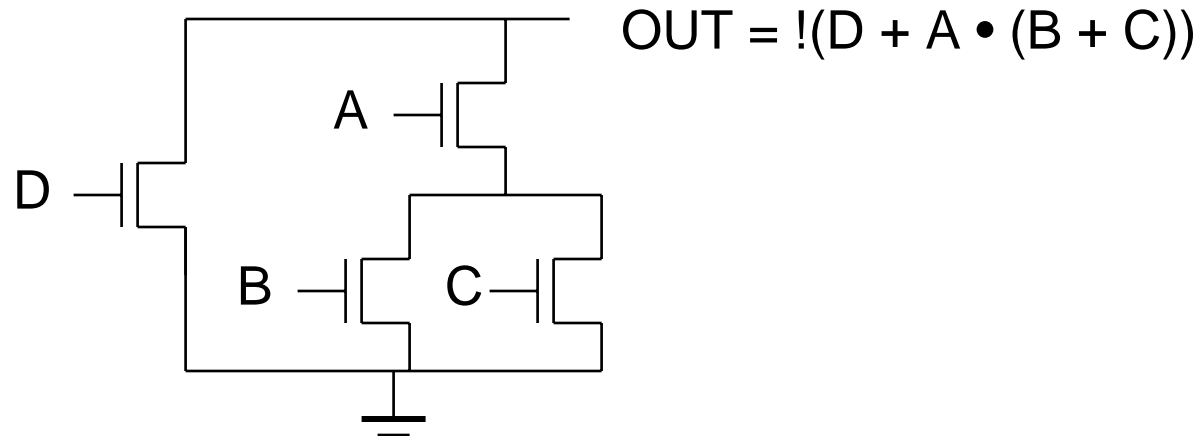
CMOS NOR



A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

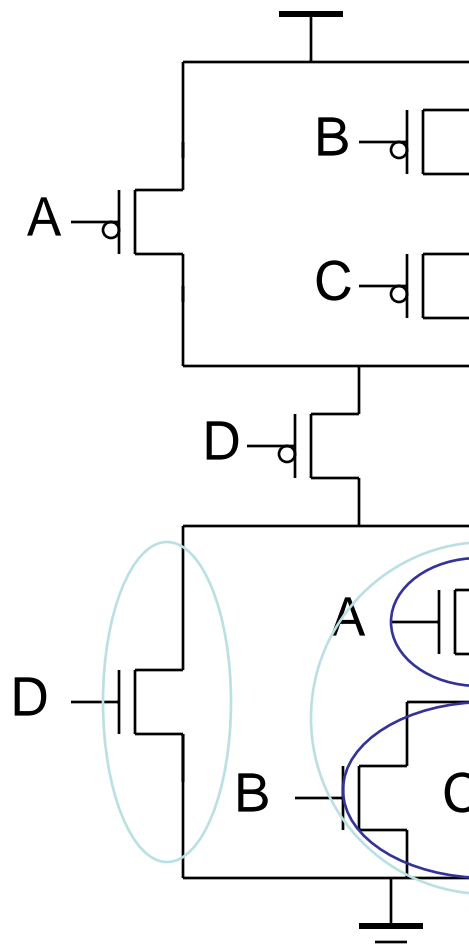


Complex CMOS Gate





Complex CMOS Gate



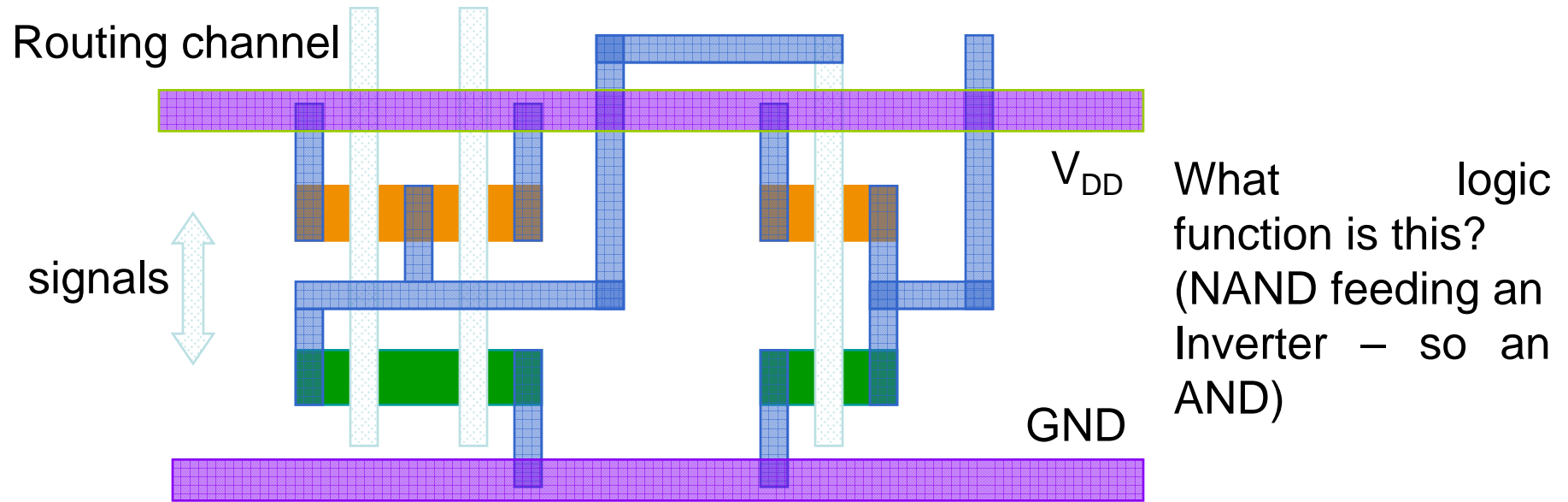
Shown synthesis of pull up from
pull down structure

Max of 3 transistors in series (in
the PUN)

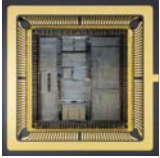
$$\text{OUT} = \neg(D + A \cdot (B + C))$$



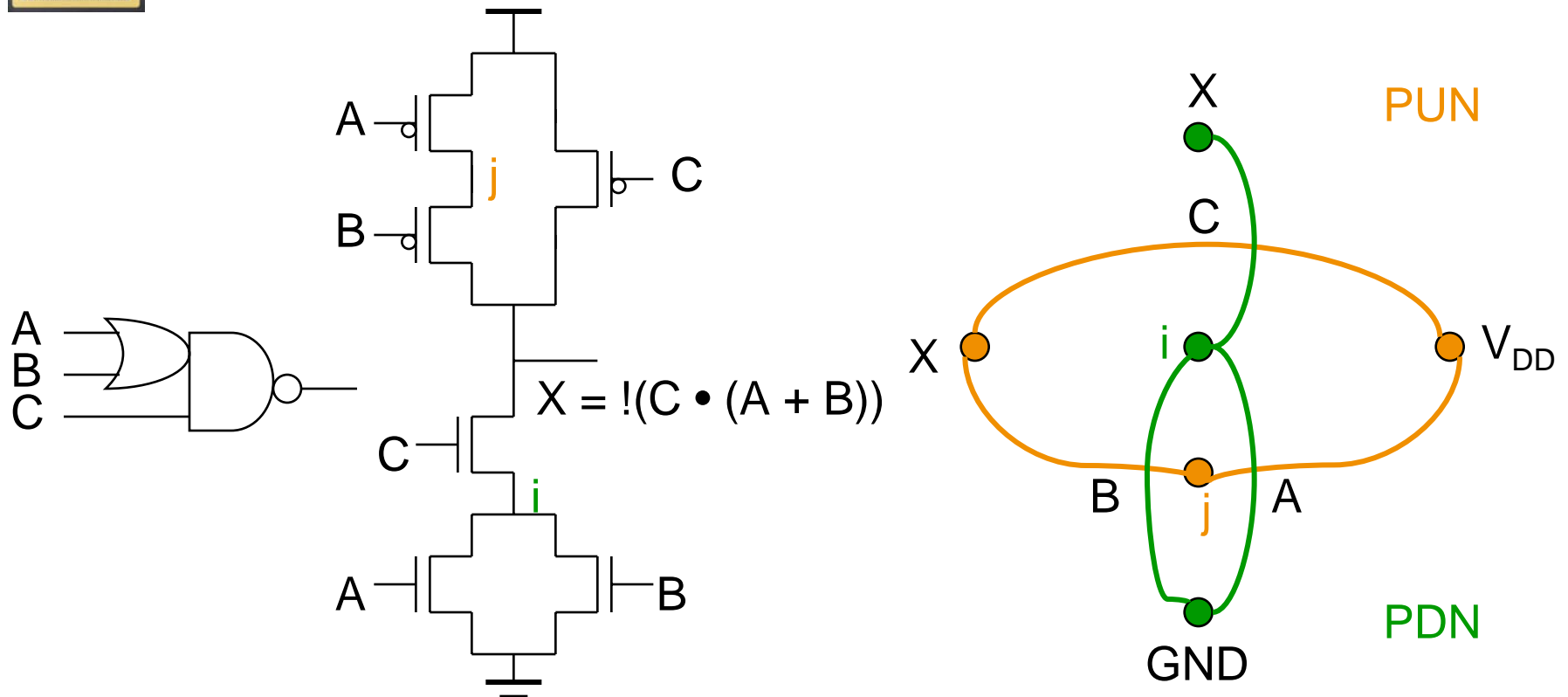
Standard Cell Layout Methodology



- Route V_{DD} and GND horizontally, Route signals in poly perpendicular to V_{DD} and GND (vertically) – poly can serve as input to NMOS and PMOS
- Order inputs (consistent Euler path) to optimize the horizontal connectivity of diff strips want unbroken row of devices with abutting source/drain connections – so there is only one strip of diffusion in both wells
- Place diffs in horizontal strips, Interconnect appropriately
- Interconnect between cells are done in “routing channels”
- Contacts and wells not shown.



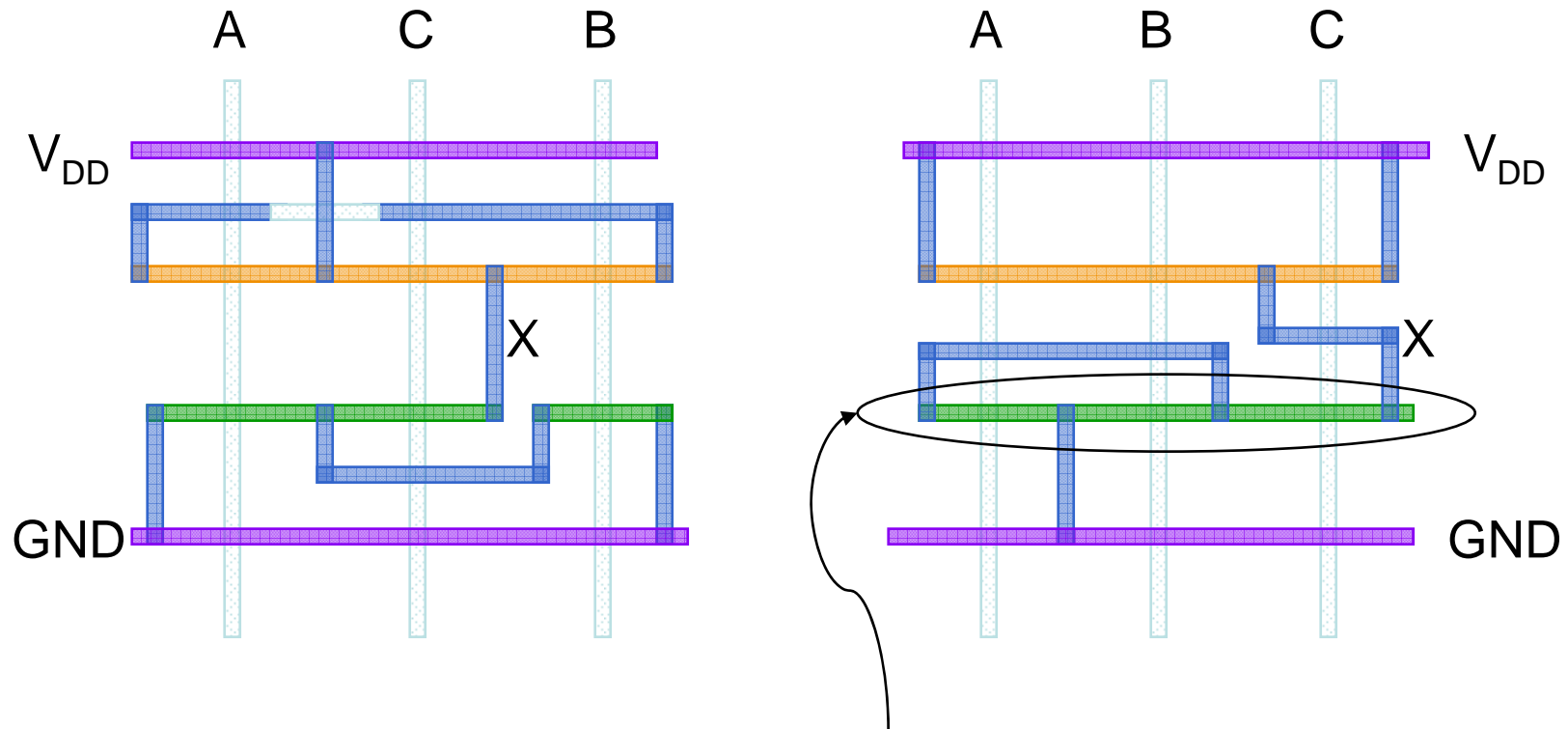
OAI21 Logic Graph



- Systematic approach to derive order of input signal wires so gate can be laid out to minimize area
- PUN and PDN are duals (parallel <-> series), Vertices are nodes (signals) of circuit, VDD, X, GND and edges are transitions

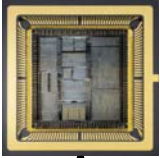


Two Stick Layouts of $!(C \bullet (A + B))$



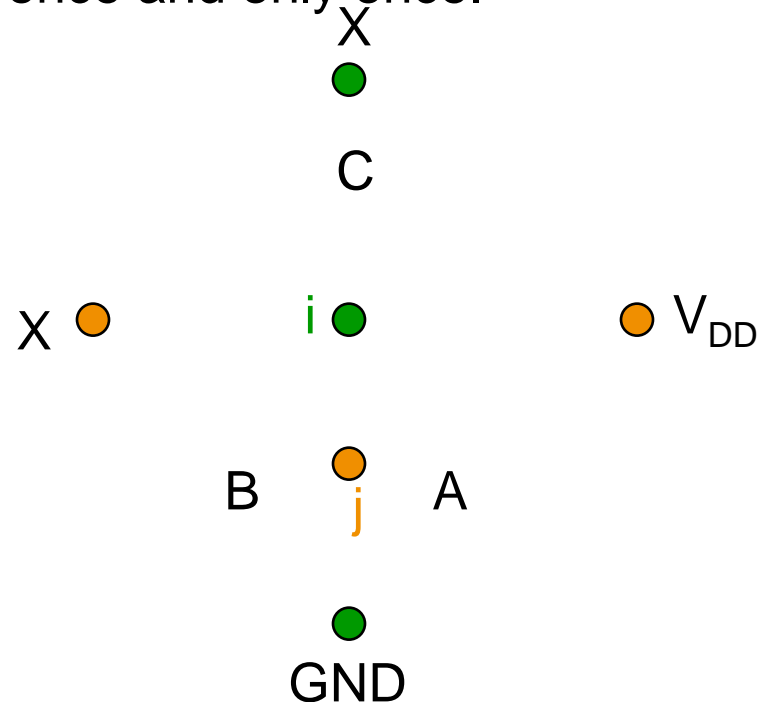
uninterrupted diffusion strip

- Line of diffusion layout – abutting source-drain connections
- Crossover of left layout eliminated by A B C ordering

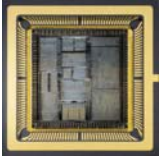


Consistent Euler Path

- An uninterrupted diffusion strip is possible only if there exists a Euler path in the logic graph
 - Euler path: a path through all nodes in the graph such that each edge is visited once and only once.

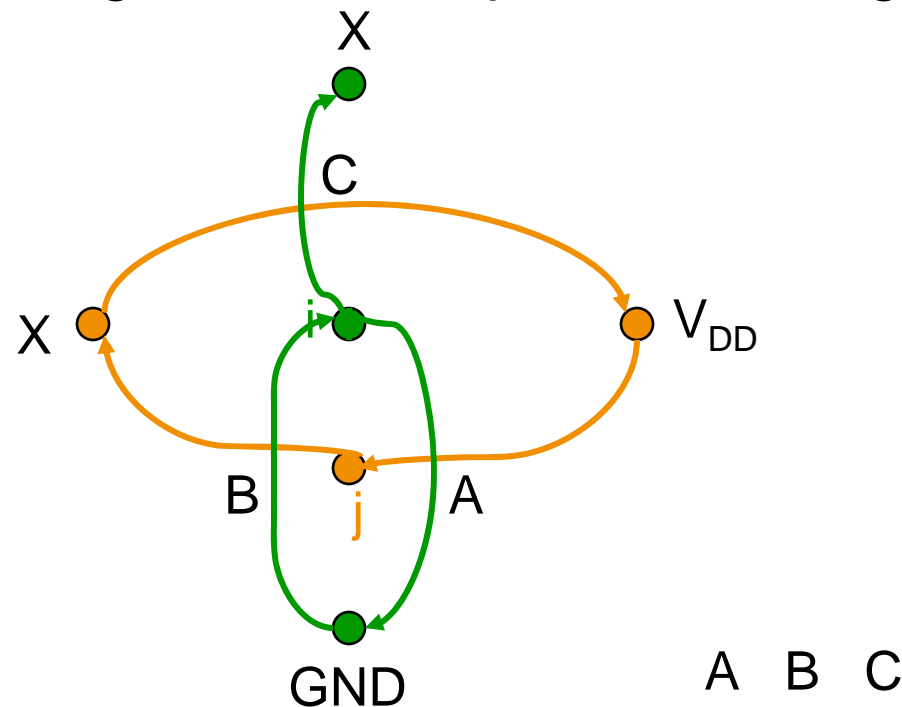


- For a single poly strip for every input signal, the Euler paths in the PUN and PDN must be **consistent** (the same)

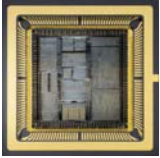


Consistent Euler Path

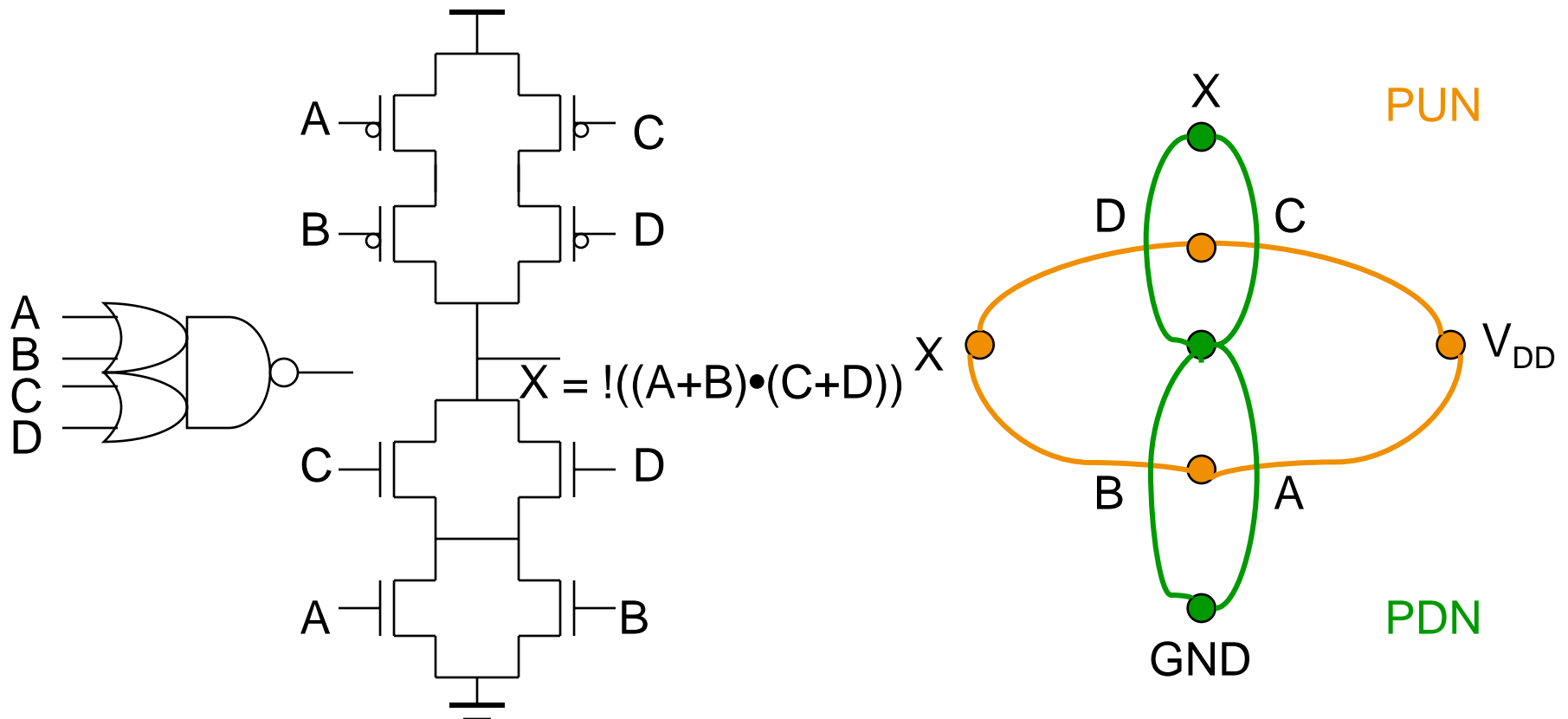
- A path through all nodes in the graph such that each edge is visited once and only once.
- The sequence of signals on the path is the signal ordering for the inputs.



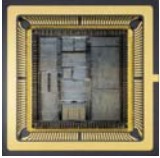
If you can define a Euler path then you can generate a layout with no diffusion breaks: A B C, C A B, B C A → no PDN
 B A C, A C B → no PDN, C B A



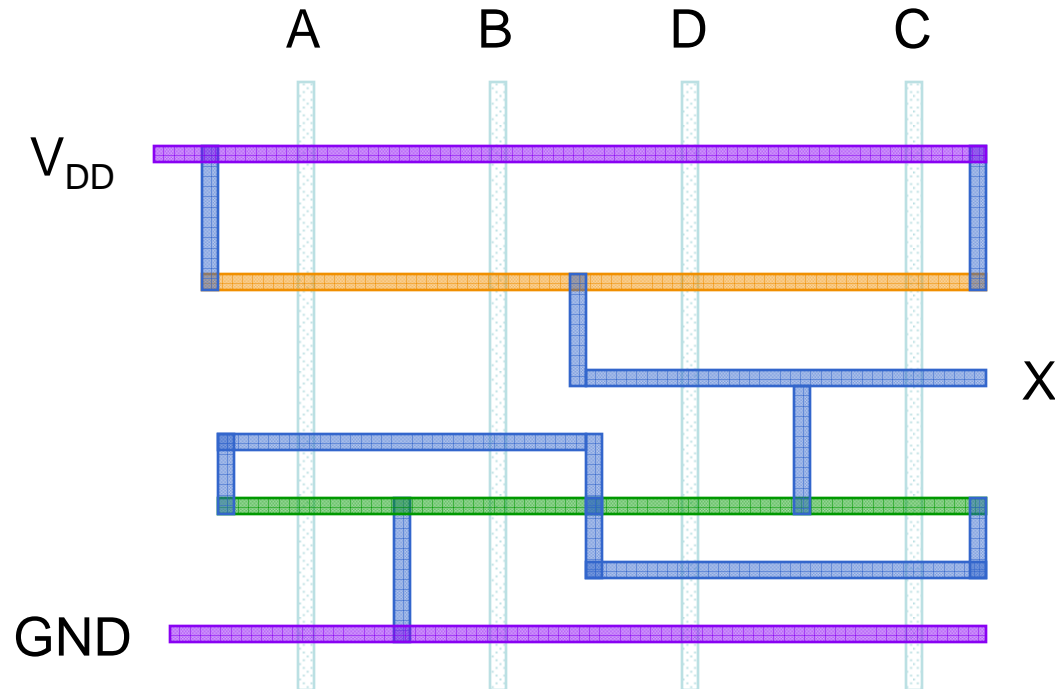
OAI22 Logic Graph



Consistent Euler paths: ABDC, BDCA, DCAB, CABD, BACD, ACDB, CDBA, DBAC, and NOT DACB, BCAD, etc.



OAI22 Layout

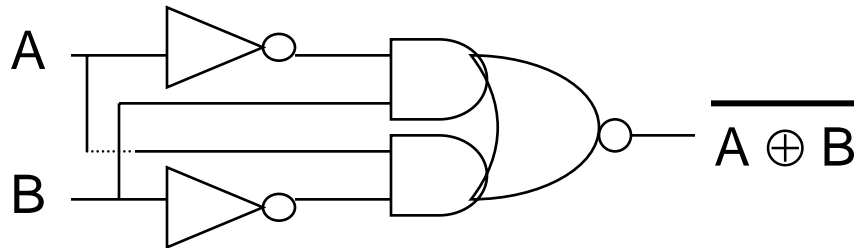


- Some functions have no consistent Euler path like $x = \neg(a + bc + de)$ (but $x = \neg(bc + a + de)$ does!)

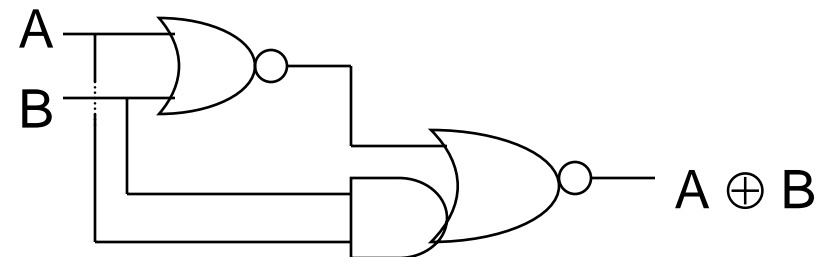
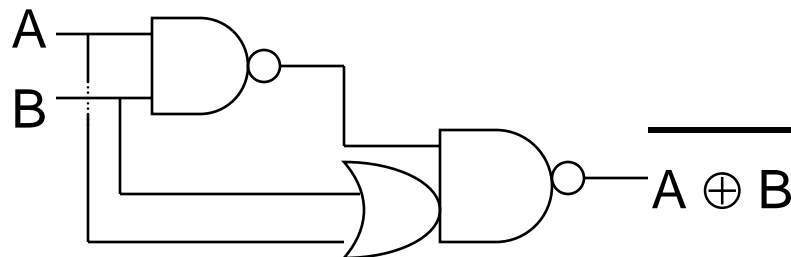
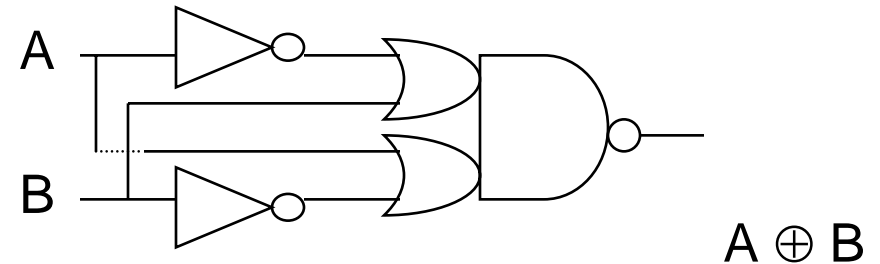


XNOR/XOR Implementation

XNOR



XOR

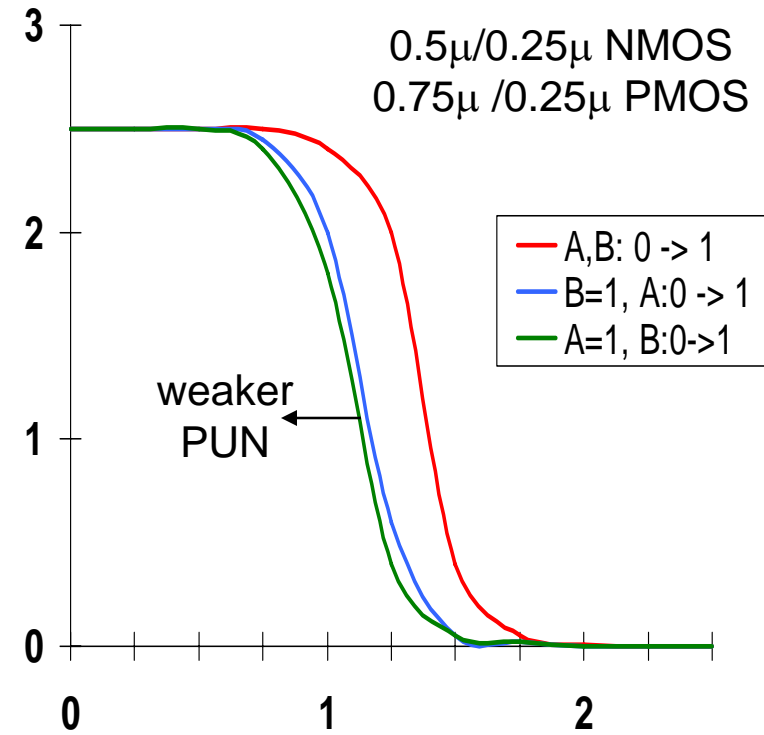
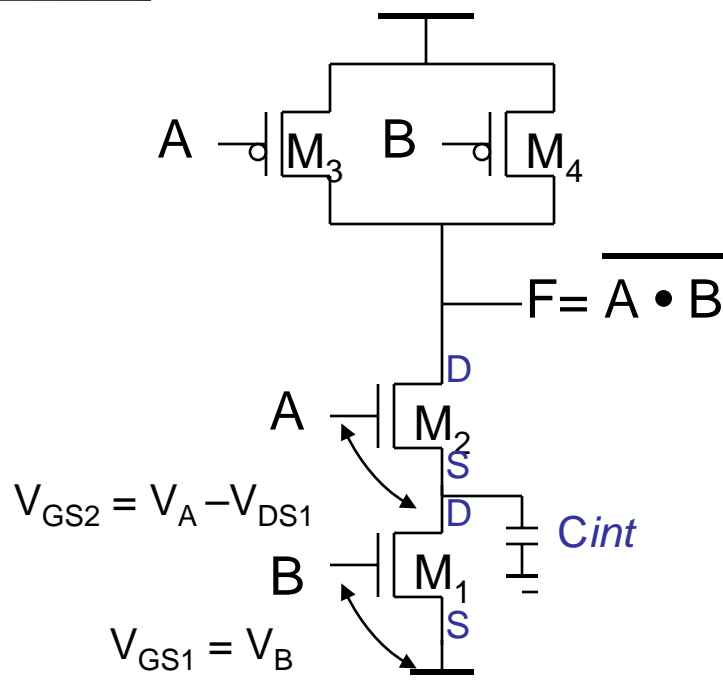


- ❑ How many transistors in each?
- ❑ Can you create the stick transistor layout for the lower left circuit?

12 and 10 transistor implementations of static XOR circuit.



VTC is Data-Dependent



- The threshold voltage of M_2 is higher than M_1 due to the body effect (γ)

$$V_{Tn1} = V_{Tn0}$$

$$V_{Tn2} = V_{Tn0} + \gamma(\sqrt{(|2\phi_F| + V_{int})} - \sqrt{|2\phi_F|})$$

since V_{SB} of M_2 is not zero (when $V_B = 0$) due to the presence of C_{int}

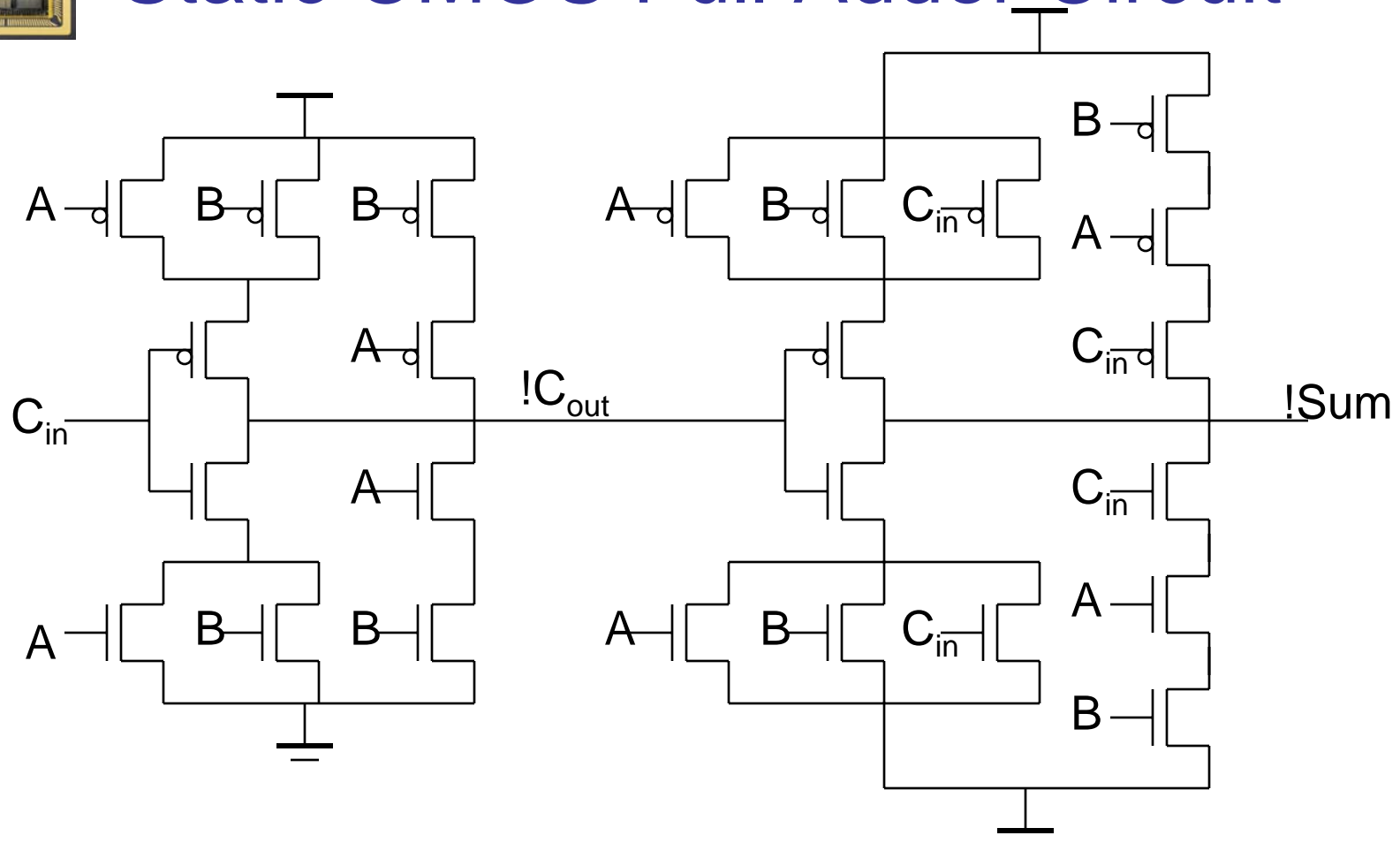


VTC is Data-Dependent

- VTC characteristics are dependent upon the data input patterns applied to the gate (so also the noise margins!)
- Threshold voltage of M2 will be higher than transistor M1 due to body effect
- Case 1 – both transistors in the PUN are on simultaneously for $A=B=0$, representing a strong pull-up. In the other two cases only one of the pull-up devices is on. So the VTC is shifted left as a result of the weaker PUN for the second and third cases.
- Case 2 – see Case 3, small difference can be attributed to the body effect of M2 and the drive voltage
- Case 3 – M2 as resistor in series with M1, so only small effect on VTC; since pulldown is strong and pullup weaker than case 1, VTC shifted to the left (also have to discharge both CL (on the output) and Cint (possibly) thru M1 so will also be slower!)



Static CMOS Full Adder Circuit



24 + 4 (for C and Sum inverter) transistor Full Adder

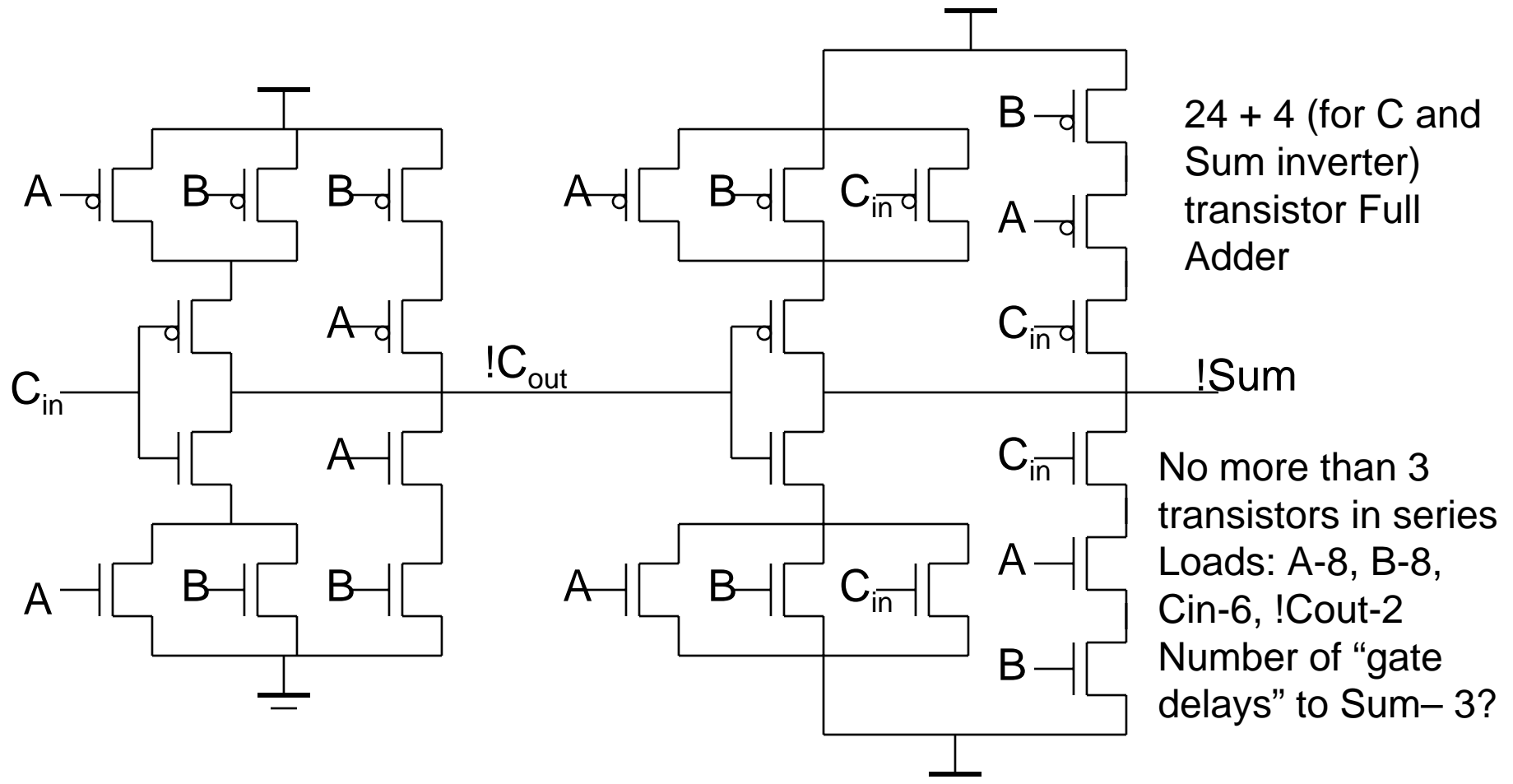
No more than 3 transistors in series

Loads: A-8, B-8, Cin-6, !Cout-2, Number of “gate delays” to Sum – 3?



Static CMOS Full Adder Circuit

$$\overline{C_{out}} = \overline{C_{in}} \& (\overline{A} \mid \overline{B}) \mid (\overline{A} \& \overline{B}) \quad \overline{Sum} = C_{out} \& (\overline{A} \mid \overline{B} \mid \overline{C_{in}}) \mid (\overline{A} \& \overline{B} \& \overline{C_{in}})$$



$$C_{out} = C_{in} \& (A \mid B) \mid (A \& B)$$

$$Sum = \overline{C_{out}} \& (A \mid B \mid C_{in}) \mid (A \& B \& C_{in})$$