Intel Pentium Processor

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Disclaimer: I do not claim any originality for this work. This is basically a review of different works/materials/papers related to computer architecture, specifically Intel Pentium Architecture. This work has been done for partial fulfillment of course work.

Abstract

Human requirements are unlimited. Human beings want to achieve those unlimited requirements in a limited time. As a consequence, they want to do all works as fast as possible with highest degree of reliability. This in turn requires some sort of automation (i.e. work with less human intervention). Computer is the major thing needed for this automation process. The computer had played a major role for revolution of civilization. We find the use of computers in all aspects of our day-to-day life. Various significant applications of computer being ATM, Laptop, Palmtop, World Wide Web, e-mail, e-commerce, and so on. The real entity that does all the work in the computer is the microprocessor. The computers have undergone generations after generations with the growth various electronic devices and software as well. There are various different computers and microprocessor developed by different manufacturers. Intel is one of the leading manufacturers. This work gives overall study of various microprocessors developed by Intel. More detailed study of Pentium processor is done. Various hardware and software aspects of the Pentium processor are studied in detail.

Key Word

Abacus, ENIAC, vacuum tubes, transistors, MHz/GHz, clone, embedded processors, coprocessor, Superscalar, CISC, RISC, cache, MMX, 2^{nd}-level (L2) cache, SISD, SIMD, processor serial ID (chip ID), VLIW, EPIC, superscalar factor, pipeline depth, micro-ops, branch prediction, instruction set

1. Introduction

The computing history starts well back from 3000 BC with the invention of *abacus* in Babylonia and consequently with the use of algorithms to solve numerical problems in 1800 BC. With the rapid development of civilization and consequent increase in the demand for faster and correct calculations human beings have tried to develop various computing machines that can meet their requirements. The different forms computing machines developed are slide rules, mechanical calculators, analytical machines and so on. In 1890, electromechanical calculator was used in US census. In 1940 Complex Numerical Calculator (the first Digital Computer) was demonstrated in Bell Labs. The first general purpose computer called "Electronic Numerical Integrator and Computer" (*ENIAC)* was made in 1946 and (unfortunately) used extensively in World War II. With the invention of *vacuum tubes* in 1951 there was few rapid development in computer designs. The modern computer age really started with invention of *transistors* in 1959 in the Bell Lab. After that the computers have undergone rapid changes in speed, size and other features what even might have never been imagined by the great pioneers of the computers. The computers size has changed from the dimensions of square feet as big as a bedroom to the size of palm. The present age is of the age of microcomputers leaving behind the mainframes and the minicomputers, etc.

The five components of a computer are :

- input,
- output
- memory
- datapath and
- control.

The processor is the combination of last two i.e. datapath and control. People call this processor as the CPU stands for “Central Processing Unit”. The “microprocessor” means the CPU on a single chip. Of course, with the development of more modern designs this terminology has become more or less fuzzy.

The microprocessor is the most active part of the computer. This consists of datapath and control. The datapath performs the arithmetic operations and the control tells the datapath, memory, and I/O devices what to do according to the instructions of the program. The hardware is made to perform the desired task with the help of software. Both hardware and software consists of different layers or abstractions. That helps the hardware as well as software designers to cope with the complexity of the computer systems. The key interface between level of abstraction is the *instruction set architecture*, (or architecture), of a computer. The instruction set architecture includes anything programmers need to know to make the binary machine language work correctly. Thus computer architecture can be defined as the attributes of a computer as visible to the programmer or those attributes that affect the execution of the program.

The first microprocessor was built in 1971 known as Intel 4004. This had only 2300 transistors. The first commercially available microprocessor is Intel 8086 in 1979. Microprocessor has undergone rapid changes now we are going to have computers with 1 GHz microprocessors having millions of transistors packed in it, thanks to VLSI technology. The speed of the microprocessors is governed by the well-known Moore’s Law, which states that the processor speed doubles every 18 months.

There are various microprocessor giants who have played important roles for this fastest growth of the compute industry, to name a few Motorola, Intel, and so on. The Intel Inc. is considered as the most successful commercially available microprocessor company.

In this work, extensive survey of Intel Pentium is done. Pentium is the most popular processor family developed by Intel. The work consists of various sections. One section is fully dedicated to the history of the microprocessors developed by Intel. The next section deals with hardware related issues of the Pentium processors. Then the work talks about the instruction set architecture of the Pentium processors. A special section is dedicated to the Pentium III processors, the fastest commercially available microprocessor till date.

2. Various Intel Processors

Intel invented the first microprocessor in the 1971, the Intel 4004, It had only 2300 transistors. Thus starting the microcomputer revolution. It was a 4-bit microprocessor. The 8021, 8022, 8041, 8048 all were Intel's 8-bit microcomputer chips. These had around 8-10 registers each. Then Intel developed 8080A and 8085A 8-bit microprocessors.

In the year 1979 Intel developed 8086/8088 16-bit microprocessors (8088 had 8-bit data bus). Both had 20-bit address line, had speeds ranging from 4-16 MHz. NEC cloned these to V20-V30 designs.

The revolution of Intel continued with the introduction of 80186 and 80188. Unfortunately, this chip didn't catch on with many hardware manufacturers;. however, this chip has enjoyed a tremendous success in the world of embedded processors. The speed of the chips was in the range 6-40 MHz.

Intel introduced the 80286 microprocessor in 1982. This had 24 address lines, thus16MB of addressibility. The speeds ranged from 6-25 MHz.

In 1985, Intel introduced the 80386 (renamed to 80386 DX). It was a 32-bit microprocessor with 4GB addressibility. Intel introduced 80386 SX shortly after 80386. This had 16-bit data bus & 24-bit address bus. Intel introduced the concept of a cache. Then came 80386SL microprocessor integrated with core logic, chipset functionality, and power saving features. The speed of all these microprocessors ranged from 16-40 MHz.

The last Intel microprocessor with x86 nomenclature was the 80486. This was also a 32-bit microprocessor with clock speed of 50-75 MHz. This is the first chip to contain one million of transistors. The Intel marketed this microprocessor in various forms. The 80486 DX was the cost-reduced version of 80486, the 80486 SX had both data and address bus compatibility with its DX counterpart, the "math coprocessor" of this being the 80487 SX. The 80486SL was the low power version one. Then the 80486 DX2 and DX4 were introduced which had clock speed of 2-3 times than the original 80486.

The introduction of Pentium in 1993 brought the end of its x86 nomenclature. This chip contains around 3 million transistors in it. The speeds varied from 90-133 MHz , of course the original product ran at 60-66 MHz. The Pentium was a *Superscalar* processor. The Pentium processor still has CISC architecture, but the high performance is achieved by using many if the organizational features of RISC architecture.

Then came the Pentium Pro processor in 1995. It had speeds in the range 100-200 MHz. It had a large 2^{nd}-level (L2) cache to make the processor faster, but dynamic branch prediction was implemented here as in the case of original Pentium. The 2^{nd} level cache increased the cost of the machine to a greater extent.
The Pentium II is an extension of Pentium Pro with MMX (multimedia Extension) for modern multimedia applications. The package of Pentium II (called slot1) is different

from Pentium Pro. The speed with a full speed 2nd level cache is claimed to be around 400 MHz. It can address up to 64 GB of main memory, but has a cache limitations preventing memory use above 512 MB.

Then Intel introduced the Celeron. This is a Pentium II MMX but without the 2nd level cache. The aim of Intel was to make available cheaper processors, at the cost of reduced speed.

The Xeon is a Pentium II processor with a ½ speed 2nd level cache. Xeon is not slot compatible with Pentium II, instead uses a slot named Slot-2. Price of Xeon is higher than Celeron or Pentium II.

The fastest Intel processor available till date is Pentium III processor. This is available up to speed of 1.0GHz. This is manufactured with Intel's new 0.18-micron technology, resulting better performance. This has got two more new features. First of all this is a SIMD (Single Instruction and Multiple Data) machine unlike its predecessors which were SISD (Single Instruction Single Data) machines. The other significant feature in Pentium III is that each processor has unique processor serial ID (or chip ID) to enhance manageability and asset tracking.

Merced is going to be the future generation processor of Intel with speed ranging from 600-1000 MHz. It is not going to have CISC architecture rather it will have RISC architecture. It will have all features VLIW (Very Long Instruction Formats) design termed as EPIC (Explicitly Parallel Instruction Computing).

Table 1. Summary of different Intel processors

SL	μ P Name	Bus Bits	MHz	Special Features
1	4004	4	-	2300 transistors, 1st μ P
2	802x, 804x	8	-	μ Computers, 8-10 registers
3	8080A/8085A	8	-	-
4	8086/8088	16	4-16	Cloning started
5	80186 and 80188	-	6-40	Fault tolerance, DMA controller
6	80286	24	6-25	Protected mode
7	80386	32	16-40	Cache introduced
8	80486	32	50-75	1 million transistors, math processor
9	Pentium	32	90-133	3 million transistors, superscalar
10	Pentium Pro	32	100-200	L2 cache
11	Pentium II	32	400	MMX, Slot-1
12	Celeron	32	-	No L2 cache, cheaper
13	Xeon	32	-	½ speed L2 cache, Slot-2
14	Pentium III	32	1000	SIMD, chip ID, 0.18 μ tech
15	Merced	-	1000	VLIW, RISC

3. Details of the Pentium Pro Microarchitecture

The Pentium Pro has advanced superscalar, pipelined architecture manufactured using 0.6µ technology. The *superscalar factor* (the maximum number of instructions that can be completed in a clock cycle) is three in the Pentium Pro processor, compared to two in Pentium processor. To handle the instruction throughput properly the processor uses a decoupled, 12-stage superpipeline. Pipeline depth in the multiple execution units is twelve, compared to five in Pentium, and the datapath width inside the processor is 64-bits, double that of the Pentium. Dynamic branch prediction is implemented in Pentium Pro that is similar to the Pentium processor. Fig.1 shows functional block diagram of the Pentium Pro processor microarchitecture.

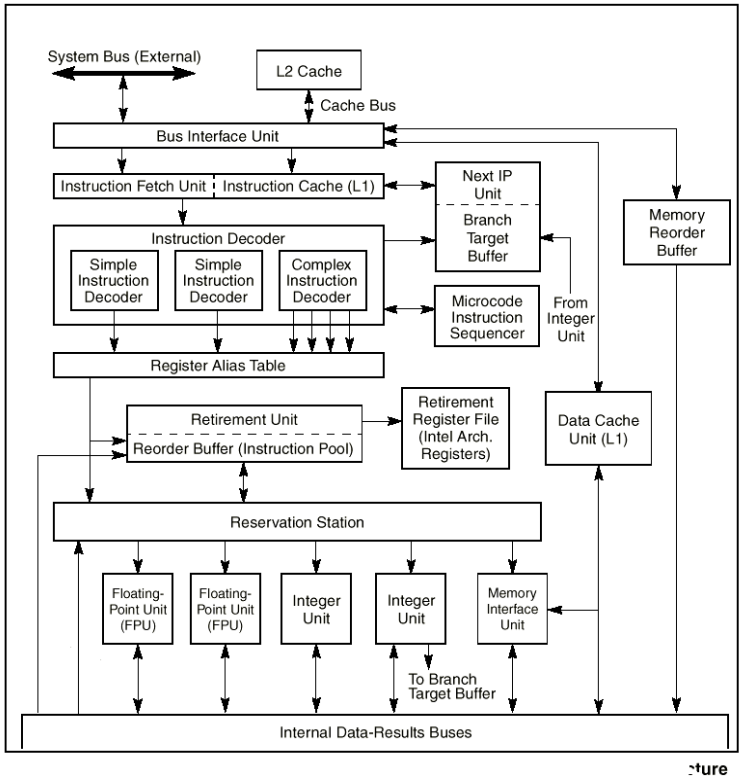

Figure 1: Functional block diagram of Pentium Pro processor

Referring to the above diagram, we can divide the architecture into four processing units and the memory subsystem as follows:

- Memory subsystem: This consists of, system bus, L2 cache, bus interface unit, instruction cache (L1), data cache unit (L1), memory interface unit, and memory reorder buffer.
- Fetch/Decode unit: This unit comprises of instruction fetch unit, branch target buffer, instruction decoder, microcode sequencer, and register alias table.
- Instruction pool: This is made up of the reorder buffer

- Dispatch/Execute unit: This has a reservation station, two integer units, two floating-point units, and two address generation units.
- Retire unit: This consists of the retire unit and retirement register file.

These processing units are discussed in little more detail in the following subsections.

Memory Subsystem

The memory subsystem for the Pentium Pro processor consists of main system memory, the primary cache (L1), and the secondary cache (L2). The bus interface unit accesses system memory through the external system bus. The external system bus is a 64-bit bus that handles each bus access as separate request and response operations (transaction-oriented bus). While the bus interface unit is waiting for a response to one bus request, it can issue numerous additional requests. The bus interface unit accesses the L2 cache through a 64-bit cache bus. This bus is also transactional oriented, supporting up to four concurrent cache accesses, and operates at the full clock speed of the processor. Bus interface unit gets access to the L1 caches is through internal buses. The L1 cache also operates at full clock speed. The 8-KByte L1 instruction cache is four-way set associative whereas the 8-KByte L1 data cache is two-way set associative, and dual-ported supporting one load and one store operation per cycle. Coherency between the caches and system memory are maintained using the MESI (modified, exclusive, shared, invalid) cache protocol. Processor's execution units request memory through the memory interface unit and the memory order buffer. These units have been designed to support a smooth flow of memory access requests through the cache and system memory hierarchy to prevent memory access blocking. The L1 data cache automatically forwards a cache miss on to the L2 cache. Memory requests to the L2 cache or system memory go through the memory reorder buffer. The memory reorder buffer functions as a scheduling and dispatch station. This unit keeps track of all memory requests and is able to reorder some requests to prevent blocks and improve throughput.

The Fetch/Decode Unit

The fetch/decode unit reads instructions from the L1 instruction cache and decodes them into a series of micro-operations (micro-ops). This micro-op stream is then sent to the instruction pool. From the instruction cache the instruction fetch unit fetches one 32-byte cache line per clock. It marks the beginning and end of the instructions in the cache lines and transmits 16 aligned bytes to the decoder. Basing on inputs from the branch target buffer, the interrupt status, and branch prediction indications the instruction fetch unit computes the instruction pointer. The branch target buffer performs the branch prediction (branch prediction means that the microprocessor tries to predict whether the branch instruction will jump or not, based on a past history of the branch). The 512 entry branch target buffer looks many instructions ahead of the retirement program counter. It is done using Yeh's algorithm. The instruction decoder contains three parallel decoders:

- two simple-instruction decoders and
- one complex instruction decoder.

Each decoder converts an instruction into one or more triadic micro-ops (two logical sources and one logical destination per micro-op). Micro-ops are primitive instructions that are executed by the processor's six parallel execution units. Many instructions are converted directly into single micro-ops by the simple instruction decoders, and some instructions are decoded into from one to four micro-ops. The more complex instructions are decoded into sequences of preprogrammed micro-ops obtained from the microcode instruction sequencer. The decoding of instruction prefixes and looping operations are handled by instruction decoders. The instruction decoder can generate up to six micro-ops per clock cycle. The processor provides 40 internal, general-purpose registers, which are used for the actual computations. These registers can handle both integer and floating-point values. The enqueued micro-ops from the instruction decoder are sent to the register alias table unit, where references to the logical architecture registers are converted into internal physical register references. Then the allocator in the register alias table unit adds status bits and flags to the micro-ops to prepare them for out-of-order execution and sends the resulting micro-ops to the instruction pool.

Instruction Pool (Reorder Buffer)

The reorder buffer is an array of content-addressable memory, arranged into 40 micro-op registers. It contains micro-ops that are waiting to be executed, as well as those that have already been executed but not yet committed to machine state. The dispatch/execute unit can execute instructions from the reorder buffer in any order.

Dispatch/Execute Unit

The dispatch/execute unit schedules and executes the micro-ops stored in the reorder buffer according to data dependencies and resource availability. The reservation station handles the scheduling and dispatching of micro-ops from the reorder buffer. The results of a micro-op execution are returned to the reorder buffer and stored along with the micro-op until it is retired. If two or more micro-ops of the same type are available at the same time, then the reorder buffer follows a FIFO algorithm to execute them. Two integer units, two floating-point units, and one memory-interface unit handle execution of micro-ops. Thus up to five micro-ops can be scheduled per clock. The two integer units can handle two integer micro-ops in parallel. One of the integer units is designed to handle branch micro-ops. This unit detects branch mispredictions and signals the branch target buffer to restart the pipeline. The memory interface unit handles the load and store micro-ops. The memory interface unit executes both a load and a store in parallel in one clock cycle. The floating-point execution units are similar to those found in the Pentium processor, few new floating-point instructions have been added to the Pentium Pro processor.

Retirement Unit

The retirement unit commits the results of speculatively executed (decided by branch prediction mechanism) micro-ops to permanent machine state and removes the micro-ops from the reorder buffer. The retirement unit continuously checks the status of micro-ops in the reorder buffer, similar to the reservation buffer. It then retires completed micro-ops in their original program order, taking into accounts interrupts, exceptions, breakpoints, and branch mispredictions. The retirement unit can retire three micro-ops per clock. In retiring a micro-op, it writes the results to the retirement register file and/or memory. The retirement register file contains the architecture registers (eight general-purpose registers and eight floating-point data registers). After the results have been committed to machine state, the micro-op is removed from the reorder buffer.

4. Instruction Set Architecture Features

To make a computer hardware work we must speak to the hardware in its language. The words of this machine language are called instructions, and the vocabulary is called an instruction set. The Pentium processor is a CISC architecture, but it achieves high performance by using many organizational features of RISC architecture. CISC stands for complex-instruction-set-computer whereas RISC stands for reduced-instruction-set-computer. Table.2 shows few popular to give feel of number of instructions available in CISC or RISC architectures.

Table.2 Instruction Set

SL	Instruction Set	Number
1	80x86	50,000,000
2	MIPS	5,500,000
3	PowerPC	3,300,000
4	SPARC	700,000
5	HP PA-RISC	300,000
6	DEC Alpha	200,000

As is well clear from Table.2 the Pentium processor family supports huge number of instructions. Few of them will be discussed in this section.

All the Intel Architecture instructions divided into three major groups:

- integer,
- MMX technology,
- floating-point, and
- system instructions.

Integer Instructions

Integer instructions perform the integer arithmetic, logic, and program flow control operations that programmers commonly use to write application and system software to run on an Intel Architecture processor. The integer instructions include different types of instructions like, data transfer instructions (PUSH, POP, MOV etc.); binary arithmetic instructions (ADD-integer add, ADC -Add with carry, SUB-Subtract, SBB-Subtract with borrow etc.); Decimal Arithmetic (DAA-Decimal adjust after addition, DAS-Decimal adjust after subtraction, etc.); Logic Instructions (AND, OR, XOR, NOT); Shift and Rotate Instructions (SAR-Shift arithmetic right, SHR-Shift logical right, etc.)

MMX™ Technology Instructions

The MMX instructions execute on those Intel Architecture processors that implement the Intel MMX technology. These instructions operate on packed-byte, packed-word, packed-doubleword, and quadword operands. All of the MMX technology instructions are grouped as MMX™ Conversion Instructions, MMX™ Packed Arithmetic Instructions, MMX™ Comparison Instructions, MMX™ Logic Instructions, MMX™ Shift and Rotate Instructions, or MMX™ State Management.

Floating-Point Instructions

The floating-point instructions are those that are executed by the processor's floating-point unit (FPU). These instructions operate on floating-point (real), extended integer, and binary-coded decimal (BCD) operands. These instructions include different types like, Data Transfer (FLD-Load real, FST-Store real, etc.); Basic Arithmetic (FADD-Add real, FADDP-Add real and pop, etc.); Comparison (FCOM-Compare real, FCOMP-Compare real and pop, etc.)

System Instructions

These instructions are used to control those functions of the processor that are provided to support for operating systems and executives.

5. Intel Pentium III Processor

The Pentium III is essentially a Pentium II running at higher speed, with two interesting and useful features:

- The processor serial number and
- Streaming SIMD Extensions (SSE).

The processor serial number (or chip ID) is a unique identifier ‘burned’ into the Pentium III processor that can be accessed over the internet, allowing e-commerce sites and others to know which machine is visiting a site or using a service. This has drag Intel Inc to a major controversy. But Intel claims that processor serial number can add value to a wide

range of applications in both business and consumer computing. The advantages that the processor serial number can provide are discussed below.

- Security: The e-commerce depends on the assurance that only only the authorized people access the confidential information. Applications that take advantage of the processor serial number can use that as another element of identification thus increasing confidentiality. Similarly, processor serial number can strengthen the data security for the consumer web sites who wants to maintain a section open only to their family members or so. It can also be used in businesses for adding a level of validation to electronic signature approvals.
- Manageability: IT departments use various ways to track assets such as MAC address or BIOS's GUID. But Intel claims that all these could be erased, so less reliable. But, processor serial number can be reliably used as a once it is burn on the chip at the time of manufacture it can never be erased. So designing applications using chip ID can help IT customers to manage their resources more efficiently.
- Information Management: Companies can turn information into a competitive advantage if they can manage it effectively. Information-related applications can use processor serial numbers to handle tasks ranging from finding multiple copies of virus-infected document, tracking change information, to delivering customized information to the end user.

The other significant feature of the Pentium III processor is the Streaming SIMD Extensions (SSE). Usually, the processors are SISD meaning Single Instruction and Single Data thus processing one data in one instruction. MMX and SSE, both share the concept of SIMD, they differ in the type of data they handle, and the way they are supported in the processor. MMX instructions are SIMD for integers, while SSE instructions are SIMD for single-precision floating-point number. MMX instructions operate on two 32-bit integers simultaneously, while SSE instructions operate on four 32-bit floats simultaneously. A major difference between MMX and SSE is that no new registers were defined for MMX, while eight new registers have been defined for SSE. The SSE can be used in 3D graphics applications.

6. Conclusions

This work is an extensive survey of Intel processors. More emphasis is given to Pentium Processors. Initially, the work explores the computing history. The detailed analysis of various generations of Intel microprocessors is done. Then the work deals with the hardware aspects of the Pentium Pro microprocessor in greater depth. The new features of Pentium III microprocessor are also discussed. It is expected that Intel's next generation microprocessors will be RISC in contrary to the present CISC ones. The Merced microprocessor is a development in that direction.

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