
EXPLORING DELAY-BASED PUFs FOR ENERGY-EFFICIENT LOW-OVERHEAD SECURITY OF WEARABLE DEVICES

Venkata Prasanth Yanambaka

School of Sciences
Texas Woman's University
Denton, TX, USA, 76201
vyanambaka@twu.edu

Uma Choppali

Department of Physics
Dallas College - Eastfield Campus,
Mesquite, TX, USA 75150
uchoppali@dallascollege.edu

Saraju P. Mohanty

Department of Computer Science
University of North Texas
Denton, TX, USA, 76201
smohanty@ieee.org

ABSTRACT

The Internet of Things (IoT) was introduced almost two decades ago. In the past two decades, technology has seen huge advancements. Many devices have become powerful and have less power consumption. Many IoT architectures and environments were introduced to help make life easier, especially in wearable devices. The market for these wearable devices has constantly increased over the years and is expected to reach its maximum in the next couple of years. They also pose a threat to users' privacy and security because they constantly store and transmit personal information such as location, heart rate, and other sensitive data. Therefore, addressing the security vulnerabilities is a crucial aspect of this research. This paper presents a hardware-assisted, energy-efficient, low-overhead security solution for wearable devices. Specifically, two Physical Unclonable Function (PUF) architectures: Arbiter PUF and Hybrid Oscillator Arbiter (HOA) PUF are analyzed for integration in IoT systems. The result shows that Arbiter PUF consumes $25 \mu\text{W}$, whereas HOA PUF consumes only $2.7 \mu\text{W}$ to generate keys for cryptographic purposes. These architectures introduce minimal power overhead while providing robust security, making them well suited for resource-constrained IoT ecosystems.

Keywords Physical Unclonable Functions · Hardware Assisted Security · Cyber Physical Systems · Smart Healthcare · Energy-Efficient Design · Wearable Devices

1 Introduction

Internet of Things (IoT) plays a vital role in shaping the modern world [1]. With rapid advancements in Artificial Intelligence (AI), the implementation of complex IoT architectures has become significantly more accessible and efficient. Robotics, in particular, integrates seamlessly with the IoT ecosystem, enabling the deployment of autonomous systems across smart healthcare, intelligent cities, and industrial automation. Autonomous drones, for example, are increasingly being deployed in diverse domains ranging from large-scale public events to military operations [2]. Furthermore, Large Language Models (LLMs) accelerate IoT development by assisting with code generation, system design, and predictive analytics, making these technologies more accessible to developers across varying expertise levels. Recent market forecasts estimate that approximately 9.1 billion active autonomous "smart" devices (AIoT) will be active worldwide by 2033. This exponential growth is anticipated to accelerate the transition toward Industry 5.0, emphasizing human-centric manufacturing, sustainability, and resilience through the integration of advanced digital technologies [3].

The rapid proliferation of AI-enabled IoT systems also expands the attack surface, thereby increasing system vulnerabilities. Recent studies have demonstrated that advanced AI agents can identify and exploit software weaknesses with increasing sophistication [4]. Even with protective guardrails in place, many users actively attempt to jailbreak and test AI models to identify exploitable security gaps. To address these integration challenges, Anthropic developed an open-source protocol called the Model Context Protocol (MCP) designed to safely connect external tools, applications, and data sources to AI models. However, there have been numerous cases of AI agents being misused, leading to unauthorized access, security breaches, and cyberattacks [5].

The rapid development in AI, and IoT devices has been made possible only with the shrinking transistor size on a chip [1]. Requirement for very high performance and ultra low power devices has never been so high. In recent years, AI has driven the demand for high-performance computing chips, including those equipped with high-bandwidth memory. The memory bandwidth for Nvidia H200 chips is 4.8 TB/s [6] which has risen from 336.5 GB/s on its Nvidia Titan X graphics processing units (GPUs) in 2015. Fin Field-Effect Transistors (FinFETs), 3D transistors that employ fin-shaped channel structures, has enabled to continue miniaturizing transistor dimensions to advanced technology nodes. Scaling bulk CMOS or planar transistors has been challenging beyond 32nm. But scaling resumed beyond 22nm with the FinFETs architecture and geometry. These advancements have enabled the development of high-performance, ultra-low-power devices for embedded and IoT applications.

Fig. 1 illustrates the architecture of wearable devices within the broader IoT ecosystem. Recent advances in consumer-grade Large Language Models (LLMs) have further simplified the development of wearable IoT applications by assisting with software development, system integration, and intelligent data processing. There are many commercial wearable headsets which are used in various applications, including opticians to diagnose various issues [7, 8]. There are also many other applications of wearable devices in Smart Healthcare [9] as shown in Fig. 1.



Figure 1: Illustration of the Internet of Things (IoT).

This paper presents a PUF architecture that can be used to secure the resource-constrained wearable technologies. Many vulnerabilities and security concerns were identified in the software and hardware developed using LLMs. Georgia Institute of Technology researchers recently released an article showing the risks of developing the software and hardware using AI models [10]. Google Threat Intelligence Group (GTIG) recently published an article showing the first known threat actor using a zero-day exploit believed to have been developed with AI [11]. The vulnerability allowed bypassing two-factor authentication after valid credentials were obtained and that it was a semantic logic flaw involving incorrect developer assumptions. Currently, AI primarily enhances the capabilities of human attackers rather than replacing them. It accelerates research, software development, reconnaissance, phishing campaigns, and exploit development. [11]. In this context, PUFs provide a hardware-assisted security primitive capable of generating device-unique cryptographic keys and strengthening hardware-rooted trust, thereby helping to mitigate several classes of attacks against resource-constrained IoT systems.

This paper is organized as follows: Section 2 presents the state of the art of Hardware Assisted Security while the novel contributions of the paper are presented in Section 3. An introduction to PUF, its working and applications are presented in Section 4. The architectures of PUF are presented in Section 6. Section 7 presents the simulation results and the conclusion and the future directions of this research is presented in Section 8.

2 Security of Wearable Devices - Challenges and Hardware-Assisted Security (HAS) Approach as a Solution

Wearable devices have become increasingly prevalent in recent years [12]. The global adoption of smartwatches and other wearable technologies continues to grow annually, driven by advances in sensing, connectivity, and artificial intelligence. These devices continuously collect physiological and environmental data, which are typically transmitted to cloud platforms for storage, analysis, and remote access. Wearable technologies have found widespread applications in both civilian and military domains, including health monitoring, fitness tracking, remote patient care, situational awareness, and mission-critical operations.

2.1 Security Challenges of Wearable Devices

Wearable devices offer numerous benefits that enhance consumers' quality of life. Fitness tracking is one of the key features that has contributed to the growing popularity of wearable technologies in the consumer market [9]. Researchers around the world are using the wearable devices for developing IoT architectures for applications such as sleep monitoring, thyroid monitoring [13] and other healthcare services. They constantly gather user information and transmit to the cloud. In certain applications, healthcare providers can remotely monitor patient data, enabling improved access to medical services and real-time health assessment [9].

Despite these advantages, wearable devices introduce security and privacy vulnerabilities that may expose sensitive user information to unauthorized entities [14]. Several commercial wearable devices have faced restrictions or bans in certain workplaces due to privacy concerns. For example, smart glasses can potentially record images or videos without the awareness or consent of individuals, creating risks in sensitive workplace environments. Additionally, wearable devices may collect personal information, including heart rate, location, and sleep patterns, when users enable such data-sharing features. Unauthorized access to this information could reveal sensitive details about users' health, daily activities, and lifestyles. Fig. 2 illustrates the major security challenges associated with wearable devices.



Figure 2: Security Challenges of Wearable Devices.

There are many security vulnerabilities that affect wearable devices as shown in the figure [15, 16, 17]. An attacker can get information from the devices using side channel attacks [18]. These attacks take advantage of the vulnerabilities in the hardware rather than in the software. Attackers can exploit devices through side-channel attacks by analyzing power consumption, signal timing, and, in some cases, sound. Attackers also introduce Trojans into the devices and eavesdrop into the conversation in the network.

2.2 Hardware-Assisted Security (HAS) - Brief Introduction

Hardware-Assisted Security (HAS) is a promising approach for addressing these security challenges. A HAS is an extra module dedicated for security in the system. Numerous HAS solutions have been proposed for IoT applications, offering various levels of security capabilities. Some HAS modules can perform end-to-end encryption of the communication channel, while others do not have this capability [19, 20, 21]. The functionality and design of a HAS module depend on the specific application requirements, system constraints, and security specifications.

One of the widely used HAS is Trusted Platform Module (TPM). It is an add-on module that has wide range of applications, from personal computers and servers to small IoT devices [14, 22, 23]. A TPM is a multifunction module that can perform tasks like encryption, decryption, and other cryptographic operations like hashing. TPM can also produce random numbers for keys and in some cases like RSA generate public and private key pairs. One disadvantage is that unlike a PUF, a TPM produces pseudorandom numbers using a program to generate the random numbers.

Another commonly used HAS module is ARM Trustzone [24, 25]. This is a commercially available solution by ARM that is similar to a TPM but also provides a quarantine zone for performing the cryptographic tasks [26]. Arm Trustzone has the ability to generate keys, perform encryption and decryption and provide hashing algorithms similar to a TPM. Arm also uses hardware based key generation similar to the PUF. However, one disadvantage of ARM TrustZone is that it is more expensive compared to a TPM.

The third widely used HAS module is PUF [27, 20]. It can generate keys necessary for end-to-end encryption of communication channel, device identification and authentication in a network. They have several other applications as well. PUFs exploit naturally occurring nanoscale manufacturing variations to generate keys; therefore, the resulting keys are inherently random adding an extra layer of security to the overall system. [28]. Attackers cannot identify the keys generated by PUF module. A PUF on its own cannot perform cryptographic tasks, such as encryption and decryption, but when integrated with a cryptoprocessor, it can provide better security.

2.3 Hardware-Assisted Security (HAS) is Best Suitable for Wearable Devices

Wearable smart devices are embedded systems that run on batteries. These devices continuously monitor the user information and transmit to the cloud or store it locally for later access. This introduces privacy and security risks as discussed earlier. A misplaced wearable device, with a weak password can potentially put the user privacy at risk.

Many software-based security solutions require high processing power or utilize significant device resources. Wearable devices have limited resources and must operate in a resource-constrained environment. Hence, adding an extra HAS module can help in the case of a wearable device. All the cryptographic processes will be off-loaded to the HAS which reduces the load on the main embedded processor.

A PUF module has the ability to generate multiple keys. With an appropriate PUF integrated into the design, it can generate multiple keys, potentially thousands in some architectures. This can be very helpful when the system is under attack. Although a PUF can generate a large number of keys, not all of them can be used for cryptographic purposes. Even when the system is under attack, the keys can be changed on-the-fly if necessary.

3 Novel Contributions

3.1 Problem Definition

Previous sections discussed various security vulnerabilities associated with wearable devices. There are many vulnerabilities that an attacker can utilize and gain access to the system [15, 16, 17, 25]. The “*things*” in the IoT network are low-power resource-constrained devices that cannot execute resource-intensive cryptographic algorithms. Furthermore, the limited storage capacity of these devices makes it challenging to securely store long cryptographic keys required for end-to-end encryption. A device key, once compromised, can potentially provide access to the entire IoT ecosystem.

3.2 Proposed Solution

HAS is one of the potential solutions for IoT and wearable devices. PUF modules help achieve robust security in IoT environments. Keys generated by a PUF module cannot be reproduced in any other module. Even if the attacker gets hold of the key, it can be changed on-the-fly using an appropriate PUF architecture.

This paper analyzes two designs of PUF architectures, Arbiter and Hybrid Oscillator Arbiter (HOA) PUF. These two PUF Architectures were selected for IoT security because they exhibit a very low key generation error rate. The key size can be scaled according to the available resources, and the proposed designs are reconfigurable. This paper

presents the PUF architectures, their simulation results and an analysis demonstrating their sustainability for tailored IoT architectures.

4 State Of The Art Of Physical Unclonable Function

During the fabrication of an Integrated Circuit (IC), several manufacturing variations get introduced that are uncontrollable, unavoidable, unpredictable and naturally occurring. Although technology has advanced sufficiently to manufacture ultra low power devices at very small technology nodes, the manufacturing variations have been affecting the yield of the final chips for decades [29]. Moreover, they not only degrade device performance but also influence aging effects throughout the device's operational lifetime [30].

PUF uses these manufacturing variations to generate the random numbers [20]. These random numbers generated by the PUF are used for a wide range of cryptographic applications, including smart healthcare, smart agriculture, smart cities, and other IoT applications [21, 31]. Fig. 3 shows the working of a PUF. Consider two PUF modules, P_1 and P_2 . The input to a PUF is called a "challenge" and the random number output generated from the PUF module is called "response". Given a PUF module P_1 , a challenge produces a corresponding response and these two are called "challenge response pair" (CRP) for that module. Every new challenge of PUF must produce a new response. If "N" challenges are given to a PUF, it generates "N" responses.

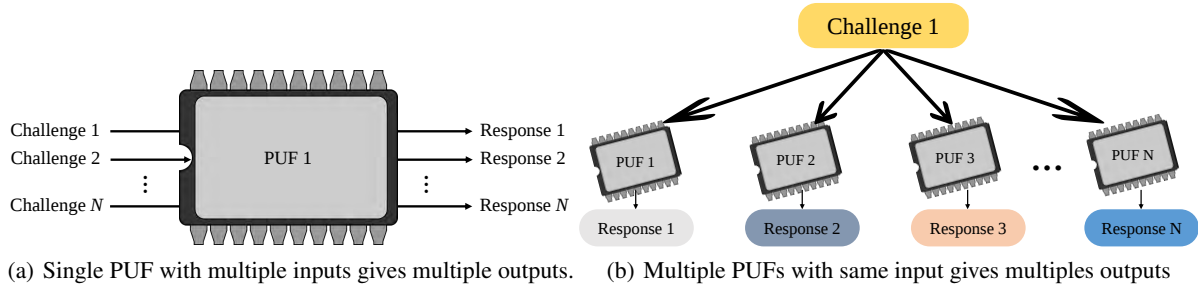


Figure 3: Working of a PUF.

PUFs have numerous cryptographic applications, including device authentication, encryption, blockchain, and particularly in mission-critical domains such as healthcare, defense, and military systems. To employ PUF modules in cryptographic applications, the PUF modules must satisfy Figures of Merit (FoM) which are discussed further in section 7.

PUFs are classified into various architectures based on their underlying core components. These architectures include SRAM PUFs, Ring Oscillator (RO) PUFs, Quantum PUFs, and other variants. [32, 33, 20]. PUFs are classified into four categories based on the number of keys each architecture can generate while satisfying the required FoMs [34] as shown in Fig. 4:

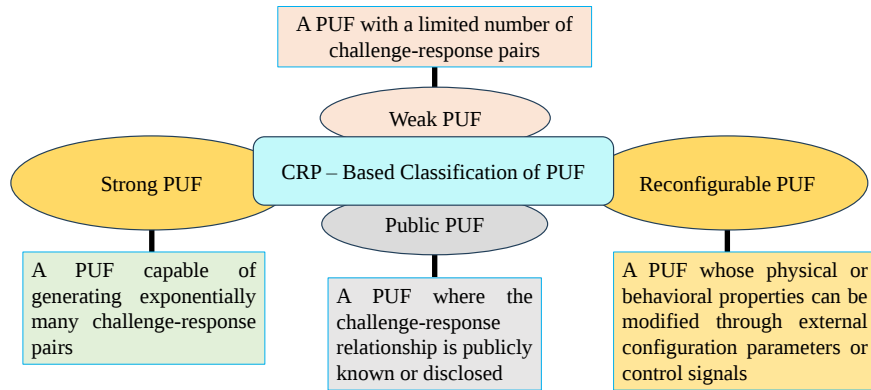


Figure 4: CRP - Based Classification of PUF.

- Weak PUF

- Strong PUF
- Reconfigurable PUF
- Public PUF

4.1 Weak PUF

Weak PUFs can generate only a limited number of random numbers that satisfy the Figures of Merit (FoMs). In certain cases, the number can be as low as '1'. The number of keys generated that can satisfy the FoMs depends on the manufacturing variations present in the IC. One such architecture that generates limited number of reliable cryptographic keys is SRAM PUF [35]. One limitation of SRAM PUF that results in a low number of usable keys is the occurrence of errors during key generation. Various factors, such as temperature, voltage fluctuations, and humidity, affect its performance, necessitating the use of fuzzy extractors. Although it is a weak PUF, almost every IoT device or board has an SRAM module, making its implementation relatively easier.

4.2 Strong PUF

Some PUF architectures, such as Arbiter PUF, can generate a larger number of cryptographic keys that satisfy the FoMs. These are called "Strong PUFs" [27]. This increases the robustness of the PUF and expands its range of applications. In certain cases, the number of usable keys can reach several hundreds. Unlike SRAM PUF, most of these architectures are application-specific modules requiring additional hardware on the chip, resulting in trade-offs between battery life and performance. Recent developments in quantum technology have also led to the emergence of quantum PUF architectures.

4.3 Reconfigurable PUF

Architectures such as Arbiter PUFs remain vulnerable to machine learning attacks [20]. With the rapid growth of AI, even the natural randomness introduced in PUF modules is susceptible to modeling attacks. To resist such adversaries, PUFs can be reconfigured on-the-fly to generate multiple responses. This capability proves particularly valuable in applications requiring a high volume of keys, such as networking.

4.4 Public PUF

A public PUF differs fundamentally from the traditional PUF. Unlike Strong or Weak PUFs, where the challenge-response behavior must remain confidential to preserve security, a Public PUF is characterized by having a publicly available mathematical model that can simulate its behavior. However, the critical distinguishing feature is that while this model can accurately predict the PUF's responses, doing so requires significantly more computational time and resources than physically querying the actual device itself. This asymmetry between the ease of physical measurement and the computational difficulty of simulation forms the security foundation of Public PUFs. This property enables unique cryptographic protocols, such as certificate-based authentication and secure key exchange [34].

4.5 Other PUF Classifications

The classification mentioned above is based on the number of CRPs generated that can satisfy the FoMs. PUF is classified into two categories based on the material used to design the PUF. They are Silicon PUFs and Non Silicon PUFs.

Silicon PUFs are the most widely studied and implemented category, leveraging inherent manufacturing variations present in silicon-based semiconductor devices such as transistors, gate delays, and memory cells. These variations arise naturally during the CMOS fabrication process due to microscopic differences in doping concentrations, oxide thickness, and threshold voltages, even when devices are manufactured using identical masks and processes. The Arbiter PUF, SRAM PUF, and Ring Oscillator (RO) PUF architectures discussed in the previous subsections are examples of silicon-based PUFs. [35, 28, 36].

Non-Silicon PUFs, on the other hand, derive their unique responses from physical phenomena outside conventional silicon-based transistor structures. These architectures exploit properties such as optical scattering, magnetic characteristics, or intrinsic material variations to generate unclonable identifiers. One such architecture is the Optical PUFs, which utilizes the unique scattering patterns produced when light passes through randomly structured optical media [37]. The other type of Non-Silicon PUFs is the Magnetic PUFs, which rely on the unpredictable magnetic domain patterns

in materials [38]. With the advancements in Quantum technology, quantum-based PUFs have also been introduced for post-quantum cryptographic applications [32].

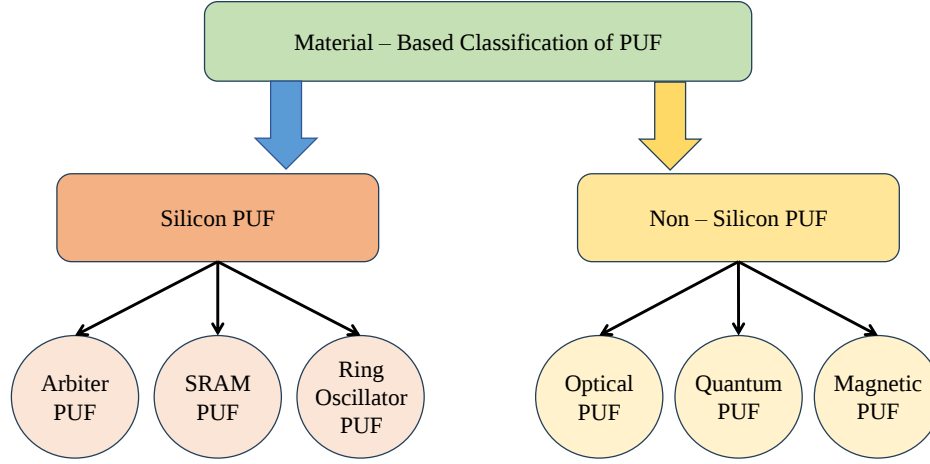


Figure 5: Material - Based Classification of PUF.

5 Related Prior Research

Table 1: Currently Available Security Protocols for Wearable Devices.

Research Works	Security Application	Specific Properties
Yamada et. al [39]	Protection against unintentional face image capture	• A dedicated device is required for the proposed work • Easily accessible by user • Anonymity of user.
Henne et. al [40]	Prevent infringing media through geo-tagged media	• Can be used in Smart Phone • Network connection is required • Cost effective Third party services required
Hoyle et. al [41]	Lifelogging cameras were used for exploring privacy management of people in daily life	• Cameras were required • Does not require network connectivity on wearable • Privacy of the user and others around them were tested
Ashok et. al [42]	Beacons in user eyewear communicate with camera to select privacy preferences	• Embedded into user eyewear • No connectivity is required • User interaction is not necessary • Uses IR signals to transmit the privacy settings

With the rapid advancement of AI, the demand for high performance and high throughput devices has increased significantly. In particular, the memory bandwidth of the GPU has increased by more than tenfold over the past decade [43, 6]. There are several challenges associated with implementing AI at the scale required [44]. Among these, the power consumption and the performance of the transistor devices are the two most significant challenges. In particular, research on transistor devices focuses on device scaling with an intent to maximize density, high throughput and ultra-low power consumption.

Technology scaling has reached the atomic level [45]. Technology scaling has reached a level that has never been seen before. Such atomic scaling levels were not possible with the planar transistors. Bulk CMOS transistors could scale well

until the 32nm technology node. However, the one dimensional planar CMOS transistor geometry was not sufficient for scaling beyond 32 nm into the 22nm. Consequently, 3-dimensional FinFETs were developed to overcome this scaling challenge of conventional planar transistors [46, 47]. Due to this increase in transistor density on a single die, high performance SoCs and NoCs have become feasible which accelerated growth and widespread development of IoT.

The price of the final chip is decided based on the yield [1]. The yield in particular is affected by the manufacturing variations introduced during the fabrication of the IC. As mentioned in previous section, they are naturally occurring, unavoidable, unpredictable and uncontrollable. Hence the research community started using the naturally introduced variations for cryptographic purposes. These are used for generating the natural random numbers using the PUF modules.

With the availability of high performance and low power technology nodes, researchers around the world have started developing IoT architectures for a wide range of applications, including smart healthcare, wearable technologies, and smart transportation over the last few decades. For example, a quadrature design using only standard components was developed in 2016 by Kougianos et al. for real-time object tracking [48]. A thyroid monitoring system was proposed by Prabha et al. in 2016 [13] as an application of smart healthcare. Recently, commercial wearable virtual reality (VR) headsets have become widely available, demonstrating the rapid evolution and growing maturity of wearable technologies [7]. The availability of highly capable commercial AI platforms, such as OpenAI, Google Gemini, and Anthropic's language models, has simplified software development by assisting with code generation, debugging, documentation, and system integration [49, 50, 51].

Widespread adoption of AI models has increased cybersecurity challenges [4]. Commercially available AI models have brought to light several unknown software vulnerabilities, including zero-day vulnerabilities [52]. Furthermore, large language models (LLMs) and agentic AI systems have increasingly been used to discover security flaws in commercial and enterprise-grade software and hardware [53]. A single solution might not be able to resist these attacks, but one of the solutions is to use Hardware Assisted Security (HAS). PUF is one such HAS primitive that can generate true random numbers using manufacturing variations. Research based on PUF has been conducted extensively over the last few decades. In [54], a ring oscillator-based PUF (RO PUF) was developed. In [55], a trusted sensor for mobile applications was proposed. Furthermore, in [56] a PUF was presented that is tolerant to process variations, temperature changes, and voltage fluctuations.

This paper mainly discusses two architectures of PUF: RO PUF and Arbiter PUF [57, 58]. These PUF architectures have been evaluated and implemented in many applications. Several other PUF architectures have also been proposed, including SRAM PUFs [59], which have been studied since the early development of PUF-based security solutions. One advantage of SRAM PUF is that most IoT devices already contain embedded SRAM, which can potentially be used to generate keys using PUF. However, SRAM PUFs are susceptible to environmental variations and noise during key reconstruction, necessitating the use of additional error correction mechanisms, such as fuzzy extractors, to reliably generate cryptographic keys.

An Oscillator Collapse Physical Unclonable Function (OC-PUF) was proposed by Zayed et al. in [60]. The architecture proposed in the paper is focused mainly on the power consumption that is more suitable for devices with resource constraints. The authors used a 20nm trigate FinFET architecture for the simulation. The overall power consumption of the device is about 140 nW with the worst case simulations showing a 750 nW power consumption. The reliability of the proposed design is 99 % with a uniqueness of 50.01 %.

A Hybrid Ring Oscillator Arbiter PUF is proposed by Driemeyer et al. in [61]. The authors utilized a 28nm planar CMOS technology to simulate and evaluate the proposed design. The primary objective of this architecture is to develop a high-speed PUF capable of generating cryptographic keys at a high bit rate while maintaining low power consumption. The PUF architecture in [61] generates the keys at a rate of 4.515 Gbits/sec while consuming about 0.259 pJ/bit.

Pahlevi et al. proposed a Per-Selection-Enhanced Arbiter PUF architecture in [62]. The authors evaluated the proposed design using 56 FPGA boards to assess its performance and reliability. The primary focus of the architecture presented in [62] was improving the authentication performance, particularly in terms of the False Acceptance Rate (FAR) and the False Rejection Rate (FRR), which remained below or close to 2.5.

Das et al. proposed a PUF architecture based on voltage-gated spin-orbit torque magnetic tunnel junctions (VGSOT-MTJs) in [63]. The proposed PUF architecture achieves a uniqueness of 50.2% and a reliability of 97.3%. Furthermore, the architecture demonstrates strong resistance against machine learning (ML)-based modeling attacks. For example, a multilayer perceptron (MLP) attack achieved a prediction accuracy of less than 55.27%, indicating improved resilience against ML-based attacks. The proposed PUF consumes approximately 63.67 fJ/bit while generating cryptographic keys at a bit rate of 0.27 Gb/s.

6 PUF Architectures of Energy-Efficient Low-Overhead Wearable Security

This section presents the HOA-PUF architecture for energy-efficient low-overhead wearable security. The core components of the HOA-PUF are Ring Oscillator (RO) PUF and the Arbiter PUF. Both of these architectures have been extensively studied over the years and have demonstrated reliable performance. These PUF architectures can be implemented on an FPGA without requiring fabrication, making them suitable for rapid prototyping and performance evaluation in low-power applications, such as the Internet of Things (IoT). This provides researchers with the advantage of readily integrating the same module into IoT environments for rapid prototyping, testing, and deployment.

6.1 Ring Oscillator PUF

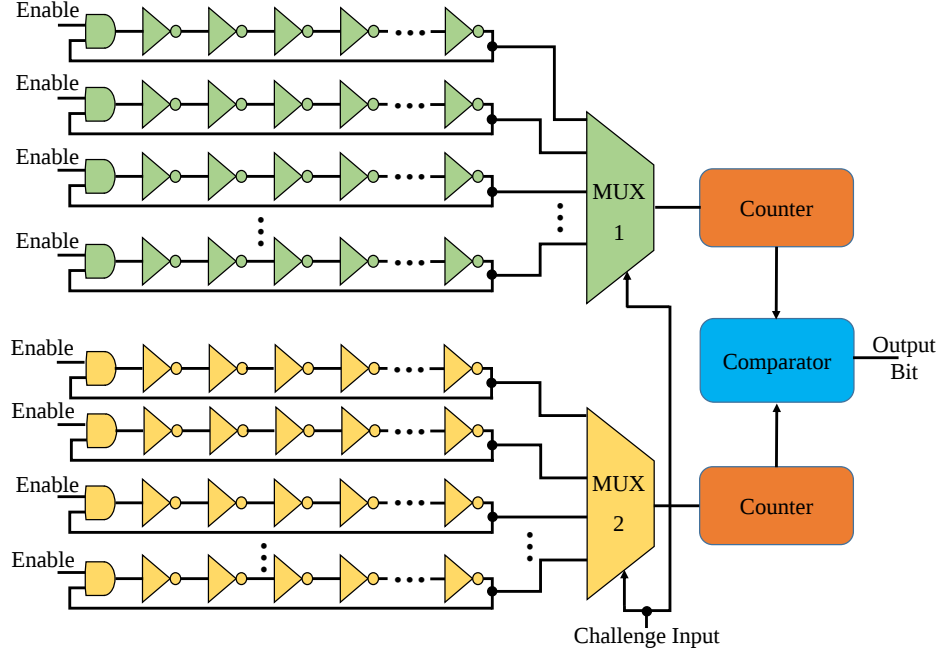


Figure 6: Ring Oscillator PUF.

The architecture of RO PUF is shown in Fig. 6. The inverter is the fundamental building block of an RO PUF. As illustrated in the figure, the architecture consists of two sets of ROs connected to multiplexers. The challenge inputs are applied as select lines to the multiplexers. When a challenge is applied to the PUF, one RO is selected from each set and the resulting oscillation signals are passed to the counters. These counters measure the frequencies of the selected ROs. Finally, a comparator evaluates the frequency difference between the selected ROs and generates the output response bit as either '1' or '0'.

The inverter, as the fundamental component of an RO PUF, captures inherent manufacturing variations, including gate delays, dopant concentration variations, and temperature-induced parameter shifts, which influence the final key generation process. Although all ring oscillators are designed identically with the same number of stages, process variations during fabrication introduce subtle, yet significant, differences in signal propagation delays. These variations contribute to the unique physical characteristics of each device and enable the generation of device-specific random responses.

6.2 Design of Arbiter PUF

Fig.7 illustrates the architecture of the Arbiter PUF consisting of two series of multiplexers. The output of the multiplexers in the first stage is connected to the input of the multiplexers in the subsequent stage. The challenge given to the PUF feeds the select lines of the multiplexers. The outputs of the multiplexers in the final stage are connected to a D flip-flop, with one output connected to the D input and the other connected to the clock input of the flip-flop. The flip-flop determines the final response bit based on the relative delay difference between the two paths.

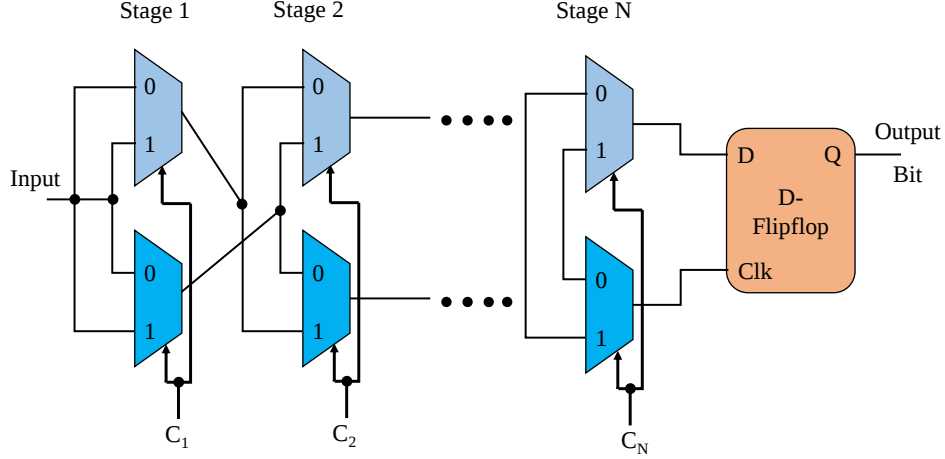


Figure 7: Design of Arbiter PUF.

The core component of an Arbiter PUF is the multiplexer. These multiplexers capture manufacturing variations and subtle differences in transistor geometries introduced during the fabrication process. The propagation delay introduced by each multiplexer stage accumulates through the delay paths, ultimately affecting the timing relationship between the two signals arriving at the D flip-flop. An input is applied simultaneously at the first stage of both series of multiplexers. The path this input takes through both the series of Multiplexers differs based on the challenge given to the PUF. Due to the gate delay added by each transistor and other components, the signals reach the D-flipflop at different times. If the signal connected to the D input arrives before the clock signal, the PUF generates an output response of '1'. Conversely, if the clock signal arrives before the D-input signal, the output response is '0'. The Arbiter PUF architecture shown in Fig.7 generates a 1-bit response for each applied challenge. Multiple Arbiter PUF instances can be combined to increase the output bit length of the overall PUF module.

6.3 Inverter-based HOA-PUF

Fig. 8 shows the design of HOA PUF. The core component of the design is the inverter as shown in the figure. Similar to the arbiter PUF, the delay is introduced to the signal by the inverters.

There are two sets of ROs in the design. All ROs in group 1 are connected to multiplexer 1 (MUX 1), while ROs in group 2 are connected to MUX 2. The architecture and design parameters of the ROs in both groups are identical. However, during the fabrication process, there are unforeseen manufacturing variations in which the output frequencies of individual ROs are not identical. As a result, each RO exhibits a unique oscillation frequency, which contributes to the generation of the PUF response. A D-flip-flop is used as the arbiter in the final stage of the circuit. The output of MUX 1 is connected to the D input of the flip-flop, while the output of MUX 2 is connected to the clock input. The challenge given to the PUF is fed as the select signal to these multiplexers. Unlike Arbiter PUF, this design has multiplexers and requires only one D-Flipflop.

The challenge decides the ROs that are selected for the output bit. A pair of ROs will generate one output bit similar to the RO PUF. The number of RO pairs selected decides the length of the output key. The length of the key varies with the design and the number of RO stages used in the architecture. Although there can be an exponential number of combinations of ROs, which gives a huge number of keys, not all of them can be used for applications. FoMs must be satisfied before they can be used for cryptographic purposes.

Fig. 9 illustrates the FinFET-based 1-bit HOA design. As shown, the inverter forms the core building block of the proposed architecture. The device dimensions, including the channel length and width used in the simulation, are also specified in the figure.

7 Experimental Results

This section presents the simulation results for the designs of Hybrid Oscillator Arbiter PUF and the Arbiter PUF. A comparison of the designs is performed and evaluated for integrating the architecture into the wearable medical designs for a robust security.

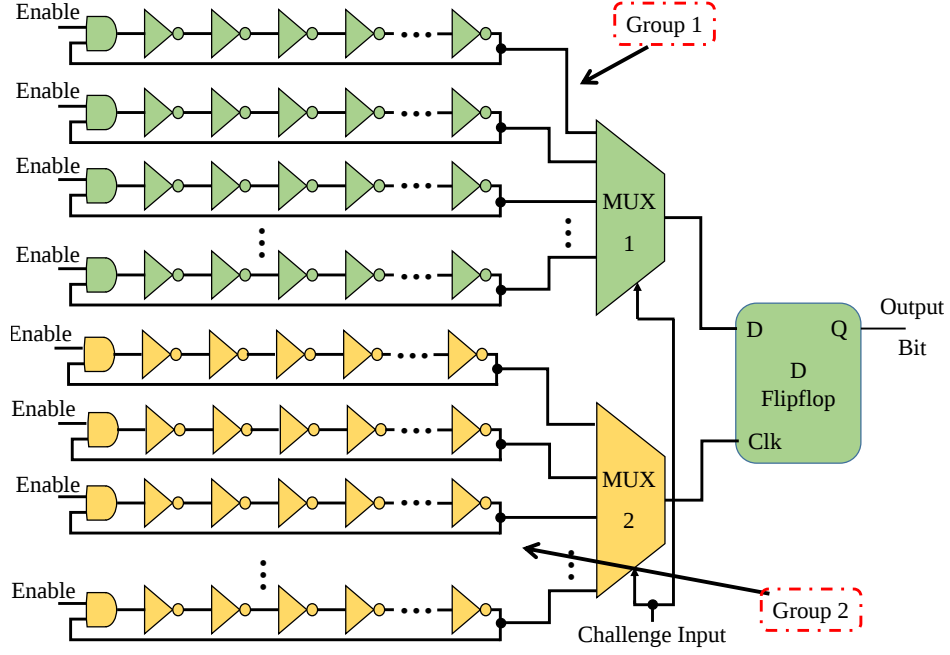


Figure 8: Hybrid Oscillator Arbiter PUF

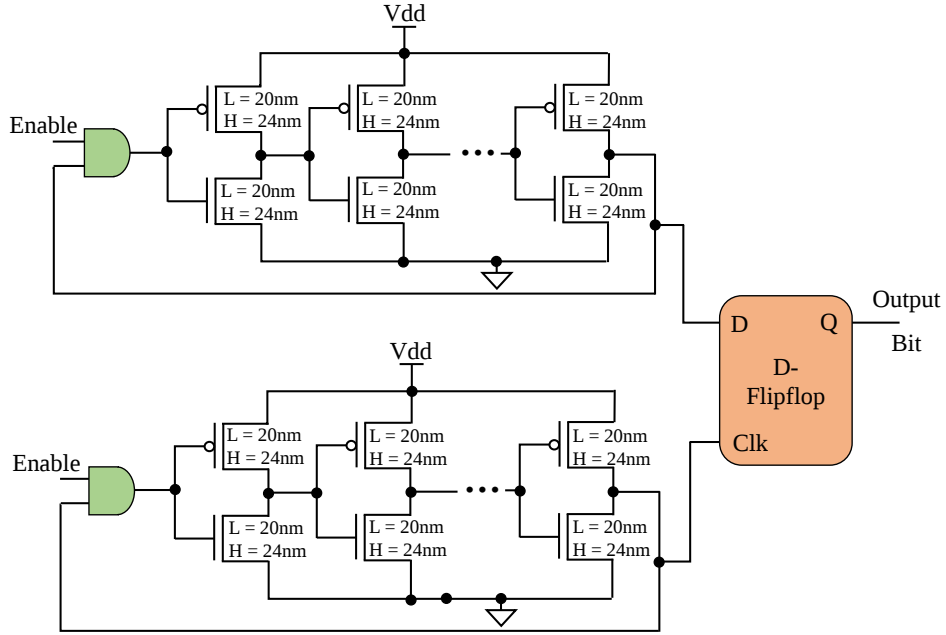


Figure 9: Design of Inverter based HOA PUF.

7.1 Experimental Setup

The models from [64] were used for simulating the HOA PUF. The FinFET parameters used for the simulation are given in Table 2. The same parameters were taken for all the transistors across all the stages of the ROs. Manufacturing variations were simulated using Monte Carlo simulations. The nominal values presented in Table 2 were varied 10 % to simulate the manufacturing variations. The characteristics of the inverter used in the proposed design are shown in Fig. 10.

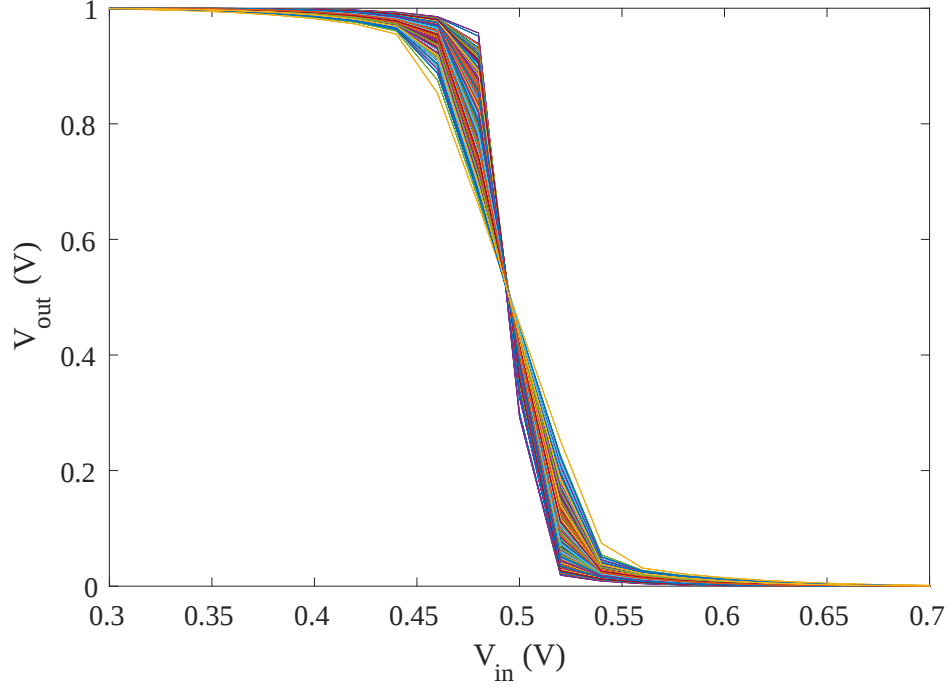


Figure 10: DC Analysis of Inverter with Process and Mismatch Variations.

Table 2: Nominal Device Parameters Used for the 14 nm FinFETs.

Device Parameters	Specific Values
Length (L)	20 nm
Height of Fin	24 nm
Fin Thickness	10 nm
Fin Width	10 nm
Number of Fins	2
Oxide Thickness	1.3 nm
Body Thickness	1.9 nm

7.2 Performance Evaluation

As mentioned in the previous sections, not all the keys generated by the PUF can be used for cryptographic purposes. The following FoMs must be satisfied before they can be used reliably:

- Uniqueness
- Reliability
- Average Power Consumed

7.2.1 Uniqueness

Uniqueness is the PUF's property to generate a unique key for that specific module. It can be categorized as two types of Uniqueness:

- *Intra-Uniqueness* - Given a single PUF module P_1 , every challenge given must produce a unique response.
- *Inter-Uniqueness* - When the same challenge input is given to multiple PUF modules, every module is expected to produce a unique response.

Uniqueness of a PUF is calculated using hamming distance. When two binary keys are considered, the number of bit positions they differ from each other is the hamming distance between the two keys. The ideal hamming distance between the considered keys must be 50 %.

Fig. 11 shows the signal frequencies generated by the ROs in the PUF module. This helps analyze the variation captured by the oscillators in the HOA PUF. Fig. 12 shows the uniqueness of all three PUF architectures, the RO PUF, the Arbiter PUF and the HOA PUF. RO PUF and Arbiter PUF uniqueness is taken as a benchmark to evaluate the proposed HOA PUF. The average uniqueness of Arbiter PUF is 50.30 %, and the average uniqueness of the RO PUF is 50.50 %. Compared to these, the keys generated by the HOA PUF show a hamming distance of 51.30 %. All the three values are closer to the ideal value, 50 %, but the number of keys that are closer to the ideal value are more in the proposed HOA PUF. This shows the HOA PUF successfully captures the manufacturing variations in the circuit.

Table 3: Uniqueness of PUF.

PUF Topology	Uniqueness (%)	Ideal Value (%)
HOA PUF	51.3	50
RO PUF	50.3	50
Arbiter PUF	50.3	50

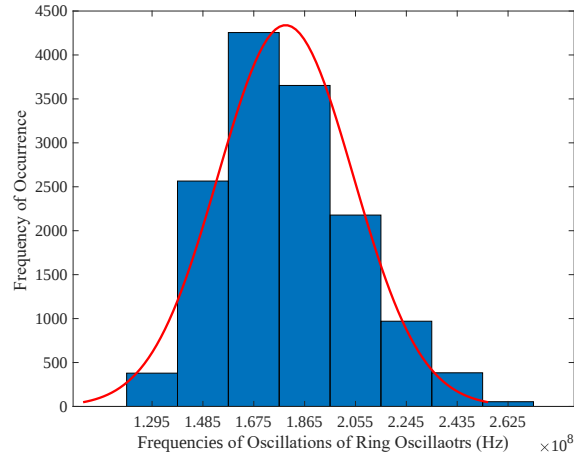


Figure 11: Histogram of Oscillation Frequencies of the Ring Oscillators in PUF for 10,000 Oscillators.

7.2.2 Reliability

Reliability is the ability of a PUF module to generate the same response for a given challenge despite the effects of circuit aging and environmental variations. Once the circuit is fabricated and deployed in a mission-critical application or consumer applications, it is expected to maintain consistent performance throughout the product's operational lifetime. Cryptographic applications, in particular, demand a high degree of reliability and robustness, as the loss or alteration of a cryptographic key may result in data loss and, in some cases, irreversible consequences. Therefore, a PUF is expected to consistently reproduce the same key under varying environmental conditions, including fluctuations in power supply voltage and temperature.

Fig. 13 shows the simulation results of the reliability of the PUF architectures. The reliability of the PUF is also measured using hamming distance. During simulation, the same challenge is given to the PUF under temperature and power supply variations. As shown in the figure, the error rate of the HOA PUF is 2.35 %, RO PUF is 1.32 %, and Arbiter PUF is 1.8 % which are closer to the ideal values of 0 %.

7.2.3 Average Power

Wearable devices require ultra low power operation for a longer battery life. The power consumption of a PUF module plays a crucial role in its integration into applications in wearable technology. The average power consumed is the average of the total power consumed by the module over the period of key generation. In addition to wearable devices, the power consumption also plays a major role in the integration of this PUF design into resource-constrained environments, including smart healthcare and smart city applications.

The average power consumption of all three PUF architectures is shown in Fig. 14. The Arbiter PUF has 16 stages of Multiplexers and HOA PUF has 7 stages of inverters. The RO PUF and the HOA PUF have the same number of inverters with the only difference being an additional counter and comparator. The benchmark results were generated

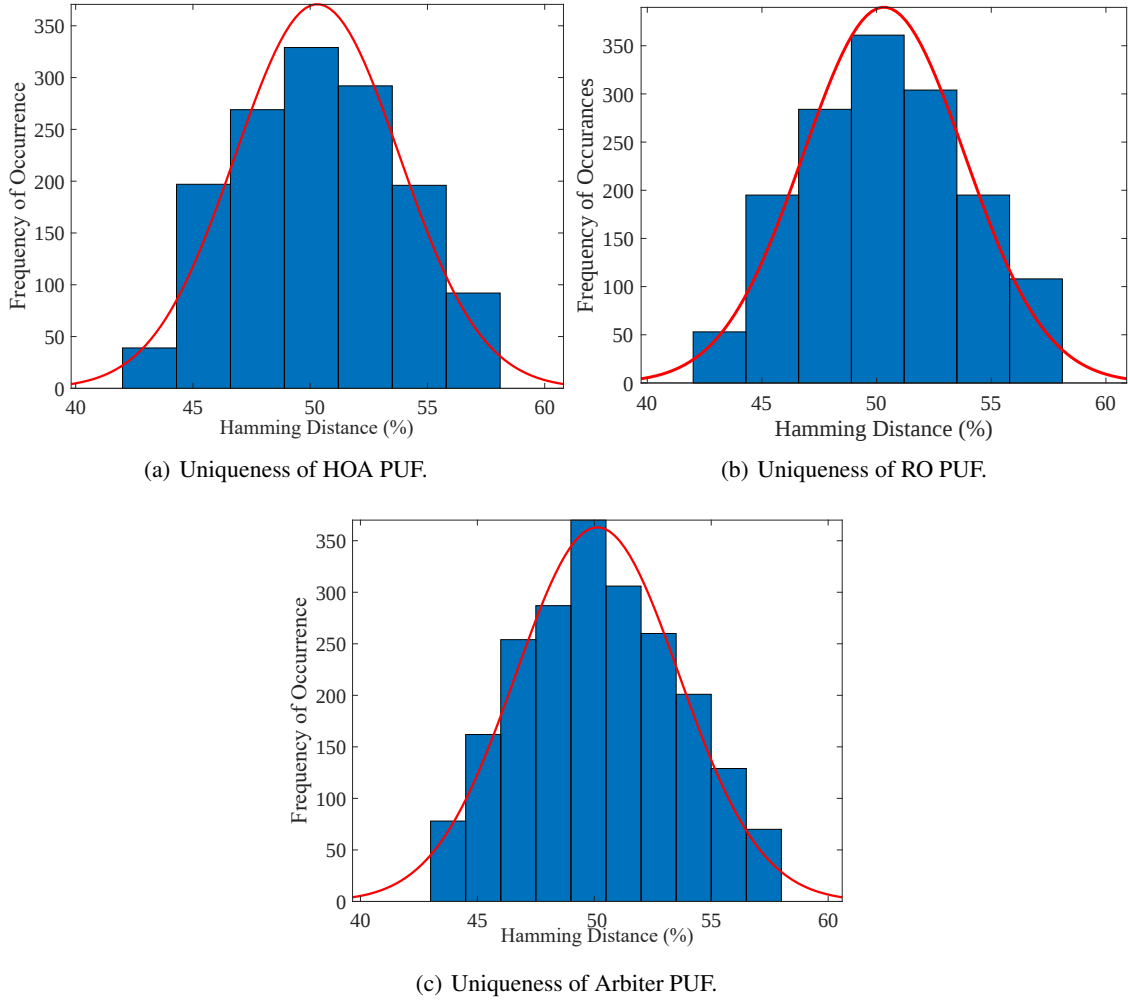


Figure 12: Uniqueness of the PUFs.

for both the RO PUF and the Arbiter PUF. RO PUF consumes about $3.5 \mu\text{W}$ and the arbiter PUF consumes about $2.5 \mu\text{W}$. The HOA PUF on the other hand, consumes about $2.7 \mu\text{W}$ to generate 1 key.

7.3 Analysis of PUF Architectures

Table 4 shows the characterization of the proposed HOA PUF and a comparison with the other two architectures, RO PUF and Arbiter PUF. The uniqueness of the HOA PUF is about 51.3 % compared to the RO PUF, which is 50.4 % and the arbiter PUF, which is 50.3 %, as shown in the table. Although the average uniqueness of the RO PUF and the Arbiter PUF are closer to the ideal value of 50 %, as mentioned before, the standard deviation is higher in keys generated by the other two architectures. In addition to the lower standard deviation of average uniqueness, the error rate of the HOA PUF is 2.35 %. The average power consumption of the HOA PUF is also significantly lower compared to the other two architectures, and Arbiter PUF in particular which is about $10 \times$ higher than the HOA PUF. As the Arbiter PUF does not contain a multiplexer dedicated to selection of the individual components, the key generation time is much higher in the arbiter PUF. But there is also a trade off of the power consumption in the Arbiter PUF.

8 Conclusion and Future Research

This paper presented the analysis of two designs of PUF, Arbiter PUF and Hybrid Oscillator Arbiter PUF for integration into wearable devices. These wearable devices are low power devices that are incapable of performing high cryptographic tasks. Introducing such a PUF module to these devices helps generate keys and eliminates the need to store the keys.

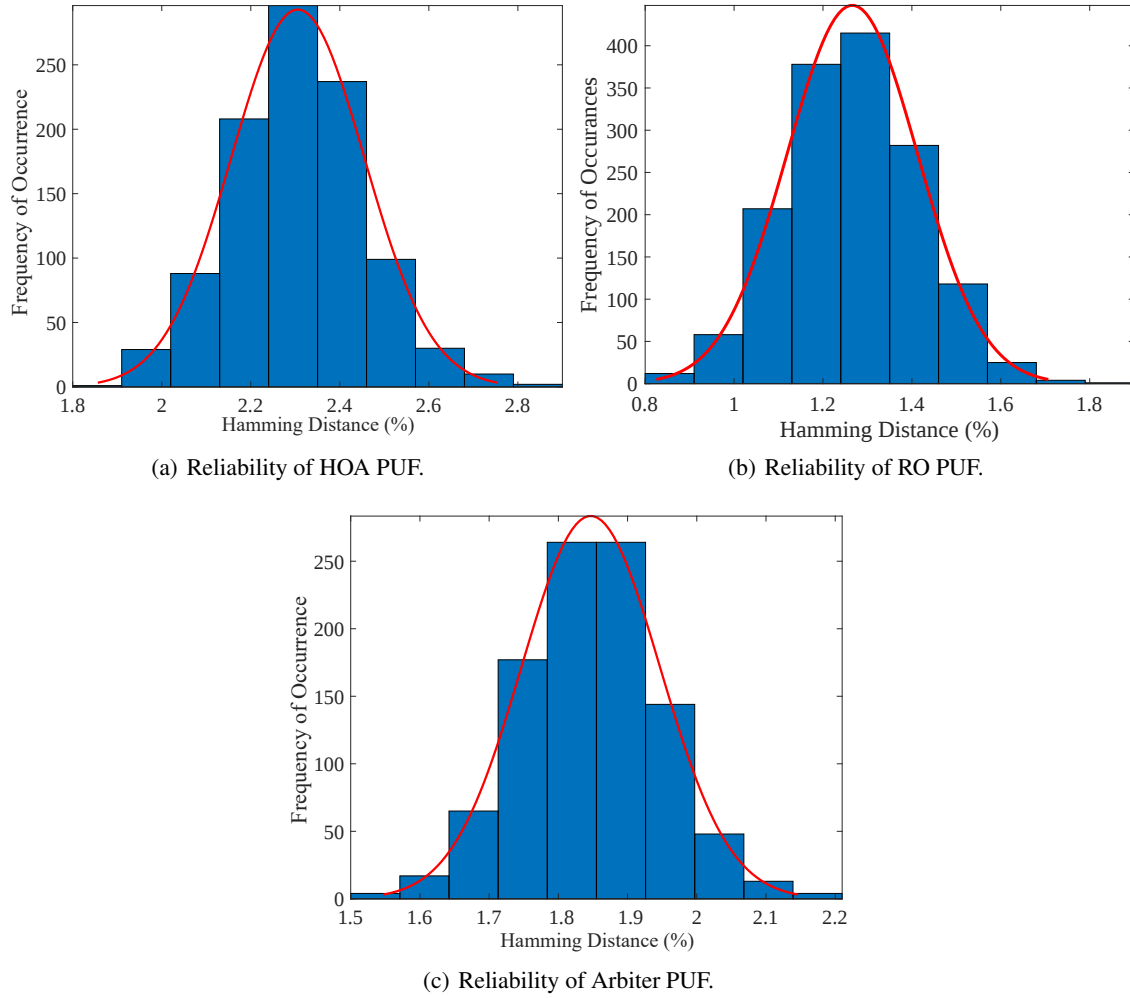


Figure 13: Reliability of PUFs.

Table 4: Characterization Of Power Optimized PUF Designs.

Metrics	Ideal Value	HOA PUF	RO PUF	Arbiter PUF
Uniqueness	50 %	51.3 %	50.4 %	50.3 %
Reliability	0 %	2.35 %	1.32 %	1.8 %
Average Power	–	2.7 μ W	3.5 μ W	25 μ W

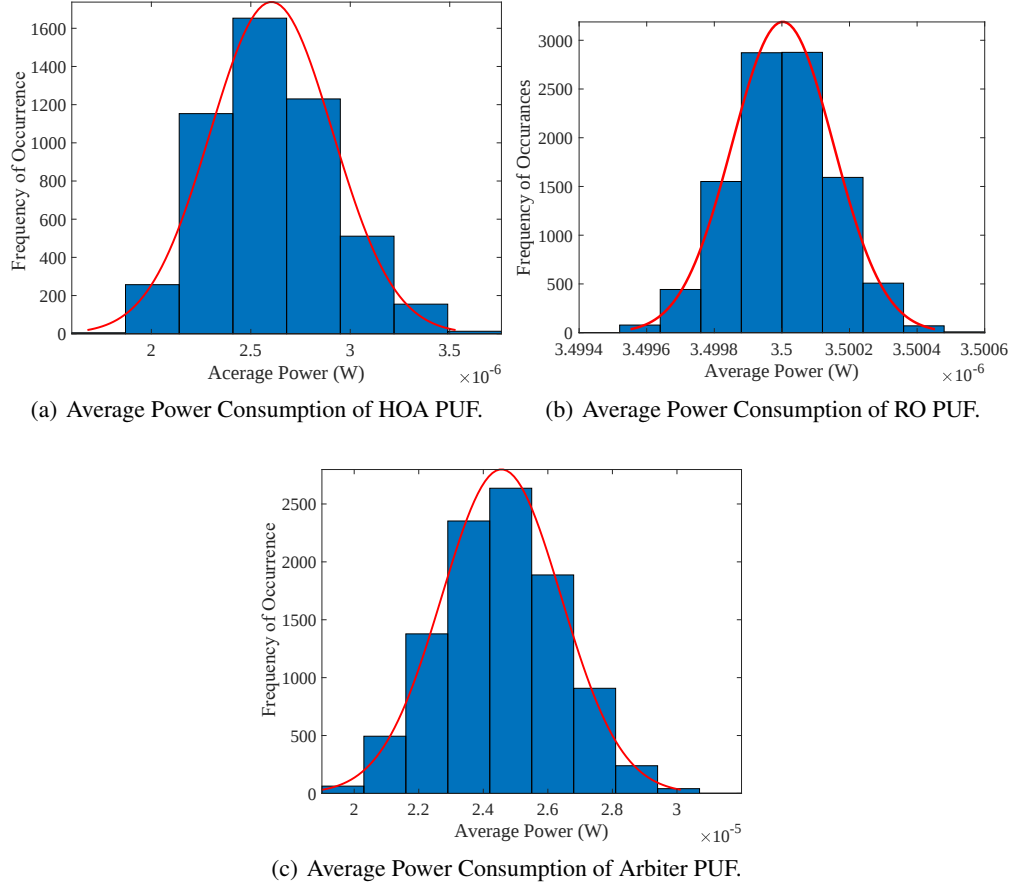


Figure 14: Average Power Consumption of the Proposed PUFs.

Depending on the PUF module architecture, it can generate any length of keys, and, if necessary, the PUF module is reconfigurable in some cases. The power consumption of Arbiter PUF is $25 \mu\text{W}$ and HOA PUF is $2.7 \mu\text{W}$. The uniqueness of the PUF modules is also 51.3 % and 50.3 % which are near the ideal values. These two designs are ideal to be implemented in an appropriate IoT ecosystem to increase security. The future directions of this research include implementing PUF designs that are capable of more reconfigurability and ultra-low power design. Moreover, these designs will be integrated into an IoT ecosystem and a prototype will be designed for further analysis.

9 Acknowledgments

The preliminary research has been presented with the 32nm FinFETs in the following peer-reviewed conference [36] and has been changed to the 14nm FinFETs in the current paper.

References

- [1] S. P. Mohanty. *Nanoelectronic Mixed-Signal System Design*. Number 9780071825719. McGraw-Hill Education, 2015.
- [2] Martin Schuck, Dinushka Orrin Dahanaggamaarachchi, Ben Sprenger, Vedant Vyas, Siqi Zhou, and Angela P. Schoellig. SwarmGPT: Combining Large Language Models With Safe Motion Planning for Drone Swarm Choreography. *IEEE Robotics and Automation Letters*, 10(11):12237–12244, 2025.
- [3] Directorate-General for Research and Innovation. Industry 5.0: A transformative vision for europe. Technical Report KI-BE-21-005-EN-N, European Commission, Luxembourg, January 2022.
- [4] Anthropic. Statement on the us government directive to suspend access to fable 5 and mythos 5. Anthropic, June 2026. <https://www.anthropic.com/news/fable-mythos-access>. Accessed 2026-07-03.

Table 5: Comparison of Results with Related Existing Research.

Research Works	Technology Used	Architecture Used	Average Power Requirement	Hamming Distance (%)
Rahman et al. [33]	90 nm		–	50
Maiti et al. [65]	180 nm	Traditional Ring Oscillator	–	50.72
Garrett et al. [66]	Memristor	Memristor Crossbar	564.83 μ W	49.96
Uddin et al. [67]	Memristor	XORed Memristor Crossbar	450 μ W	50
Suh et al. [68]	–		–	46.15
Maiti et al. [69]	–	–	–	47.31
Mathew et al. [56]	22 nm CMOS	Hybrid Delay Cross Coupled	–	50.14
Suh et al. [54]	90 nm	Ring Oscillator	–	50
Cao et al. [70]	180 nm	CMOS Image Sensor PUF	–	49.37
Yanambaka et al. [71]	32 nm FinFET	Inverter based MKG PUF	251 μ W	48.3
Yanambaka et al. [71]	32 nm FinFET	Current Starved Oscillator	320 μ W	50.9
Nozaki et al. [72]	180 nm	Ring Oscillator PUF	–	63.83
Sahoo et al. [28]	65 nm	Arbiter PUF	–	50.04
Zayed et al. [60]	20nm FinFET	Oscillator Collapse	140 nW - 740 nW	50.01 %
Driemeyer et al. [61]	28-nm CMOS	Hybrid RO/Arbiter PUF	0.259 pJ/bit	51.80 %
Pahlevi et al. [62]	-	Pre-Selection-Enhanced Arbiter PUF	-	10 % - 50 %
Das et al. [63]	45 nm	voltage-gated spin-orbit torque magnetic tunnel junctions (VGSOT-MTJs) based PUF	63.67 fJ/bit	50.20 %
This Paper (Arbiter PUF)	14 nm FinFET	Multiplexer	25 μ W	50.3
This paper (HOA PUF)	14 nm FinFET	Traditional Ring Oscillator	2.7 μ W	51.3

- [5] Swati Khandelwal. Microsoft warns poisoned mcp tool descriptions can make ai agents leak data. The Hacker News, June 2026. <https://thehackernews.com/2026/06/microsoft-warns-poisoned-mcp-tool.html>. Accessed 2026-07-03.
- [6] NVIDIA. Nvidia h200 tensor core gpu. NVIDIA, 2024. <https://www.nvidia.com/en-us/data-center/h200/>. Accessed 2026-07-03.
- [7] Apple Inc. Apple Vision Pro Available in the U.S. on February 2. <https://www.apple.com/newsroom/2024/01/apple-vision-pro-available-in-the-us-on-february-2/>, January 2024. Apple Newsroom, accessed: 2026-07-04.
- [8] Alexandra Sipatchin, Siegfried Wahl, and Katharina Rifai. Eye-Tracking for Clinical Ophthalmology with Virtual Reality (VR): A Case Study of the HTC Vive Pro Eye’s Usability. *Healthcare*, 9(2):180, 2021.
- [9] P. Sundaravadivel, C. Tumwesigye, S. P. Mohanty, and E. Kougianos. imed-tour: An iot-based privacy-assured framework for medical services in smart tourism. In *IEEE International Conference on Consumer Electronics (ICCE)*, pages 1–5, 2020.
- [10] Georgia Institute of Technology. Bad Vibes: AI-Generated Code is Vulnerable, Researchers Warn. <https://research.gatech.edu/bad-vibes-ai-generated-code-vulnerable-researchers-warn>, April 2026. Georgia Tech Research News, accessed: 2026-07-04.
- [11] Google Threat Intelligence Group. GTIG AI Threat Tracker: Adversaries Leverage AI for Vulnerability Exploitation, Augmented Operations, and Initial Access. <https://cloud.google.com/blog/topics/>

- threat-intelligence/ai-vulnerability-exploitation-initial-access/, May 2026. Google Cloud Blog, accessed: 2026-07-04.
- [12] Paul Lamkin, October 2018. <https://www.forbes.com/sites/paullamkin/2018/10/23/smart-wearables-market-to-double-by-2022-27-billion-industry-forecast/#7e5258582656>.
 - [13] P. Sundaravadivel, S. P. Mohanty, E. Kougianos, and U. Albalawi. An Energy Efficient Sensor for Thyroid Monitoring Through the IoT. In *Proceedings of the 17th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE)*, pages 1–4, 2016.
 - [14] Prakash Shrestha and Nitesh Saxena. An Offensive and Defensive Exposition of Wearable Computing. *ACM Comput. Surv.*, 50(6), Nov 2018.
 - [15] B. Ahuja, D. Mishra, and R. Bose. Optimal green hybrid attacks in secure iot. *IEEE Wireless Communications Letters*, 9(4):457–460, 2020.
 - [16] S. Guo, J. Wang, Z. Chen, Y. Li, and Z. Lu. Securing IoT Space via Hardware Trojan Detection. *IEEE Internet of Things Journal*, xx(yy):1–1, 2020.
 - [17] C. Dong, G. He, X. Liu, Y. Yang, and W. Guo. A multi-layer hardware trojan protection framework for iot chips. *IEEE Access*, 7:23628–23639, 2019.
 - [18] Y. Liu and Z. Li. aleak: Context-free side-channel from your smart watch leaks your typing privacy. *IEEE Transactions on Mobile Computing*, xx(yy):1–14, 2019.
 - [19] V. P. Yanambaka, S. P. Mohanty, and E. Kougianos. Making use of manufacturing process variations: A doping-less transistor based-puf for hardware-assisted security. *IEEE Transactions on Semiconductor Manufacturing*, 31(2):285–294, 2018.
 - [20] Venkata P. Yanambaka, Jian Zhang, Jonathan Gratch, and Kahlan Edwards. Puf-ml: Machine learning - based physical unclonable functions for cost effective integration in smart healthcare. In *proceedings of IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, volume 1, pages 1–6, 2025.
 - [21] Seema G. Aarella, Venkata P. Yanambaka, Saraju P. Mohanty, and Elias Kougianos. Fortified-edge 2.0: Advanced machine-learning-driven framework for secure puf-based authentication in collaborative edge computing. *Future Internet*, 17(7):272, 2025.
 - [22] Yongjin Kim and Evan Kim. hTPM: Hybrid Implementation of Trusted Platform Module. In *Proceedings of the 1st ACM Workshop on Workshop on Cyber-Security Arms Race*, pages 3 – 10, 2015.
 - [23] Rashmi Sahay, L. Lakshmi, P. V. Jayavardhana Sai, Maha M. Althobaiti, Amina Salhi, Muhammad Ijaz Khan, and Mirjalol Ismoilov. Trust-Centric Mitigation of Time-Warping Adversarial Attacks in Wearable Sensor Platforms. *IEEE Transactions on Consumer Electronics*, 72(2):4932–4946, 2026.
 - [24] Arm. <https://developer.arm.com/ip-products/security-ip/trustzone>.
 - [25] Zheyuan Ma, Xi Tan, Lukasz Ziarek, Ning Zhang, Shambhu Upadhyaya, Hongxin Hu, and Ziming Zhao. Microft: Exploring and Mitigating Cross-State Control-Flow Hijacking Attacks on ARM Cortex-M TrustZone. *IEEE Transactions on Information Forensics and Security*, 20:12096–12111, 2025.
 - [26] X. Yang, P. Shi, B. Tian, B. Zeng, and W. Xiao. Trust-e: A trusted embedded operating system based on the arm trustzone. In *IEEE 11th Intl Conf on Ubiquitous Intelligence and Computing*, pages 495–501, 2014.
 - [27] S. P. Mohanty, V. P. Yanambaka, E. Kougianos, and D. Puthal. Pufchain: A hardware-assisted blockchain for sustainable simultaneous device and data security in the internet of everything (ioe). *IEEE Consumer Electronics Magazine*, 9(2):8–16, 2020.
 - [28] D. P. Sahoo, D. Mukhopadhyay, R. S. Chakraborty, and P. H. Nguyen. A multiplexer-based arbiter puf composition with enhanced reliability and security. *IEEE Transactions on Computers*, 67(3):403–417, 2018.
 - [29] Peng Zheng, Yi-Bo Liao, Nattapol Damrongplasit, Meng-Hsueh Chiang, and Tsu-Jae King Liu. Variation-Aware Comparative Study of 10-nm GAA Versus FinFET 6-T SRAM Performance and Yield. *IEEE Transactions on Electron Devices*, 61(12):3949–3954, 2014.
 - [30] Meng Li, Xin Xu, Xianghui Li, Yunpeng Li, Yiqun Shi, Qingqing Sun, and Hao Zhu. Aging analysis and degradation prediction of pll circuits in 14-nm finfet technology. *IEEE Journal of the Electron Devices Society*, 13:270–277, 2025.
 - [31] Pintu Kumar Sadhu and Venkata P. Yanambaka. Easy-sec: PUF-based rapid and robust authentication framework for the internet of vehicles. In Deepak Puthal, Saraju Mohanty, and Byeong Yoo Choi, editors, *Internet of Things*, volume 684 of *IFIP Advances in Information and Communication Technology*, pages 262–279. Springer, 2024.

- [32] Venkata K. V. V. Bathalapalli, Saraju P. Mohanty, Chenyun Pan, and Elias Kougianos. QPUF 2.0: Exploring Quantum Physical Unclonable Functions for Security-by-Design of Energy Cyber-Physical Systems. *IEEE Internet of Things Journal*, 12(23):49864–49883, 2025.
- [33] M. T. Rahman, D. Forte, J. Fahrny, and M. Tehranipoor. ARO-PUF: An Aging-Resistant Ring Oscillator PUF Design. In *Proceedings of the Design, Automation Test in Europe Conference Exhibition (DATE)*, pages 1–6, 2014.
- [34] Y. Gao, D. C. Ranasinghe, S. F. Al-Sarawi, O. Kavehei, and D. Abbott. Emerging Physical Unclonable Functions With Nanotechnology. *IEEE Access*, 4:61–80, 2016.
- [35] Kuheli Pratihar, Soumi Chatterjee, Rajat Subhra Chakraborty, and Debdeep Mukhopadhyay. Enhancing SRAM-Based PUF Reliability Through Machine Learning-Aided Calibration Techniques. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 43(11):3491–3502, 2024.
- [36] Venkata P. Yanambaka, Saraju P. Mohanty, and Elias Kougianos. Secure Multi-Key Generation Using Ring Oscillator based Physical Unclonable Function. In *Proceedings of the 2nd IEEE International Symposium on Nanoelectronic and Information Systems (iNIS)*, pages 200–205, 2016.
- [37] Xuyang Lu, Lingyu Hong, and Kaushik Sengupta. Cmos optical pufs using noise-immune process-sensitive photonic crystals incorporating passive variations for robustness. *IEEE Journal of Solid-State Circuits*, 53(9):2709–2721, 2018.
- [38] Shanshan Wang, Xiaowei Zhang, Pengjun Wang, and Xiangyu Li. Design of magnetic sensor array-based pufs for iot security. *IEEE Transactions on Instrumentation and Measurement*, 75:1–9, 2026.
- [39] Takayuki Yamada, Seiichi Gohshi, and Isao Echizen. Privacy Visor: Method for Preventing Face Image Detection by Using Differences in Human and Device Sensitivity. In Bart De Decker, Jana Dittmann, Christian Kraetzer, and Claus Vielhauer, editors, *Communications and Multimedia Security*, pages 152–161. Springer Berlin Heidelberg, 2013.
- [40] Benjamin Henne, Christian Szongott, and Matthew Smith. SnapMe If You Can: Privacy Threats of Other Peoples’Geo-Tagged Media and What We Can Do About It. In *Proceedings of the 6th ACM Conference on Security and Privacy in Wireless and Mobile Networks*, pages 95–106, 2013.
- [41] Roberto Hoyle, Robert Templeman, Steven Armes, Denise Anthony, David Crandall, and Apu Kapadia. Privacybehaviors of lifeloggers using wearable cameras. In *Proceedings of the ACM International Joint Conference on Pervasive and Ubiquitous Computing*, pages 571–582, 2014.
- [42] Ashwin Ashok, Viet Nguyen, Marco Gruteser, Narayan Mandayam, Wenjia Yuan, and Kristin Dana. In proceedings of the 1st acmmobicom workshop on visible light communication systems. In *Do notshare! Invisible Light Beacons for Signaling Preferences To Privacy-Respecting Cameras*, pages 39–44, 2014.
- [43] Nvidia. <http://www.geforce.com/> [Last Accessed on : 6/21/2017].
- [44] Dimitri Kusnezov. Architectural challenges: AI Chips, Decision Support and High Performance Computing. In *IEEE Hot Chips 33 Symposium (HCS)*, pages 1–21, 2021.
- [45] Noah Bean. Intel’s 18A: The Chip That Determines Whether America Has a Semiconductor Industry. <https://medium.com/@noahbean3396/intels-18a-the-chip-that-determines-whether-america-has-a-semiconductor-industry-ce76b536036c>, March 2026. Medium, accessed: 2026-07-04.
- [46] Venkata P. Yanambaka, Saraju P. Mohanty, Elias Kougianos, and Dhruva Ghai. *Nanoscale high- κ /metal gate CMOS and FinFET based logic libraries*, volume 1 of *Nano-CMOS and Post-CMOS Electronics: Devices and Modelling*, chapter 6, pages 169–211. Institute of Engineering and Technology, 2015.
- [47] ARM 7 nm Vega Technology. <https://www.amd.com/en/technologies/vega7nm>.
- [48] E. Kougianos, S. P. Mohanty, G. Coelho, U. Albalawi, and P. Sundaravadivel. Design of a High-Performance System for Secure Image Communication in the Internet of Things. *IEEE Access*, 4:1222–1242, 2016.
- [49] OpenAI. Gpt-5 and gpt-5.3 model family documentation and updates. <https://openai.com>, 2026. Model family release documentation, accessed: 2026-07-04.
- [50] Anthropic. Claude fable 5 / mythos 5 model updates and release information. <https://www.anthropic.com>, 2026. Reported via official announcements and news coverage, accessed: 2026-07-04.
- [51] Google DeepMind. Gemini 3.1 pro: A smarter model for your most complex tasks. <https://blog.google/innovation-and-ai/models-and-research/gemini-models/gemini-3-1-pro/>, February 2026. Official model announcement, accessed: 2026-07-04.

- [52] Microsoft Threat Intelligence. 33 Malicious npm Packages Abuse Dependency Confusion to Profile Developer Environments. <https://www.microsoft.com/en-us/security/blog/2026/05/29/33-malicious-npm-packages-abuse-dependency-confusion-profile-developer-environments/>, May 2026. Microsoft Security Blog, accessed: 2026-07-04.
- [53] Red Hat Product Security. Libvirt Privilege Escalation Vulnerabilities. <https://access.redhat.com/articles/libvirt-privesc-vulnerabilities>, May 2025. Red Hat Customer Portal, accessed: 2026-07-04.
- [54] G. E. Suh and S. Devadas. Physical Unclonable Functions for Device Authentication and Secret Key Generation. In *2007 44th ACM/IEEE Design Automation Conference*, pages 9–14, June 2007.
- [55] Ihtesham Haider, Michael Höberl, and Bernhard Rinner. Trusted Sensors for Participatory Sensing and IoT Applications based on Physically Unclonable Functions. In *Proceedings of the 2nd ACM International Workshop on IoT Privacy, Trust, and Security (IoTPTS 16)*, pages 14–21, 2016.
- [56] S. K. Mathew, S. K. Satpathy, M. A. Anders, H. Kaul, S. K. Hsu, A. Agarwal, G. K. Chen, R. J. Parker, R. K. Krishnamurthy, and V. De. 16.2 A 0.19pJ/b PVT-Variation-Tolerant Hybrid Physically Unclonable Function Circuit for 100% Stable Secure Key Generation in 22nm CMOS. In *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, pages 278–279, Feb 2014.
- [57] A. Maiti and P. Schaumont. Improving The Quality of a Physical Unclonable Function using Configurable Ring Oscillators. In *Proceedings of the International Conference on Field Programmable Logic and Applications*, pages 703–707, 2009.
- [58] Y. Hori, T. Yoshida, T. Katashita, and A. Satoh. Quantitative and Statistical Performance Evaluation of Arbiter Physical Unclonable Functions on FPGAs. In *Proceedings of the International Conference on Reconfigurable Computing and FPGAs*, pages 298–303, 2010.
- [59] Christophe Clavier and Kris Gaj. *Cryptographic Hardware and Embedded Systems*. Springer, 2009.
- [60] Amin A. Zayed, Hanady Hussein Issa, Khaled A. Shehata, and Hani Fikry Ragai. Ultra-Low Power Oscillator Collapse Physical Unclonable Function Based on FinFET. *IEEE Access*, 9:27696–27707, 2021.
- [61] Bjoern Driemeyer, Holger Mandry, David-Peter Wiens, John G. Kauffman, Joachim Becker, and Maurits Ortmanns. An Eye-Opening Arbiter PUF With Auto-Error Detection and PVT-Robust Masking Achieving a BER of $2e-8$. *IEEE Journal of Solid-State Circuits*, pages 1–13, 2026.
- [62] Rizka Reza Pahlevi, Hirokazu Hasegawa, Yukiko Yamaguchi, and Hajime Shimada. A Pre-Selection-Enhanced Arbiter PUF for Strengthening PUF-Based Authentication. *IEEE Access*, 13:127526–127544, 2025.
- [63] Kunal Kranti Das, Aditya Japa, Deepika Gupta, and Brajesh Kumar Kaushik. Energy-Efficient and Attacks Resilient PUF Design Exploiting VGSOT-MTJ. *IEEE Open Journal of Nanotechnology*, 6:153–161, 2025.
- [64] Kirti Bhanushali and W. Rhett Davis. FreePDK15: An Open-Source Predictive Propcess Design Kit for 15nm FinFET Technology. In *Proceedings of the 15th International Symposium on Physical Desing (ISPD)*, pages 165–170, 2015.
- [65] Abhranil Maiti and Patrick Schaumont. Improved Ring Oscillator PUF: An FPGA-friendly Secure Primitive. *Journal of Cryptography*, 24(2):375–397, 2010.
- [66] G. S. Rose and C. A. Meade. Performance analysis of a memristive crossbar PUF design. In *2015 52nd ACM/EDAC/IEEE Design Automation Conference (DAC)*, pages 1–6, June 2015.
- [67] M. Uddin, M. B. Majumder, G. S. Rose, K. Beckmann, H. Manem, Z. Alamgir, and N. C. Cady. Techniques for Improved Reliability in Memristive Crossbar PUF Circuits. In *2016 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, pages 212–217, July 2016.
- [68] G. E. Suh and S. Devadas. Physical Unclonable Functions for Device Authentication and Secret Key Generation. In *Proceedings of the 44th ACM/IEEE Design Automation Conference*, pages 9–14, 2007.
- [69] A. Maiti, J. Casarona, L. McHale, and P. Schaumont. A Large Scale Characterization of RO-PUF. In *Proceedings of the IEEE International Symposium on Hardware-Oriented Security and Trust (HOST)*, pages 94–99, 2010.
- [70] Y. Cao, L. Zhang, S. S. Zalivaka, C. H. Chang, and S. Chen. CMOS Image Sensor Based Physical Unclonable Function for Coherent Sensor-Level Authentication. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 62(11):2629–2640, Nov 2015.
- [71] Venkata P. Yanambaka, Saraju P. Mohanty, and Elias Kougiannos. Novel FinFET based Physical Unclonable Functions for Efficient Security in Internet of Things. In *Proceedings of the 2nd IEEE International Symposium on Nanoelectronic and Information Systems (iNIS)*, pages 172–177, 2016.
- [72] Y. Nozaki and M. Yoshikawa. Quantitative performance evaluation of pl puf and ro puf with asic implementation. In *in Proceedings of IEEE 8th Global Conference on Consumer Electronics (GCCE)*, pages 1127–1128, 2019.

Authors' Biographies



Venkata P. Yanambaka received the Bachelor of Technology degree in Computer Science and Engineering from Priyadarshini College of Engineering and Technology, Nellore, India, the Master of Science degree in Computer Engineering from the University of North Texas, Denton, TX, and the Ph.D. degree in Computer Science and Engineering from the University of North Texas, Denton, TX, in 2019, under the supervision of Dr. Saraju P. Mohanty. His dissertation, titled “Exploring Physical Unclonable Functions for Efficient Hardware Assisted Security in IoT,” was awarded the Best Poster Award at IEEE MetroCon 2017. He is currently an Assistant Professor of Computer Science at Texas Woman’s University, Denton, TX. His research interests are in the Internet of Things (IoT), hardware-assisted security primitives, Physical Unclonable Functions (PUFs), and security in IoT architectures. He has authored over 50 peer-reviewed publications, including multiple journal and transaction articles and a book chapter. He has served as a reviewer for several peer-reviewed journals and conferences. He has been an active member of IEEE since 2012.



Uma Choppali Uma Choppali received her bachelor’s degree in science and education from the Regional Institute of Education, Bhubaneswar, India, in 1999, the master’s degree in physics from the University of South Florida, USA, in 2004, and the Ph.D. degree in materials science and engineering from the University of North Texas, USA, in 2006. She is a Faculty Member with Dallas College (Eastfield Campus), Mesquite, TX, USA. She has authored a dozen research articles. Her Google Scholar H-index is 12 and i10-index is 13 with 2275 citations. She is a regular reviewer of several international journals and conferences.



Saraju Mohanty received the bachelor’s degree (Honors) in electrical engineering from the Orissa University of Agriculture and Technology, Bhubaneswar, in 1995, the master’s degree in Systems Science and Automation from the Indian Institute of Science, Bengaluru, in 1999, and the Ph.D. degree in Computer Science and Engineering from the University of South Florida, Tampa, in 2003. He is a Professor with the University of North Texas. His research is in “Smart Electronic Systems” which has been funded by National Science Foundations (NSF), Semiconductor Research Corporation (SRC), U.S. Air Force, NIDILRR, IUSSTF, and Mission Innovation. He has authored 600 research articles, 5 books, and 10 granted and pending patents. His Google Scholar h-index is 68 and i10-index is 338 with 19,000 citations. He is regarded as a visionary researcher on Smart Cities technology in which his research deals with security and energy aware, and AI/ML-integrated smart components. He introduced the Secure Digital Camera (SDC) in 2004 with built-in security features designed using Hardware Assisted Security (HAS) or Security by Design (SbD) principle. He is widely credited as the designer for the first digital watermarking chip in 2004 and first the low-power digital watermarking chip in 2006. He is a recipient of 21 best paper awards, Fulbright Specialist Award in 2021, IEEE Consumer Electronics Society Outstanding Service Award in 2020, the IEEE-CS-TCVLSI Distinguished Leadership Award in 2018, and the PROSE Award for Best Textbook in Physical Sciences and Mathematics category in 2016. He has delivered 33 keynotes and served on 15 panels at various International Conferences. He has been serving on the editorial board of several peer-reviewed international transactions/journals, including IEEE Transactions on Big Data (TBD), IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), IEEE Transactions on Consumer Electronics (TCE), and ACM Journal on Emerging Technologies in Computing Systems (JETC). He has been the Editor-in-Chief (EiC) of the IEEE Consumer Electronics Magazine (MCE) during 2016-2021. He served as the Chair of Technical Committee on Very Large Scale Integration (TCVLSI), IEEE Computer Society (IEEE-CS) during 2014-2018 and on the Board of Governors of the IEEE Consumer Electronics Society during 2019-2021. He serves on the steering, organizing, and program committees of several international conferences. He is the steering committee chair/vice-chair for the IEEE International Symposium on Smart Electronic Systems (IEEE-iSES), the IEEE-CS Symposium on VLSI (ISVLSI), and the OITS International Conference on Information Technology (OCIT). He has

supervised 3 post-doctoral researchers, 21 Ph.D. dissertations, 29 M.S. theses, and 41 undergraduate projects. received the bachelor's degree (Honors) in electrical engineering from the Orissa University of Agriculture and Technology, Bhubaneswar, in 1995, the master's degree in Systems Science and Automation from the Indian Institute of Science, Bengaluru, in 1999, and the Ph.D. degree in Computer Science and Engineering from the University of South Florida, Tampa, in 2003. He is a Professor with the University of North Texas. His research is in "Smart Electronic Systems" which has been funded by National Science Foundations (NSF), Semiconductor Research Corporation (SRC), U.S. Air Force, NIDILRR, IUSSTF, and Mission Innovation. He has authored 600 research articles, 5 books, and 10 granted and pending patents. His Google Scholar h-index is 68 and i10-index is 338 with 19,000 citations. He is regarded as a visionary researcher on Smart Cities technology in which his research deals with security and energy aware, and AI/ML-integrated smart components. He introduced the Secure Digital Camera (SDC) in 2004 with built-in security features designed using Hardware Assisted Security (HAS) or Security by Design (SbD) principle. He is widely credited as the designer for the first digital watermarking chip in 2004 and first the low-power digital watermarking chip in 2006. He is a recipient of 21 best paper awards, Fulbright Specialist Award in 2021, IEEE Consumer Electronics Society Outstanding Service Award in 2020, the IEEE-CS-TCVLSI Distinguished Leadership Award in 2018, and the PROSE Award for Best Textbook in Physical Sciences and Mathematics category in 2016. He has delivered 33 keynotes and served on 15 panels at various International Conferences. He has been serving on the editorial board of several peer-reviewed international transactions/journals, including IEEE Transactions on Big Data (TBD), IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), IEEE Transactions on Consumer Electronics (TCE), and ACM Journal on Emerging Technologies in Computing Systems (JETC). He has been the Editor-in-Chief (EiC) of the IEEE Consumer Electronics Magazine (MCE) during 2016-2021. He served as the Chair of Technical Committee on Very Large Scale Integration (TCVLSI), IEEE Computer Society (IEEE-CS) during 2014-2018 and on the Board of Governors of the IEEE Consumer Electronics Society during 2019-2021. He serves on the steering, organizing, and program committees of several international conferences. He is the steering committee chair/vice-chair for the IEEE International Symposium on Smart Electronic Systems (IEEE-iSES), the IEEE-CS Symposium on VLSI (ISVLSI), and the OITS International Conference on Information Technology (OCIT). He has supervised 3 post-doctoral researchers, 21 Ph.D. dissertations, 29 M.S. theses, and 41 undergraduate projects.