iVAMS 3.0: Hierarchical-Machine-Learning-Metamodel-Integrated Intelligent Verilog-AMS for Ultra-Fast, Accurate Mixed-Signal Design Optimization

A Preprint

Saraju P. Mohanty
Department of Computer Science and Engineering
University of North Texas
saraju.mohanty@unt.edu

Elias Kougianos
Department of Electrical Engineering
University of North Texas
elias.kougianos@unt.edu

June 1, 2025

Abstract

Analog/Mixed-Signal (AMS) circuits and systems continually present significant challenges to designers with the increase of design complexity and aggressive technology scaling. This is due to the large number of design factors and parameters that must be taken into account as well as the process variations which are prominent in nano-CMOS circuits. Design optimization techniques that account for process variations while presenting an accurate and fast design flow which can perform design optimization in reasonable time are still lacking. Even with techniques such as metamodeling that aid the design phase, there is still the need to improve them for accuracy and time cost. As a trade-off of the accuracy and speed, this paper presents a process-variation aware design flow for ultra-fast variability-aware optimization of nano-CMOS based physical design of analog circuits. It combines a Kriging bootstrapped Artificial Neural Network (ANN) metamodel with a Particle Swarm Optimization (PSO) based algorithm in the design optimization flow. The Kriging bootstrapped ANN metamodel provides a trade-off between analog-quality accuracy and scalability and can be effectively used for large and complex AMS circuits while capturing the correlation in process variations. Kriging captures correlated process variations of the circuits and accurately trains the ANN to generate the metamodels. The proposed technique uses Kriging to bootstrap target samples used for the ANN training. This introduces Kriging characteristics, which account for correlation effects between design parameters, to the ANN. The effectiveness of the design flow is demonstrated using a 180nm CMOS based PLL as a case study with as many as 21 design parameters. It is observed that the bootstrapped Kriging metamodeling is 24× faster than simple ANN metamodeling. The layout optimization for such a complex circuit can be performed effectively in a short time using this approach. The optimization flow could achieve significant reductions in the mean and standard deviation of the PLL characteristics. Thus, the proposed research is a major contribution to design for cost.

Keywords Metamodeling, Machine Learning, Geostatistics, Kriging, Bootstrap Techniques, Artificial Neural Networks (ANN), Phase-Locked Lopp (PLL), Nano-CMOS, Process Variation, Mixed-Signal Circuit, Particle Swarm Optimization

1 Introduction

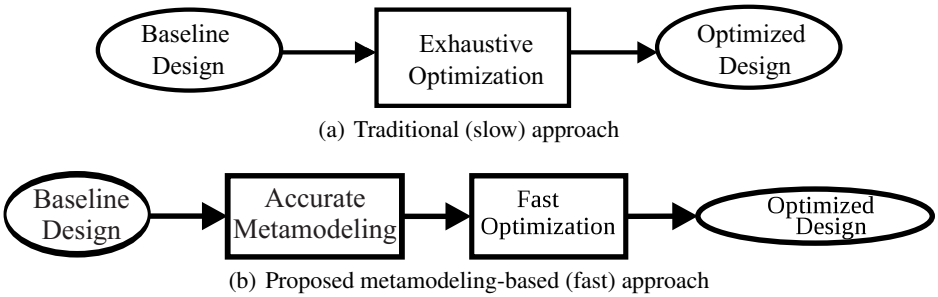
The development and improvement of metamodeling, (or surrogate) techniques have been gradually increasing in recent years. Significant research has been published on various metamodeling techniques for nano-CMOS applications [1, 2]. The goal has been to develop accurate metamodels with lower computational time costs. Extensive research work exploring polynomial, artificial neural network (ANN) and Kriging techniques have been presented

in [3, 4]. ANNs are appealing because of their high accuracy and relative time efficiency. However, with the aggressive scaling of integrated circuit design, the number of design and process parameters that must be taken into consideration for design space exploration also increases.

The design of Analog/Mixed signal (AMS) systems continues to present significant challenges. Especially in design optimization, considerable time must be spent on exploring the design space to achieve optimal designs that are robust and tolerant to the effects of process variation. This required design time is however infeasible in the face of current time-to-market constraints. For example the simulation of a PLL with full parasitics can take several days or weeks of SPICE runs for a complete space exploration. Metamodeling design techniques are used to aid the design process by reducing the design time while maintaining accuracy. There still is a need to improve the metamodels currently used to increase time efficiency and accuracy.

In order to obtain an optimal design, a designer can optimize the actual circuit model (a SPICE netlist). This optimization on the actual circuit (Fig. 1(a)) is very slow and may be even impossible for complex and nanoscale circuits with large numbers of transistors and interconnects. For fast, yet accurate design optimization of analog circuits this paper proposes the approach demonstrated in Fig. 1(b). In this approach, metamodels of the circuit model are first generated. The circuit optimization is then performed on the metamodels instead of the actual circuit. This makes the design exploration fast and accurate. It may be noted that *metamodeling is not macromodeling*. Macromodels are reduced complexity models but they rely on the same type of modeling and simulator as the original models (e.g., SPICE). In the *metamodeling approach, the underlying system is completely decoupled from the simulator and the resulting metamodel (i.e., mathematical model of the circuit) is more general, flexible and easier to simulate and optimize than macromodels*. Macromodels are typically simplified versions of the circuit which are used in the same simulation tool and are hard to create. A metamodel has the following attributes:

1. It is a mathematical representation of the circuit output.
2. It is a prediction equation.
3. Metamodels can be used in a variety of tools, such as MATLAB®, and are language independent.



(a) Traditional (slow) approach

(b) Proposed metamodeling-based (fast) approach

Figure 1: Fast design space exploration of analog circuits through accurate metamodeling.

Kriging based techniques for generating metamodels [5–8] take into account the correlation between process and circuit parameters and also incorporate a stochastic component that mitigates the deterministic nature of computer simulations, hence producing a more accurate statistical representation of the modeled circuit. The disadvantage of Kriging is that each point is predicted with a set of unique weights leading to time inefficient metamodel generations on large design spaces. ANN generated metamodels on the other hand are more time efficient for simulations. In this paper we propose a metamodeling based design approach that combines the benefits of Kriging with the accuracy and time efficiency of ANN models to produce accurate metamodels which are also more effectively process aware. Kriging is used to bootstrap the design samples used for training the ANN models, thus introducing a process aware component into the training set. We show that the Kriging trained ANN models are more process aware accurate than the bare ANN models.

We also present a process aware design flow that incorporates into different levels of the design process techniques to account for the effects of process variation. It combines a Kriging bootstrapped ANN metamodeling technique with a Particle Swarm Optimization (PSO) algorithm [9, 10] in the design optimization flow. The effectiveness of the design flow is shown using a PLL as a case study. PSO techniques are part of genetic, evolutionary, and population based algorithms. In using PSO to train ANN models, the PSO aims to optimize the set of design parameters that are fed into the training of the ANN models. This modification hence improves the selection of parameters from the training set, thus resulting in a faster and more efficient training of the ANN models. While the case-study has been presented with

PSO optimization in the current paper, the use of other similar optimization algorithms is possible. While PSO and Neural Network (NN) metamodels have demonstrated increased accuracy [11], certain design factors such as device parameter variations continue to pose a significant concern to circuit performance estimation. Analog circuits are particularly sensitive and hence prone to these effects [12].

Finally, this work should be placed within the general framework of Digital Twins (DT) in the context of the semiconductor space [13]. DTs are models that encompass the entire life cycle of an electronic product, such as, but not limited to, integrated circuits (IC). Our work is specific to IC design and as such could form a component of a DT but would not supersede it.

This paper is organized as follows: Section 2 highlights the novel contribution of this work. Section 3 contains a brief discussion on current related research. The proposed design optimization flow methodology is presented in section 4. The Kriging-bootstrapped metamodeling process is described in Section 6. Section 7 discusses the optimization algorithm used. Experimental results are presented in section 10. Finally, in section 11 a summary conclusion and future research ideas are presented.

2 Novel Contributions of the Current Paper

The overall contribution of this paper is an ultra-fast, accurate statistical design exploration flow that combines Kriging bootstrapped neural network metamodels and particle swarm optimization to advance the state-of-art in design for cost. This is due to significant reduction in the design cycle time which leads to decrease in non-recurrent design cost of the chip. This paper presents the following *novel contributions* to the state-of-the art of analog/mixed-signal CAD:

1. Fast and accurate physical design and optimization flow incorporating process awareness in analysis, characterization and optimization of performance measures.
2. Process-variations aware accurate and scalable metamodeling using Kriging bootstrapped Neural Networks.
3. Adaptation of the PSO algorithm for nano-CMOS based process-variation aware optimization.
4. A case study exploration using a 180 nm CMOS based PLL design.

It may be noted that a generic overview of Kriging metamodeling is presented in [14]. A Kriging metamodel approach for process variation analysis is presented in [15]. The current paper presents a natural progression of our research to ultra-fast physical design optimization of large analog blocks through the use of Kriging metamodeling.

3 Related Prior Research

Related research in the context of this work includes the design and formulation of modeling and metamodeling techniques to improve the accuracy of such models and simultaneously reduce design exploration time. Polynomial regression methods which include response surface methodology (RSM) [16–18] are one of the most common and reliable methods explored. However, low order polynomial regression techniques are not very accurate for global design space exploration [19, 20]. They assume a random error between design variables while in the presence of process variations, these errors may be correlated, especially in deep nanometer process technology. Non-polynomial based metamodels, particularly built from Neural Network training have also been reported to surpass polynomial regression techniques [21–24]. NN techniques use a learning process to continuously train weights used in approximating these models. The weight training process is critical in the development of NN models and research in exploring techniques for optimizing this process is currently active. A technique popularly used is applying optimization algorithms to optimize the weight training of NN models [11]. Use of Kriging training for the NN architecture provides a trade-off between the accuracy of Kriging and scalability of the NN method [15]. In the current paper, we propose to infuse the characteristics of Kriging based techniques by bootstrapping the sample data points which are then used for the NN training process. We believe that the bootstrapped data points enhance the modeling of process variation effects.

Monte Carlo (MC) simulations methods have been a reliable and effective method for yield analysis of designs. Multiple simulations of the modeled circuit are run while varying the design and process parameters (transistor length, transistor width, supply voltage, thickness oxide, etc.) to reflect the effect of process variations. In [12] hierarchical statistical analysis and regression based techniques have been explored for variation analysis. The proposed Kriging bootstrapped NN model is analyzed for statistical variation using the MC method.

4 Process Variation Aware Ultra-Fast Design Optimization Flow for Mixed-Signal Circuits

We propose a novel design flow that integrates a Kriging bootstrapped metamodeling process with the PSO algorithm for the design optimization of nano-CMOS circuits as, depicted in Fig. 2. The key idea is to generate a Kriging surface

using a small number of analog simulations with latin hypercube sampling (LHS) of the variables. An NN architecture is then trained to create a metamodel of the baseline circuits. Statistical analysis and optimization is performed over the metamodel instead of its SPICE netlist. The use of metamodels for design optimization iterations significantly speeds up the design-optimization process and analog-level accuracy is maintained by the use of accurate metamodels which are generated from the parasitic-aware netlist.

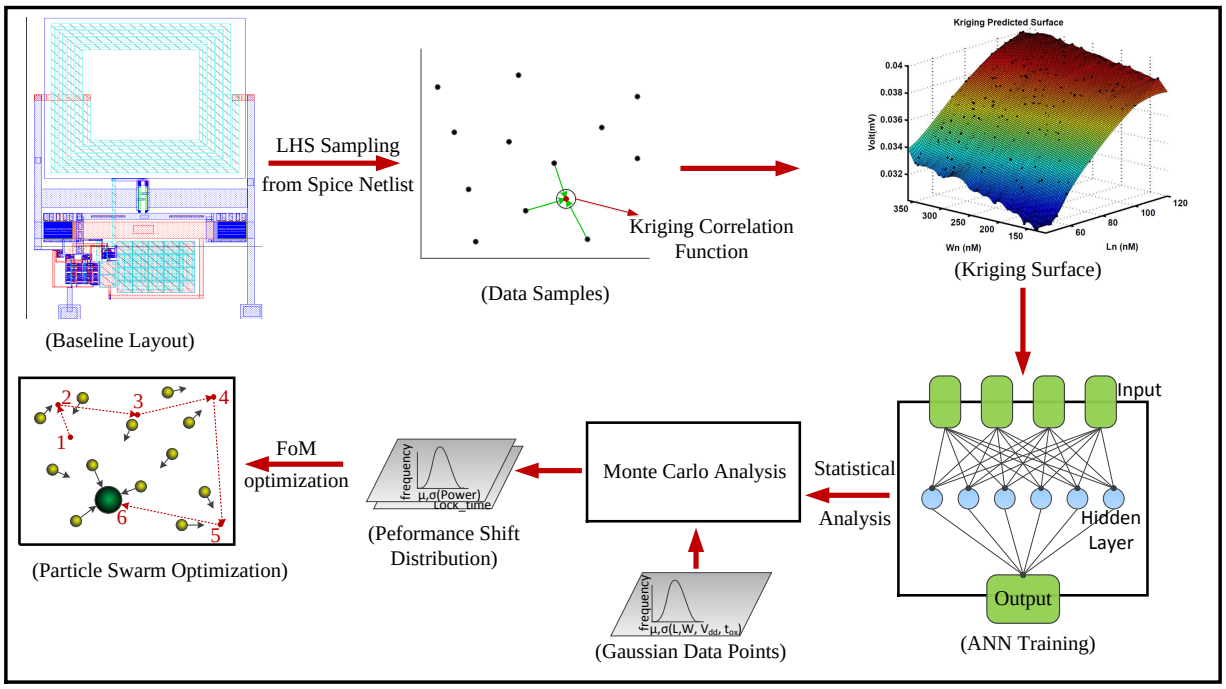


Figure 2: Proposed high level design flow with Hierarchical Machine Learning Modeling [25].

The overall flow of the design process shown in Fig. 3 highlights the major phases of the design flow. The first phase labeled "A" consists of the baseline logical and physical design. In this phase, the baseline design is drawn both as a circuit schematic and the associated layout. The baseline is simulated for functional verification of the performance objectives. The functional verification also serves to characterize the circuit design objectives which are defined in Section 8. The next phase involves the creation of the process variation aware metamodel of the circuit design. The first step in this phase is the identification and parameterization of the variables used to create the metamodel from the extracted parasitic netlist. Incorporating the process parameters early on in the design phase ensures a process variation aware metamodel. An LHS of the circuit from the parasitic netlist is then used by Kriging techniques to bootstrap the sample data points infusing process variation characteristics. We detail this process in Section 6. The Kriging bootstrapped points are used for the NN Training. The final phase is the process aware design optimization. The optimization algorithm is used together with the created metamodel and design objectives as an input to optimize the design. The final design parameters are then used to update the physical design for an optimal design of the circuit. The process aware design optimization phase is discussed in detail in Section 7.

The use of bootstrapping Kriging with ANN improves both the accuracy and speed of the design flow process. Bootstrapping Kriging techniques ensure process aware accuracy while ANN metamodeling techniques have been shown to be very fast. The overall design flow metamodel incorporates process variation awareness in the design metamodeling phase and the design optimization phase.

5 Proposed Kriging Bootstrapped Artificial Neural Network (ANN) Metamodeling

In this section, we introduce and discuss the proposed Kriging bootstrapped Artificial Neural Network metamodeling technique. First we briefly introduce traditional Kriging and Artificial Neural Network metamodeling and then discuss our proposed modifications. Our proposed kriging bootstrapped ANN metamodeling technique is shown in Fig. 4.

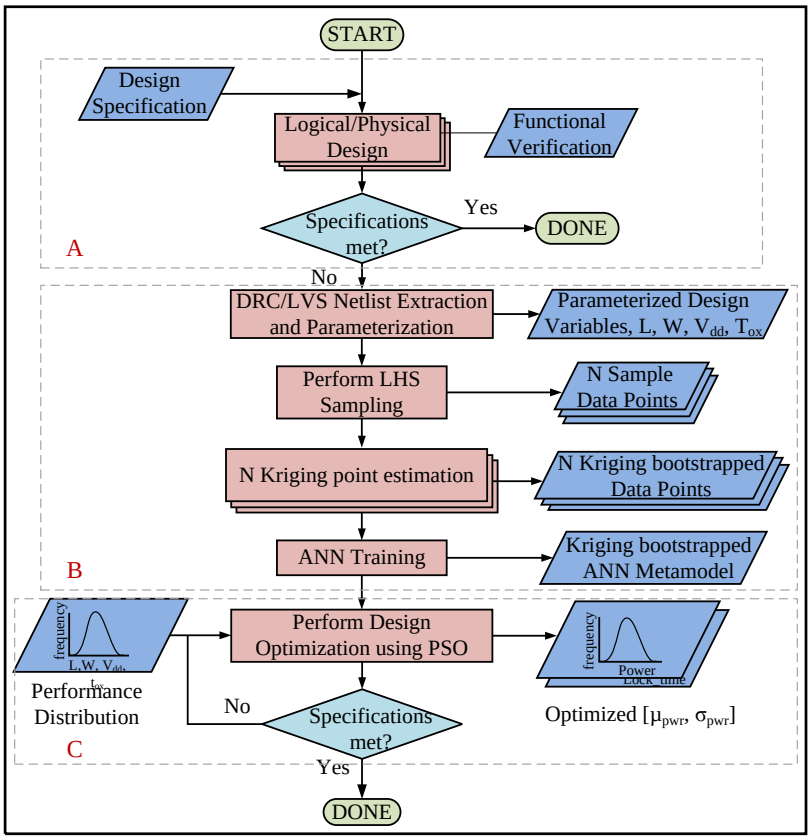


Figure 3: Proposed design optimization flow [25].

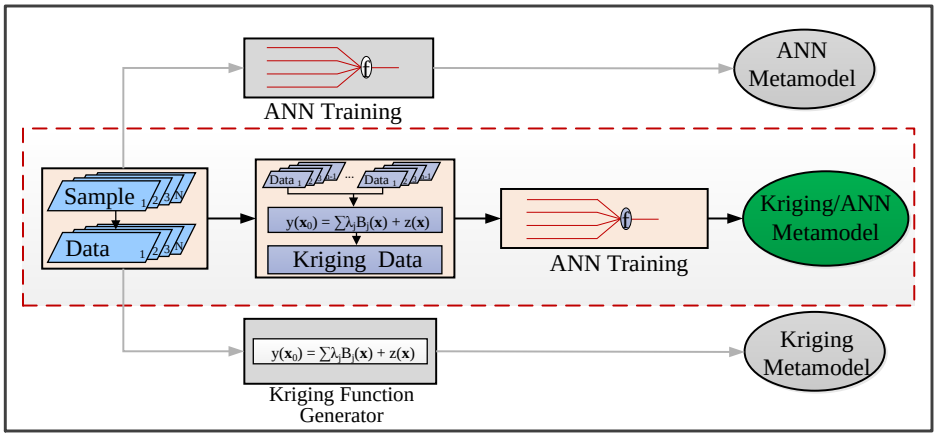


Figure 4: Proposed Kriging Bootstrapped ANN Metamodel Generation Flow [15].

5.1 Kriging Based Metamodeling

Kriging prediction techniques were originally applied in geostatistics but have since been explored for other applications such as circuit design [6–8]. Kriging metamodeling combines polynomial regression with a stochastic approach to mitigate the deterministic nature of computer simulations. The Kriging equations can be expressed in the form of the following:

$$y(\mathbf{x_0}) = \sum_{j=1}^{L} \lambda_j B_j(\mathbf{x}) + z(\mathbf{x}), \tag{1}$$

where $y(\mathbf{x_0})$, is a stochastic function which predicts the response y at the design point $(\mathbf{x_0})$. $\{B_j(\mathbf{x}), j = 1, \cdots, L\}$ is a specific set of basis functions over the design domain D_N and λ_j are fitting coefficients (also known as weights) to be determined based on the Kriging method applied. $z(\mathbf{x})$ is a stochastic process with zero mean and is based on a spatial correlation function.

In calculating the weights λ_j for estimating Kriging functions, the autocorrelation between the input parameters is accounted for and characterized by the covariance function of the following form [26]:

$$r(\mathbf{s}, \mathbf{t}) = \mathrm{Corr}(z(\mathbf{s}), z(\mathbf{t})). \tag{2}$$

This property of Kriging prediction is exploited to model the effects of process variation on circuit metamodels. The correlations between the process variation of the design and process parameters are taken into consideration in calculating the weights for the metamodel functions. The drawback of Kriging is that the weight for each predicted point is unique and involves matrix calculations which could become time intensive for a large design space.

5.2 Artificial Neural Network Metamodeling

ANN models consist of simple computational elements with rich interconnections between the elements. They are modeled after biological neural networks which operate in a parallel and distributed fashion. The neural networks create models over a set of inputs by training the weights of the interconnections. Multilayer and radial neural networks are few of the commonly employed neural networks. The multilayer network which is used in this work uses a combination of non-linear activation functions in a hidden layer and a linear activation function in the output layer. The linear layer of the function output can be expressed as follows:

$$v_i = \sum_{i=1}^{s} w_{ji} x_i + w_{j^0}, \tag{3}$$

where w_{ji} is the weight of the connection between the jth element in the hidden layer and the ith component in the input layer x_i and w_{j^0} is a constant bias [27]. The input layer is represented using a sigmoid function such as the following:

$$b_j(\nu_i) = \tanh(\lambda v_j). \tag{4}$$

The neural network utilizes an algorithm (a training function) that updates the weights and biases of the interconnections to minimize the error between the predicted point and the actual response. For this work, the ANN metamodel was created using a MATLAB®toolbox which implements the Levenberg-Marquardt optimization algorithm [28].

5.3 Kriging Bootstrapped ANN Metamodeling

Metamodeling techniques based on Kriging prediction have been explored in [7,17]. In estimating performance points, Kriging prediction techniques take into account the correlation effects between design parameters. This characteristic is very appealing and can be used to model the correlation effects between design parameters due to process variation for design processes deep in the nanometer range. The drawback to Kriging based techniques is that the weights used for each point prediction are unique and have to be calculated for each performance point to be estimated using linear algebra calculations (mostly matrix inversion). This can lead to potential time consuming metamodel generation for high dimensional designs and very large design spaces. Artificial Neural Network (ANN) training, which has also been presented for NanoCMOS metamodeling in [27], has been shown to be robust and accurate for high dimensional models [21]. While ANN also produces highly accurate models, it does not effectively model process variation effects with correlations present.

Hence, the proposed metamodeling technique aims to combine Kriging and ANN to generate accurate models which account for the effects of correlated process variation in a fast and efficient manner. Fig. 4 highlights the already presented methods for ANN and Kriging metamodel generation. For each method sample data points are generated

using a Latin Hypercube Sampling (LHS) design and then are either fed into an ANN trainer or a Kriging function generator. In the proposed metamodel generation method, the sample data points are fed into a Kriging generator that produces an intermediate set of sample data points (bootstrapped) which are then fed into the ANN trainer. This method feeds the ANN trainer Kriging generated sample data points which are process and correlation aware. We demonstrate that using the Kriging generated sample data points will result in a more robust metamodel which is process variation aware and also less time intensive.

The methodology for the generation of the proposed metamodel-based design flow is shown in Fig. 5. The first step involves creating a SPICE netlist of the design. The functional simulation of the circuit schematic is performed to ensure the SPICE model meets design specifications. The physical layout design is also constructed using Design Rule Check (DRC) and Layout vs. Schematic (LVS) verification to ensure a match to the circuit schematic. The physical layout design is used to generate a silicon-aware accurate model (netlist). The performance of the physical design is often degraded due to the parasitic effects. A fully extracted parasitic netlist, including resistance (R), capacitance (C) and self (L) and mutual inductance (K) is used to ensure silicon-level accuracy.

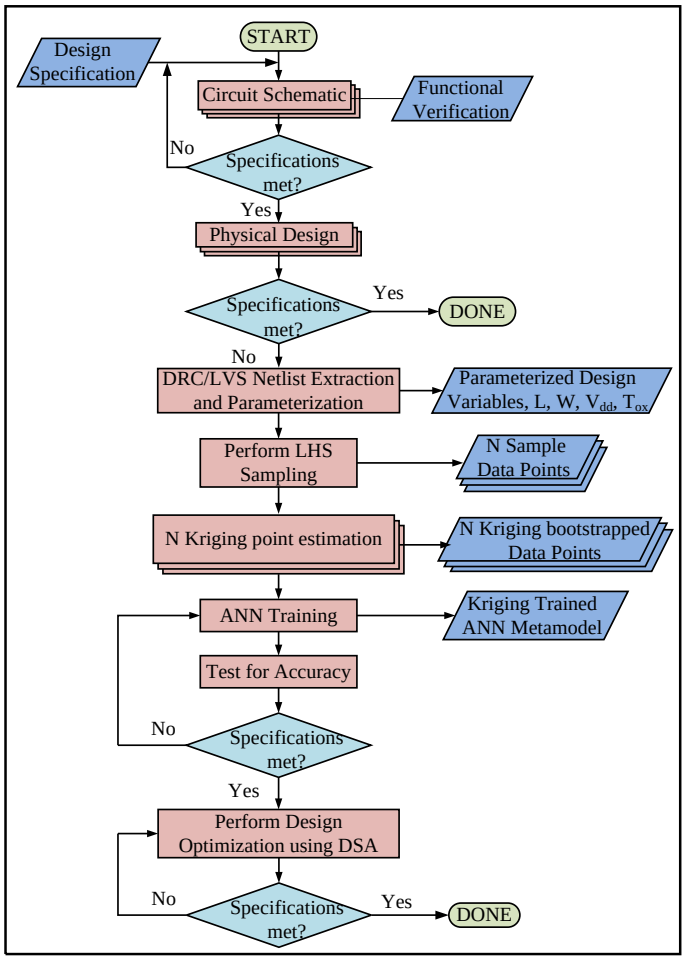


Figure 5: Proposed Metamodel Design Flow [15, 25].

The generation of the metamodel is based on the extracted parasitic $RCLK$ netlist. In order to generate data sample points, the extracted parasitic netlist is parameterized for the design and process variables and then simulated to eliminate the strenuous task of physically varying the design parameters on the physical layout design. The Latin Hypercube Sampling technique is used in the proposed method to vary the design and process parameters. LHS methods generate N random sample points from a given design space. They divide the design space into equal intervals and then randomly select design points from an interval in such a way that each interval appears once in a row-column matrix of the design space. Several techniques may be used to select the data points including uniformly, midpoints or randomly. We use Random LHS which has been reported to generate more accurate models [3]. The

LHS parameter points are used as inputs to the parameterized netlist to generate corresponding performance outputs (data point) for each sample point.

The next step in the metamodeling process is the Kriging bootstrapping of the data points. The generated sample points are fed into a Kriging metamodel generator. We implement the Kriging metamodel presented in our previous work [reference removed] for this process. We generate N Kriging bootstrapped data points by using $N-1$ points and the Kriging method to estimate the Nth point. N iterations of this process will generate N Kriging bootstrapped data points which are then used for the ANN training.

The ANN training process is used to create metamodels for each performance objective (Figure-of-Merit or FoM) characterized for the design. In this research, 4 metamodels were created for the Phase Locked Loop (PLL) circuit described in Section 8.

The final step of the metamodel design flow is the verification and test of accuracy of the generated metamodel. The statistical metric used to verify the accuracy is the Root of Mean Square Error (RMSE). The expression of the RMSE is given as follows:

$$RMSE = \sqrt{\frac{1}{N}\sum_{i=1}^{N}\left(Y_i - \widehat{Y}_i\right)^2}, \tag{5}$$

where N is the number of sampled points, Y_i is the "true" circuit response (SPICE simulation results) and $\widehat{Y}_i$ is the metamodel predicted response. The RMSE measures the difference between the metamodel and the SPICE model where a smaller value indicates a more accurate model.

6 The Proposed Process-Variation Aware Kriging Bootstrapped Metamodeling

The metamodeling technique incorporates Kriging to infuse process variation characteristics to the sampled data. Kriging by itself has been successfully used for metamodel generation with high accuracy [17]. The property of Kriging which makes it very appealing and lends to its high accuracy is its ability to take into account the correlation between the input parameters in performance point prediction. This can be effectively utilized to model the correlation between the process parameters which also serves as input in the sample data point bootstrapping.

In Kriging, the weights are chosen to minimize the variance under the unbiasedness constraint that $E(\widehat{y}(x)-y(x)) = 0$, where $\widehat{y}(x)$ is the predicted response at point x and $y(x)$ is the true response. Hence the weights are chosen so that the following expression is satisfied:

$$\sum_{j=1}^{n}\lambda_j = 1. \tag{6}$$

The weights then are given by the following:

$$\begin{pmatrix}\lambda_1\\ \vdots\\ \lambda_n\\ \mu\end{pmatrix} = \Gamma^{-1}\begin{pmatrix}\gamma(e_1,e_0)\\ \vdots\\ \gamma(e_n,e_0)\\ 1\end{pmatrix}, \tag{7}$$

where μ is a Lagrange multiplier used to ensure equation (6). Γ is the covariance matrix of the observed points and for ordinary Kriging is given by:

$$\Gamma = \begin{pmatrix}\gamma(e_1,e_1) & \cdots & \gamma(e_1,e_n) & 1\\ \vdots & \ddots & \vdots & 1\\ \gamma(e_n,e_1) & \cdots & \gamma(e_n,e_n) & 1\\ 1 & 1 & 1 & 0\end{pmatrix}, \tag{8}$$

where

$$\gamma(e_1,e_2) = E\left(|z(e_1)-z(e_2)|^2\right). \tag{9}$$

A disadvantage of Kriging is that it uses a set of matrix equations in calculating the unique weights for point predictions. For large circuits and high dimensional designs, the time cost can become expensive. The use of NN on the other hand can generate metamodels which are ultra-fast and robust in accuracy. The NN models however do not efficiently model the effects of process variation. To ensure accuracy and time efficiency as well, we present a Kriging bootstrapped metamodeling technique that combines the accuracy of Kriging with the speed of NN models.

The metamodel generation process takes in sample data from the extracted parasitic netlist. The sample data points are fed into the Kriging metamodel generator for resampling of the data (bootstrapping). We generate N Kriging bootstrapped data points by using $N-1$ points and the Kriging method to estimate the Nth point. N iterations of this process will generate N Kriging bootstrapped data points which are then used for the NN training. The NN training process is used to create metamodels for each performance objective (Figure-of-Merit or FoM) for the design. In this work, 4 metamodels were created for the PLL circuit described in section 10.

7 Particle Swarm Optimization (PSO) Algorithm for Process-Variation Aware Optimization

This Section presents a detailed discussion on the proposed particle swarm optimization (PSO) algorithm which performed statistical design exploration over the bootstrapped Kriging metamodels.

7.1 Particle Swarm Optimization (PSO) Algorithm

PSO is a type of evolutionary swarm intelligence algorithm for numerical optimization problems. Swarm intelligence algorithms are based on the exploitation of social or communal behavior of naturally or artificially occurring agents to collectively search for solutions. While heuristic in nature and based on social behaviors, swarm intelligence algorithms have proved to be very effective in optimization [29–31], and circuit design [32, 33].

PSO uses candidates of solutions termed "particles" and modeled after movement of organisms in bird flocks or fish schools, hence the term swarm. The PSO algorithm models the swarm like motion to implement a collective search algorithm, where the particles correspond to search agents which explore different habitats based on the quality of previous solutions. The quality of the results is expressed through the position and velocity of the particles. The particle's movement are updated based on its previous solution (local intelligence) and are also influenced by the global best known solution. Reiterative updates of the particles swarm towards the best solution.

7.2 Process-Variation Aware Adaptation of Particle Swarm Optimization (PSO) Algorithm

The optimization problem implemented in this flow is to minimize the power consumption of the PLL circuit using the locking time as a design constraint. The process aware optimization of the circuit involves minimizing the mean μ and standard deviation σ of the optimal power consumption. As a specific example, the optimization function can be expressed as follows:

$$\text{Minimize}[\mu_{pwr} + 3\sigma_{pwr}], \tag{10}$$

while subjected to locking time constraint. The PSO algorithm for the PLL is shown in Algorithm 1. Fig. 6 presents an illustration of the algorithm.

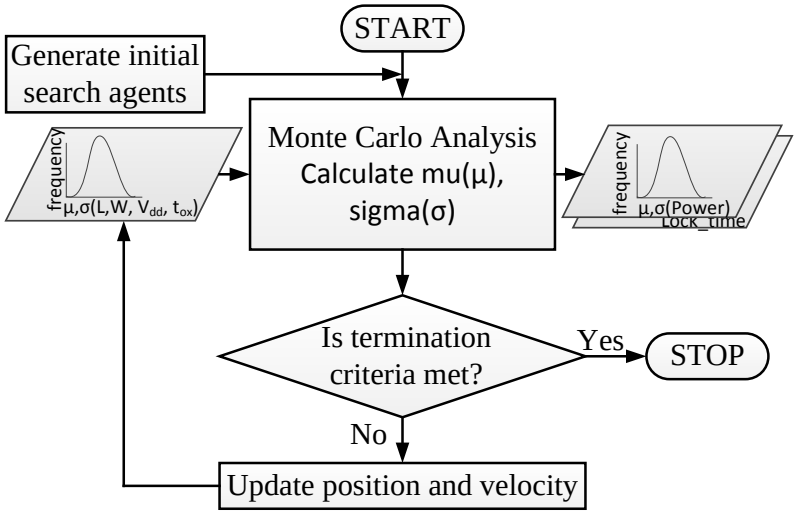


Figure 6: Flow diagram for the PSO algorithm [25].

Algorithm 1: Particle Swarm Optimization of PLL over the Metamodels [25].

Input: Tuning parameter set X, Bootstrapped Kriging metamodels, Tuning parameter ranges.
Output: $X = (x_1, x_2, ..., x_n)$ parameter set with optimized statistical performance;

begin
  SET: N, number of particles;
  SET: Max$_{iteration}$, counter $\longleftarrow$ 0;
  SET: local best $l_{x_i} \longleftarrow$ current position;
  SET: global best $g_{x_i} \longleftarrow$ current position;
  Initialize: weight for swarm effect ϱ;
  Initialize: velocity for swarm effect w;
  while *counter* $<$ *Max*$_{iteration}$ **do**
    foreach *N* **do**
      Monte Carlo analysis over metamodels with nominal x_i;
      $v_i = wv_i + \varrho_p\tau_p(lx_i - x_i) + \varrho_g\tau_g(gx_i - x_i)$;
      $x_i \leftarrow x_i + v_i$;
      if $x_i < l_{x_i}$ **then**
        $l_{x_i} \leftarrow x_i$;
        if $l_{x_i} < g_{x_i}$ **then**
          $g_{x_i} \leftarrow l_{x_i}$;

Result: Parameter set X with minimized μ, σ;

8 Case Study Circuit: A 180nm CMOS PLL

The phase locked loop (PLL) is a closed feedback loop circuit system whose output signal is locked to a reference input signal. The PLL is a critical component in many Analog/Mixed Signal (AMS) systems including processors, telecommunication devices, Field-Programmable Gate Arrays (FPGAs), controllers and many other systems. The system level diagram of a PLL shown in Fig. 7 shows the major components of the PLL which include the phase detector, the charge pump/loop filter, the voltage controlled oscillator (VCO) and the frequency divider.

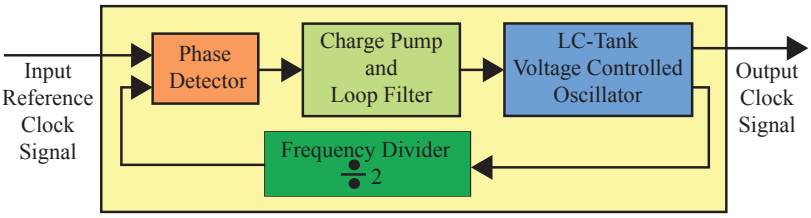


Figure 7: High level system diagram for the PLL.

The reference clock feeds the input signal to the phase detector, which compares and detects the phase difference between the input signal and the output from the VCO. The charge pump generates a supply charge in proportion to the error detected in the phase difference. The generated signal is then filtered by the loop filter to produce a control signal which the VCO uses to produce an output signal which is locked to the reference input signal. The divider is an optional component of the PLL which is used to generate an output signal which is a multiple of the reference input signal.

The schematic and physical layout design of the PLL using a 180 nm CMOS technology was produced on the CADENCE®Virtuoso platform. Figure 8 shows the physical layout of the design.

The PLL was characterized for power consumption, frequency output, locking time and jitter. The baseline design values are shown in Table 1. The FoMs selected are Power (P_{PLL}), Frequency (F_{PLL}), Locking time (Lck_{PLL}), and Jitter (J_{PLL}). The design objective is the minimization of power consumption using the locking time as optimization cost and 21 parameters as design variables.

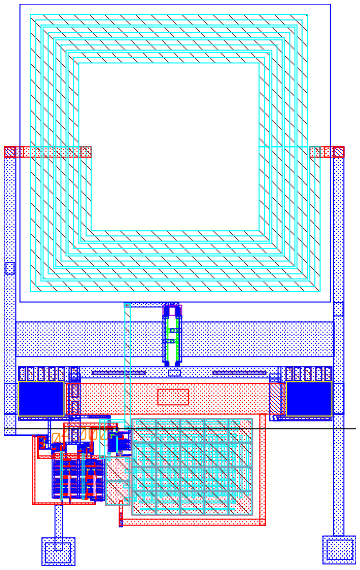


Figure 8: Physical design of the 180 nm PLL [15].

Table 1: Characterization of PLL for Figures of Merit (FoM) [15].

PLL Circuit	Power P_{PLL}	Frequency F_{PLL}	Locking Lck_{PLL}	Jitter J_{PLL}
Layout	2.48 mW	2.66 GHz	5.51 μs	16.80 ns

9 Process Variation Aware Statistical Analysis

In this section we perform a process variation aware statistical analysis of the generated Kriging trained ANN metamodel. Monte Carlo simulation experiments are a common method for the analysis of process variation on analog circuits in order to estimate the yield and efficiency of the design. Monte Carlo analysis enables an efficient investigation of the design space by randomly generating a distribution test case of design variables. The set of test cases form a given probability distribution with a mean of the nominal value of the variable. This is particularly efficient in high dimensional designs where a test case simulation time increases exponentially. For example, in our PLL case study circuit which has 21 design and process parameters, even a high and low test case will require 2^{21} simulations.

The selection of design and process parameters significantly affects the accuracy of the analysis. A sensitivity test is usually performed to select parameters which are most sensitive to performance measure. Reported research [12,34,35] shows that the length (L_n, L_p), width (W_n, W_p) and oxide thickness (T_{ox}) have a significant effect on the performance shift. L_n, L_p, W_n, W_p for the various sub-circuit components of the PLL have been used as design parameters. The nominal values are selected from the baseline design in Section 8 and a Gaussian distribution with 10 % standard deviation is used to generate the sample set for the metamodel simulation. Fig. 9 summarizes the statistical analysis process. $N = 1000$ Monte Carlo simulations are performed for each FoM.

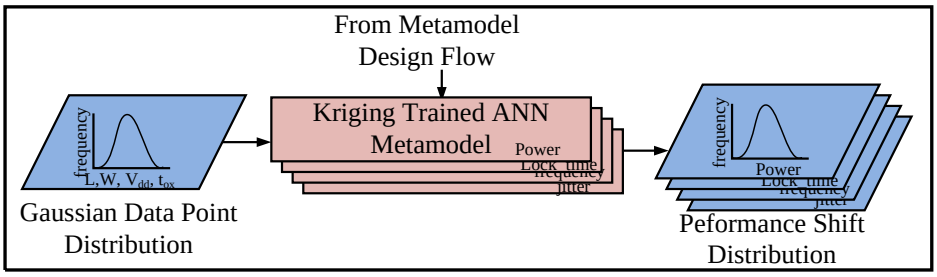


Figure 9: Statistical Variation Analysis

The performance results of the Monte Carlo analysis are compared with an analysis from the spice simulation of the PLL design in the next section.

10 Experimental Results

In this section, simulation experiments are performed on the case study 180 nm PLL design discussed in section 8 to illustrate the effectiveness of our proposed approach. The Kriging bootstrapped neural network metamodel is built using the MATLAB®Neural Network toolbox and the mGstat toolbox [28, 36]. The model used in the design flow is discussed in Section 5.3. The extracted parasitic netlist is parameterized and used for the sample data point generation. mGstat is used to implement the Kriging boostrapping of the sample data points and then the metamodel is generated using the Neural Network toolbox. Four metamodels are generated, one for each Figure of Merit (FoM) (Power(P_{PLL}) , Frequency (F_{PLL}), Locking time (Lck_{PLL}), and Jitter (J_{PLL})) characterizing the PLL. A Monte Carlo method is used to evaluate the statistical distribution of the four FoMs. A Gaussian distribution of 1000 samples is used for the simulation analysis. The results are presented in Fig. 12. Also presented in Figures 13, and 14 are statistical distributions using the ANN and the Kriging based metamodels, respectively, for comparison to the proposed metamodel.

10.1 Design Objective and Simulation Setup

All of the logical schematic and physical layout designs were performed using the CADENCE®virtuoso platform. The full blown parasitic (RLCK) netlist is extracted and parameterized with respect to the corresponding design variables. The parameterized netlist is used as the circuit description for design sampling. An ocean script is created with the parameterized netlist that can automate the design sampling procedure using MATLAB®. The Spectre analog simulator was used to perform the simulations. The algorithm used to generate the Kriging metamodels was written using MATLAB®with the help of the toolboxes mGstat [36] and SUMO [37]. A diagram showing the different tool interactions is shown in Fig. 10. Any design engineer can use this as a guideline for tool usage to reproduce our results when needed to be used in their circuit design.

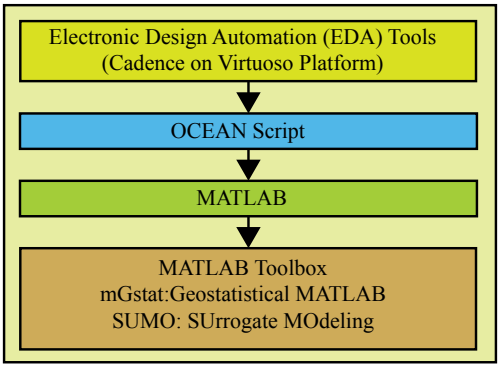


Figure 10: Experimental Steps and EDA/Non-EDA Tool Interactions.

The 180 nm PLL circuit design was simulated for a low power consumption optimization using the locking time as a design constraint. The optimization objective was to increase the yield and tolerance to process variation by minimizing the mean and variance of the power dissipation of the PLL. The statistical optimization process uses the Particle Swarm Optimization (PSO) algorithm described in Algorithm 1 and illustrated in Fig. 6 to search the design space on the generated Kriging trained ANN metamodel. Monte Carlo simulation experiments are a common method for the analysis of process variations on analog circuits in order to estimate the yield and efficiency of the design. Monte Carlo enables an efficient analysis of the design by randomly generating a distribution test case of design variables. The set of test cases is derived from a given probability distribution with a mean of the nominal value of the variable. The initial nominal values are selected from the baseline design and a Gaussian distribution with 10 % standard deviation is used to generate the sample set for the metamodel simulation. Subsequent iterations of the algorithm give the nominal point for the Monte Carlo simulations.

10.2 Results Analysis

Table 2 shows the accuracy of the proposed Kriging Bootstrapped Trained ANN Metamodels. The Root Mean Square Errors (RMSE) for each of the FoMs is shown. A lower value of RMSE indicates a higher accuracy. The low RMSE values thus demonstrate that the created metamodels are sufficiently accurate and can be used for design exploration.

Table 2: Statistical Accuracy of Kriging Generated Points [15].

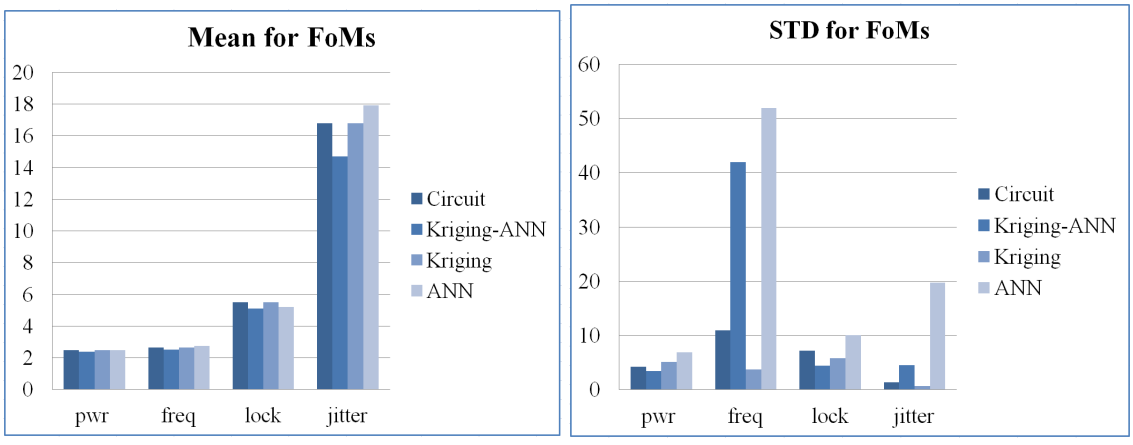
FoM	RMSE
Power (P_{PLL})	2.51 x 10 $^{-6}$
Frequency (F_{PLL})	5.68 x 10 $^{-13}$
Locking Time(Lck_{PLL})	5.01 x 10 $^{-12}$
Jitter (Lck_{PLL})	1.69 x 10 $^{-19}$

The Monte Carlo results for the various metamodels are shown in Table 3. A Monte Carlo analysis on the SPICE model is used as baseline to compare the results. The results are also compared with the bare Kriging and ANN metamodels.

Table 3: Statistical Analysis for Accuracy of Neural Network Metamodel for PLL FoMs [15].

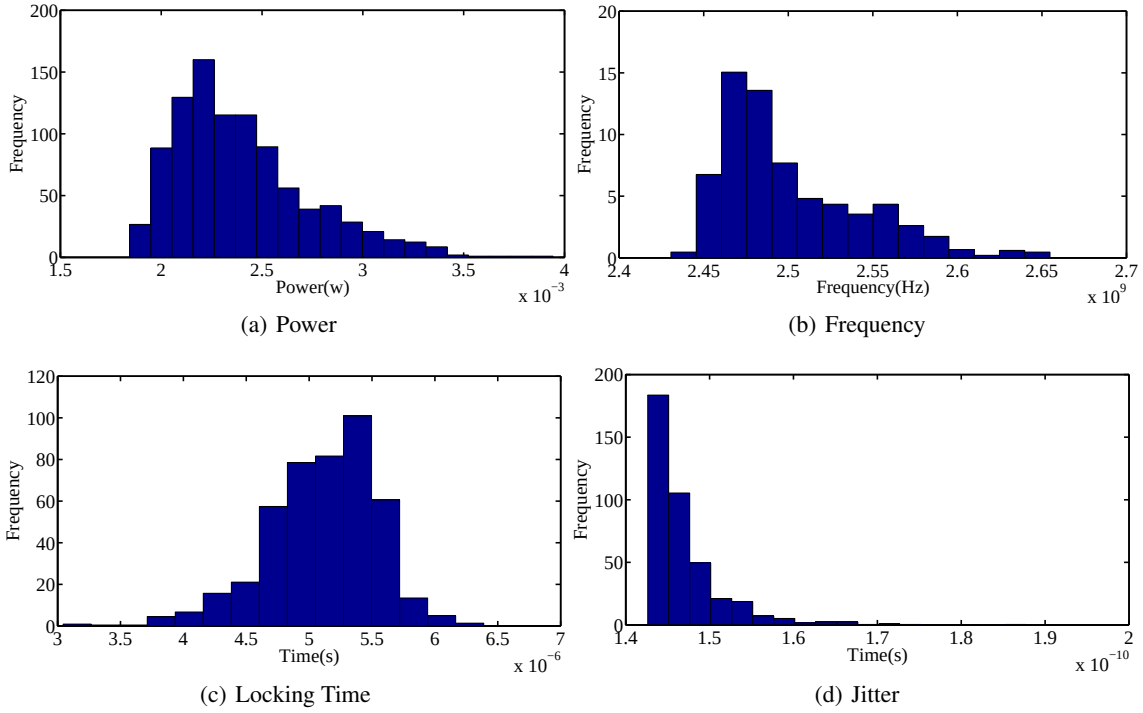
		Circuit	Kriging-ANN		Kriging		ANN	
		Value	Value	error (%)	Value	error (%)	Value	error (%)
P_{PLL}	Mean	2.48 mW	2.40 mW	3.22	2.50 mW	0.81	2.50 mW	0.81
	STD	0.42 mW	0.34 mW	19.05	0.51 mW	21.43	0.69 mW	64.28
F_{PLL}	Mean	2.66 GHz	2.51 GHz	5.64	2.66 GHz	0.11	2.74 GHz	5.38
	STD	10.95 MHz	41.93 MHz	282.92	3.72 MHz	66.03	51.9 MHz	373.97
Lck_{PLL}	Mean	5.51 μs	5.11μs	7.26	5.51 μs	0.07	5.20 μs	5.63
	STD	0.72 μs	0.44 μs	38.88	.58 ns	10.25	1.01 μs	40.27
J_{PLL}	Mean	16.80 ns	14.69ns	10.25	16.78ns	0.12	17.91 ns	6.61
	STD	1.32 ps	4.50 ps	240.91	0.68ps	48.48	19.17 ps	1352.22

Table 3 shows the mean (μ) and standard deviation (σ) for the FoMs in each of the metamodels. From the results the Kriging metamodels are shown to be most accurate on both the mean (μ) and (σ) values for all FoMs. The Kriging bootstrapped neural network metamodel on the other hand is shown to be more accurate on the (σ) values than the plain neural network metamodel but less accurate on the (μ) values. This difference is expected because while bootstrapping infuses the autocorrelation property of Kriging based techniques, some error is also introduced as well. Fig. 11 shows the errors for the (μ) and (σ) as a bar chart. The histograms of the Monte Carlo analysis for the Kriging bootstrapped, Kriging and neural network metamodels are shown in Figures 12, 13, and 14.



(a) Mean (b) STD

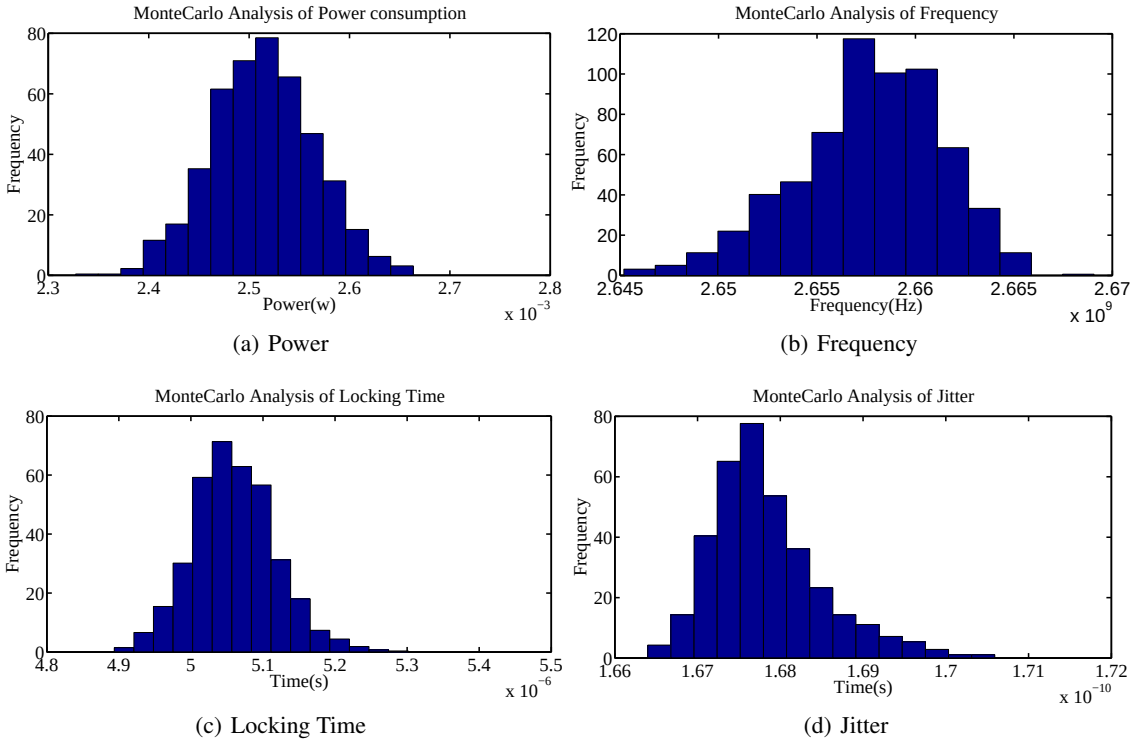
Figure 11: Comparative Results with Kriging and Neural Network [15].



(a) Power (b) Frequency

(c) Locking Time (d) Jitter

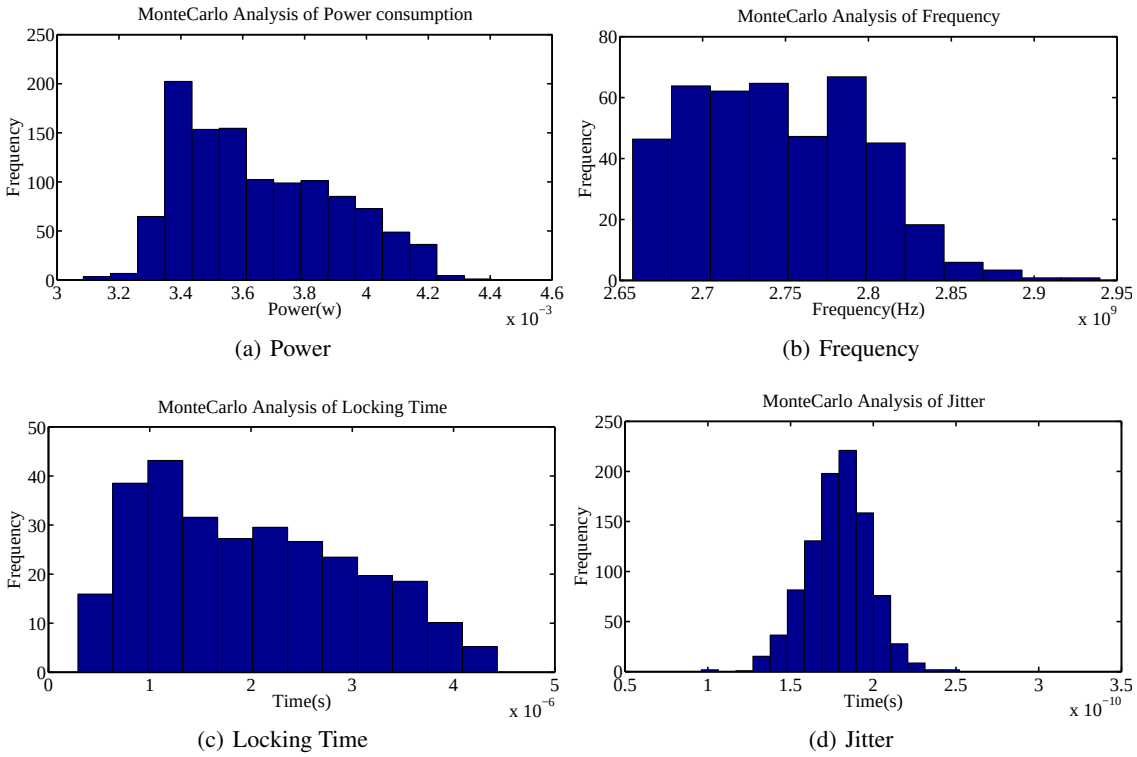
Figure 12: Statistical Analysis of FoMs using Kriging Bootstrapped Trained Neural Network based metamodeling [15].



(a) Power (b) Frequency

(c) Locking Time (d) Jitter

Figure 13: Statistical Analysis of FoMs using Kriging based metamodeling [15].



(a) Power (b) Frequency

(c) Locking Time (d) Jitter

Figure 14: Statistical Analysis of FoMs using Neural Network based metamodeling [15].

The value of the Kriging bootstrapped metamodeling technique is due to the reduced time cost for design exploration. While Kriging models may be more accurate, the time cost for design exploration for a large design space still becomes too expensive due to the repetitive solution of large-dimension systems of equations for *each* sample point. One obvious goal for metamodel use is the improved time cost. Table 4 shows the time cost for the Monte Carlo Analysis on each metamodel.

Table 4: Monte Carlo Time Analysis Comparison for Metamodels [15].

Model	Kriging-ANN	Kriging	ANN
Time	19 s	468 s	19 s
Speedup	24.63×	1	24.63×

Table 4 shows a speedup of approximately 25 times in time cost for the Monte Carlo Simulation of 1000 runs for the Kriging bootstrapped model over traditional Kriging. The significant improvement in time cost is large enough to mitigate the minimal error incurred in the metamodel. The overall use of metamodels significantly reduces the simulation time over SPICE models. It may be noted that the Monte Carlo simulation time on the SPICE models is approximately 5 days, which highlights the huge time gain with the use of metamodels.

The experimental analysis was performed using the generated parasitic netlists of the 180nm PLL designs. The optimization of the statistical analysis for the power consumption (P_{PLL}) was the objective, while using the locking time (Lck_{PLL}) as a design constraint. A total of 21 design parameters were used for the optimization simulation. Further statistical analysis was carried out using MATLAB®. The results from the optimization simulation displayed in Table 5 show an improved statistical variation of the design simulation. The histograms of the Monte Carlo analysis for the optimized Kriging bootstrapped metamodel are shown in Fig. 12.

From the results it is observed that the standard deviation for P_{PLL}, Lck_{PLL}, and jitter (J_{PLL}) are all minimized with the frequency (F_{PLL}) having an increased deviation. The mean power consumption was also reduced while the other FoMs were increased. This is expected since the statistical optimization started off with the design parameters for optimal performance.

Table 5: Statistical Optimization for Kriging Neural Network Metamodel for PLL FoMs [25].

		SPICE Netlist	Kriging-ANN Metamodel			
			Before Optimization		After Optimization	
		Value	Value	Error (%)	Value	Error (%)
Power (P_{PLL})	Mean (μ)	2.48 mW	2.40 mW	3.33	2.35 mW	2.08
	St. Dev. (σ)	0.42 mW	0.34 mW	19.05	0.39 mW	7.14
Frequency (F_{PLL})	Mean (μ)	2.66 GHz	2.51 GHz	5.64	2.78 GHz	4.51
	St. Dev. (σ)	10.95 MHz	41.93 MHz	282.92	16.92 MHz	54.52
Locking Time (Lck_{PLL})	Mean (μ)	5.51 μs	5.11μs	7.26	5.21 μs	5.44
	St. Dev. (σ)	0.72 μs	0.44 μs	38.88	0.42 μs	41.67
Jitter (J_{PLL})	Mean (μ)	16.80 ns	14.69ns	10.25	17.72ns	5.47
	St. Dev. (σ)	1.32 ps	4.50 ps	240.91	0.33ps	75

10.3 Comparative Research

Table 6 shows a brief comparison of metamodeling based design techniques. The comparisons are only a perspective and illustrate the applicability and viability of our proposed method for statistical variability analysis. Kriging modeling is presented in [6]. In [12] a polynomial based metamodeling design including a statistical analysis on process variation is presented. A polynomial regression based technique is presented in [38]. The accuracy based on the RMSE value of the models (except for [6] which uses MSE) is shown in column 4 of Table 6. The presented metamodels have been generated for different circuits, and even when the circuits are similar there are fabricated using different silicon technologies and performance measures making, direct comparisons impossible. Hence, the comparisons are only from a broad perspective point.

Table 6: Comparative Analysis of Related Research [15].

Research	Metamodel	Test Circuit	Accuracy
Garitselov [38]	Polynomial	PLL	0.157
Yu [6]	Kriging	RO	0.5325 (MSE)
		LC-VCO	0.5325 (MSE)
Okobiah [39]	Kriging	Simulated Annealing	3.2×10^{-9}
Kuo [12]	Polynomial	PLL	2.0×10^{-4}
iVAMS 3.0 [15]	Kriging-ANN	PLL	2.51×10^{-6}

11 Conclusion and Future Research

This paper presented a metamodeling design analysis, design exploration and optimization technique that combines traditional Kriging and ANNs to create process aware metamodels. Kriging based techniques are used to bootstrap sample data points which accommodate the correlation characteristics of Kriging techniques into the sample data. Simulation results indeed show an improved process awareness on the metamodels generated for the test case of an 180 nm PLL circuit. The Monte Carlo Simulation time also improved approximately 25×. The preliminary results are promising. Future research is planned to explore the use of Deep Learning techniques for the ANN structure and training and the automated incorporation of this framework within mixed-signal hardware description languages, such as Verilog-AMS, as presented in our previous work [41].

Acknowledgments

The current arXiv paper is based on the following conference presentations [15, 25]. The current paper presenting iVAMS 3.0 advances the state-of-art of iVAMS 1.0 [40] and iVAMS 2.0 [41], which were presented by us in the past. The authors would like to thank UNT graduate Dr. Oghenekarho Okobiah for his help on conference versions of this work.

References

[1] O. Okobiah, S. Mohanty, and E. Kougianos, "Fast Design Optimization through Simple Kriging Metamodeling: A Sense Amplifier Case Study," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 22,

no. 4, pp. 932–937, Apr 2014.

[2] O. Garitselov, S. P. Mohanty, and E. Kougianos, "A Comparative Study of Metamodels for Fast and Accurate Simulation of Nano-CMOS Circuits," *IEEE Transactions on Semiconductor Manufacturing*, vol. 25, no. 1, pp. 26–36, Feb 2012.

[3] O. Garitselov, S. Mohanty, and E. Kougianos, "A Comparative Study of Metamodels for Fast and Accurate Simulation of Nano-CMOS Circuits," *IEEE Transactions on Semiconductor Manufacturing*, vol. 25, no. 1, pp. 26–36, 2012.

[4] O. Okobiah, S. P. Mohanty, E. Kougianos, and M. Poolakkaparambil, "Towards Robust Nano-CMOS Sense Amplifier Design: A Dual-Threshold versus Dual-Oxide Perspective," in *Proceedings of the 21st ACM Great Lakes Symposium on VLSI*, 2011, pp. 145–150.

[5] W. Van Beers, "Kriging Metamodeling in Discrete-Event Simulation: An Overview," in *Proceedings of the Winter Simulation Conference*, 2005, pp. 202–208.

[6] G. Yu and P. Li, "Yield-Aware Analog Integrated Circuit Optimization Using Geostatistics Motivated Performance Modeling," in *Computer-Aided Design, 2007. ICCAD 2007. IEEE/ACM International Conference on*, Nov. 2007, pp. 464–469.

[7] O. Okobiah, S. P. Mohanty, E. Kougianos, and O. Garitselov, "Kriging-Assisted Ultra-Fast Simulated-Annealing Optimization of a Clamped Bitline Sense Amplifier," *VLSI Design, International Conference on*, vol. 0, pp. 310–315, 2012.

[8] H. You, M. Yang, D. Wang, and X. Jia, "Kriging Model Combined with Latin Hypercube Sampling for Surrogate Modeling of Analog Integrated Circuit Performance," in *Proceedings of the International Symposium on Quality of Electronic Design*, 2009, pp. 554–558.

[9] N. Jin and Y. Rahmat-Samii, "Advances in Particle Swarm Optimization for Antenna Designs: Real-Number, Binary, Single-Objective and Multiobjective Implementations," *IEEE Transactions on Antennas and Propagation*, vol. 55, no. 3, pp. 556–567, 2007.

[10] C. A. C. Coello, G. T. Pulido, and M. S. Lechuga, "Handling Multiple Objectives With Particle Swarm Optimization," *IEEE Transactions on Evolutionary Computation*, vol. 8, no. 3, pp. 256–279, 2004.

[11] I. Vilović, N. Burum, and D. Milić, "Using Particle Swarm Optimization in Training Neural Network for Indoor Field Strength Prediction," in *51st International Symposium ELMAR*, 2009, pp. 275–278.

[12] C.-C. Kuo, M.-J. Lee, C.-N. Liu, and C.-J. Huang, "Fast Statistical Analysis of Process Variation Effects Using Accurate PLL Behavioral Models," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 56, no. 6, pp. 1160–1172, June 2008.

[13] (2023) What Are Digital Twins? A Primer on Virtual Models. [Online]. Available: https://www.synopsys.com/blogs/chip-design/digital-twins-semiconductor-industry.html

[14] O. Okobiah, S. P. Mohanty, and E. Kougianos, "Exploring Kriging for Fast and Accurate Design Optimization of Nanoscale Analog Circuits," in *Proceedings of the 13th IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, 2014, pp. 244–247.

[15] O. Okobiah, S. P. Mohanty, and E. Kougianos , "Kriging Bootstrapped Neural Network Training for Fast and Accurate Process Variation Analysis," in *Proceedings of the 15th IEEE International Symposium on Quality Electronic Design (ISQED)*, 2014, pp. 365–372.

[16] M. Zakerifar, W. Biles, and G. Evans, "Kriging Metamodeling in Multi-objective Simulation Optimization," in *Proceedings of the Winter Simulation Conference (WSC)*, 2009, pp. 2115–2122.

[17] W. E. Biles, J. P. C. Kleijnen, W. C. M. van Beers, and I. van Nieuwenhuyse, "Kriging Metamodeling in Constrained Simulation Optimization: An Explorative Study," in *Proceedings of the 39th Winter Simulation Conference*, 2007, pp. 355–362.

[18] G. Dellino, J. Kleijnen, and C. Meloni, "Robust Simulation-Optimization using Metamodels," in *Proceedings of the Winter Simulation Conference (WSC)*, Dec. 2009, pp. 540–550.

[19] B. Ankenman, B. Nelson, and J. Staum, "Stochastic Kriging for Simulation Metamodeling," in *Proceedings of the Winter Simulation Conference*, 2008, pp. 362–370.

[20] V. Aggarwal, "Analog Circuit Optimization using Evolutionary Algorithms and Convex Optimization," Master's thesis, Massachusetts Institute of Technology, May 2007.

[21] L. Wang, "A Hybrid Genetic Algorithm- Neural Network Strategy for Simulation Optimization," *Applied Mathematics and Computation*, vol. 170, no. 2, pp. 1329–1343, 2005.

[22] A. Khosravi, S. Nahavandi, and D. Creighton, "Developing Optimal Neural Network Metamodels Based on Prediction Intervals," in *Proceedings of the International Joint Conference on Neural Networks*, 2009, pp. 1583–1589.

[23] C. W. Zobel and K. B. Keeling, "Neural Network-based Simulation Metamodels for Predicting Probability Distributions," *Computers and Industrial Engineering*, vol. 54, pp. 879–888, May 2008.

[24] I. Sabuncuoglu and S. Touhami, "Simulation Metamodelling With Neural Networks: An Experimental Investigation." *International Journal of Production Research,*, vol. 40, no. 11, pp. 2483–2505, 2002.

[25] S. P. Mohanty, E. Kougianos, and V. P. Yanambaka, "Ultra-Fast Variability-Aware Optimization of Mixed-signal Designs Using Bootstrapped Kriging," in *Sixteenth International Symposium on Quality Electronic Design ISQED*, 2015, pp. 239–242.

[26] G. Bohling, "Kriging," Kansas Geological Survey, Tech. Rep., 2005.

[27] O. Garitselov, S. Mohanty, E. Kougianos, and G. Zheng, "Particle Swarm Optimization over Non-Polynomial Metamodels for Fast Process Variation Resilient Design of Nano-CMOS PLL," in *Proceedings of the great lakes symposium on VLSI*, ser. GLSVLSI '12, 2012, pp. 255–258.

[28] MATLAB, *MATLAB and Neural Network Toolbox Release 2012b*. Natick, Massachusetts, United States: The MathWorks Inc., 2012.

[29] R. Poli, "Analysis of the Publications on the Applications of Particle Swarm Optimisation," *Journal of Artificial Evolution and Applications*, vol. 2008, pp. 4:1–4:10, January 2008.

[30] P. Civicioglu, "Transforming Geocentric Cartesian Coordinates to Geodetic Coordinates by Using Differential Search Algorithm," *Computers and Geosciences*, vol. 46, no. 0, pp. 229–247, 2012.

[31] M. Dorigo, M. Birattari, and T. Stutzle, "Ant Colony Optimization – Artificial Ants as a Computational Intelligence Technique," *IEEE Computational Intelligence Magazine*, vol. 1, pp. 28–39, 2006.

[32] S. Bennour, A. Sallem, M. Kotti, E. Gaddour, M. Fakhfakh, and M. Loulou, "Application of the PSO technique to the Optimization of CMOS Operational Transconductance Amplifiers," in *Proceedings of the 5th International Conference on Design and Technology of Integrated Systems in Nanoscale Era*, 2010, pp. 1–5.

[33] O. Garitselov, S. Mohanty, E. Kougianos, and G. Zheng, "Particle Swarm Optimization over Non-Polynomial Metamodels for Fast Process Variation Resilient Design of Nano-CMOS PLL," in *Proceedings of the great lakes symposium on VLSI*, 2012, pp. 255–258.

[34] K. Kang, B. Paul, and K. Roy, "Statistical Timing Analysis using Levelized Covariance Propagation," in *Design, Automation and Test in Europe, 2005. Proceedings*, vol. 2, 2005, pp. 764–769.

[35] S. Nassif, "Modeling and analysis of manufacturing variations," in *Custom Integrated Circuits, 2001, IEEE Conference on.*, 2001, pp. 223–228.

[36] *mGstat: A Geostatistical Matlab Toolbox*, last accessed on 08 Apr 2025. [Online]. Available: mgstat.sourcefourge.net

[37] D. Gorissen, I. Couckuyt, P. Demeester, T. Dhaene, and K. Crombecq, "A Surrogate Modeling and Adaptive Sampling Toolbox for Computer Based Design," *J. Mach. Learn. Res.*, vol. 11, pp. 2051–2055, August 2010.

[38] O. Garitselov, S. Mohanty, and E. Kougianos, "Accurate Polynomial Metamodeling-Based Ultra-Fast Bee Colony Optimization of a Nano-CMOS Phase-Locked Loop," *ASP Journal of Low Power Electronics (JOLPE)*, vol. 8, no. 3, pp. 317–328, June 2012.

[39] O. Okobiah, S. Mohanty, and E. Kougianos, "Ordinary Kriging Metamodel-Assisted Ant Colony Algorithm for Fast Analog Design Optimization," in *Proceedings of the 13th International Symposium on Quality Electronic Design (ISQED)*, March 2012, pp. 458–463.

[40] S. P. Mohanty and E. Kougianos, "iVAMS 1.0: Polynomial-Metamodel-Integrated Intelligent Verilog-AMS for Fast, Accurate Mixed-Signal Design Optimization," *arXiv Computer Science*, vol. abs/1905.12812, 2019. [Online]. Available: http://arxiv.org/abs/1905.12812

[41] S. P. Mohanty and E. Kougianos , "iVAMS 2.0: Machine-Learning-Metamodel-Integrated Intelligent Verilog-AMS for Fast and Accurate Mixed-Signal Design Optimization," *arXiv Electrical Engineering and Systems Science*, vol. abs/1907.01526, 2019. [Online]. Available: http://arxiv.org/abs/1907.01526

Authors' Biographies

Saraju P. Mohanty received the bachelor's degree (Honors) in electrical engineering from the Orissa University of Agriculture and Technology, Bhubaneswar, in 1995, the master's degree in Systems Science and Automation from the Indian Institute of Science, Bengaluru, in 1999, and the Ph.D. degree in Computer Science and Engineering from the University of South Florida, Tampa, in 2003. He is a Professor with the University of North Texas. His research is in "Smart Electronic Systems" which has been funded by National Science Foundations (NSF), Semiconductor Research Corporation (SRC), U.S. Air Force, NIDILRR, IUSSTF, and Mission Innovation. He has authored 550 research articles, 5 books, and 10 granted and pending patents. His Google Scholar h-index is 62 and i10-index is 300 with 17,000 citations. He is regarded as a visionary researcher on Smart Cities technology in which his research deals with security and energy aware, and AI/ML-integrated smart components. He introduced the Secure Digital Camera (SDC) in 2004 with built-in security features designed using Hardware Assisted Security (HAS) or Security by Design (SbD) principle. He is widely credited as the designer for the first digital watermarking chip in 2004 and first the low-power digital watermarking chip in 2006. He is a recipient of 21 best paper awards, Fulbright Specialist Award in 2021, IEEE Consumer Electronics Society Outstanding Service Award in 2020, the IEEE-CS-TCVLSI Distinguished Leadership Award in 2018, and the PROSE Award for Best Textbook in Physical Sciences and Mathematics category in 2016. He has delivered 31 keynotes and served on 15 panels at various International Conferences. He has been serving on the editorial board of several peer-reviewed international transactions/journals, including IEEE Transactions on Big Data (TBD), IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), IEEE Transactions on Consumer Electronics (TCE), and ACM Journal on Emerging Technologies in Computing Systems (JETC). He has been the Editor-in-Chief (EiC) of the IEEE Consumer Electronics Magazine (MCE) during 2016-2021. He served as the Chair of Technical Committee on Very Large Scale Integration (TCVLSI), IEEE Computer Society (IEEE-CS) during 2014-2018 and on the Board of Governors of the IEEE Consumer Electronics Society during 2019-2021. He serves on the steering, organizing, and program committees of several international conferences. He is the steering committee chair/vice-chair for the IEEE International Symposium on Smart Electronic Systems (IEEE-iSES), the IEEE-CS Symposium on VLSI (ISVLSI), and the OITS International Conference on Information Technology (OCIT). He has supervised 3 post-doctoral researchers, 19 Ph.D. dissertations, 29 M.S. theses, and 41 undergraduate projects.

Elias Kougianos received a BSEE from the University of Patras, Greece in 1985 and an MSEE in 1987, an MS in Physics in 1988 and a Ph.D. in EE in 1997, all from Louisiana State University. From 1988 through 1998 he was with Texas Instruments, Inc., in Houston and Dallas, TX. In 1998 he joined Avant! Corp. (now Synopsys) in Phoenix, AZ as a Senior Applications engineer and in 2000 he joined Cadence Design Systems, Inc., in Dallas, TX as a Senior Architect in Analog/Mixed-Signal Custom IC design. He has been at UNT since 2004. He is a Professor in the Department of Electrical Engineering, at the University of North Texas (UNT), Denton, TX. His research interests are in the area of Analog/Mixed-Signal/RF IC design and simulation and in the development of VLSI architectures for multimedia applications. He is an author of over 200 peer-reviewed journal and conference publications.