Process Variation Analysis and Optimization of a FinFET based VCO

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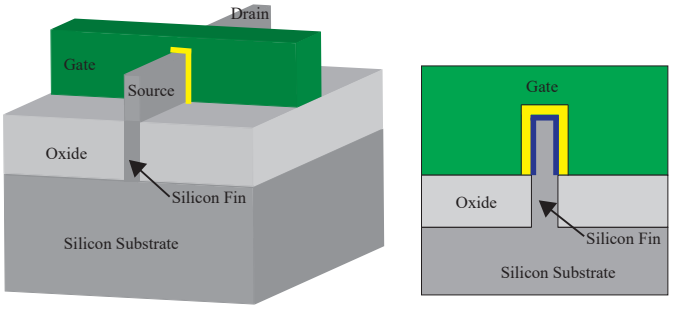
***Abstract*—Fin-type field-effect transistors (FinFETs) are promising substitutes for bulk CMOS for nanoscale technologies. In this paper, the viability of a mixed-signal design for FinFET based technologies using a nanoscale current-starved voltage controlled oscillator (VCO) is investigated. Design issues are analyzed and a comparison between a CMOS VCO and a FinFET-based VCO is presented. The figures-of-merit (FoMs) used for comparison are center frequency and frequency-voltage ($f - V$) characteristics under process variation. Models are developed for the $f - V$ characteristics of both the CMOS and FinFET VCOs. In addition, width quantization-aware modeling has been performed for the FinFET-based VCO using a polynomial metamodel, which can be used for further optimization. The quantization aware modeling is highly accurate as evident from a correlation coefficient R^2 of 0.999 and Root Mean Square Error of 6.2 MHz. The FinFET VCO has 5.5× faster oscillation frequency with 2.6% variability as opposed to 19.7% for the CMOS VCO. To the best of the authors' knowledge, this is the first paper that examines FinFET technology with respect to process variation in mixed signal designs at the circuit level, and presents a quantitative as well as qualitative comparison between CMOS and FinFET technologies.**

***Index Terms*—Process Variation, FinFET, Voltage Controlled Oscillator (VCO), Mixed-signal design, Metamodeling**

I. Introduction

Moore's law has remained a driving force for scaling CMOS technologies at the 45 nm node and below to meet power, speed and packaging density requirements of current state-of-the-art integrated circuits. The current size of commercially available CMOS technologies has reached 14 nm or below. At these nano CMOS regimes, short channel effects (SCEs) are dominant [1], [2]. In addition to SCEs, planar MOSFETs suffer from random dopant fluctuations (RDF) in the channel area, which are believed to be the main source of threshold voltage mismatch among devices fabricated on the same wafer [3]. FinFET and multigate Field Effect Transistors are promising replacements for the traditional CMOS technology. Process variation in FinFETs due to RDF is reduced due to undoped or lightly doped body and reduced carrier mobility degradation [4]. Various FinFET devices have been introduced which can be used as replacement for CMOS transistors. In a FinFET transistor, the channel electrical potential is controlled by the voltage at the gate. Effectively, this reduces the SCE compared to CMOS transistors [5]. Another advantage of the FinFET is that the traditional MOSFET fabrication processes can be used. Fig. 1 shows the structure of a traditional tri-gate FinFET as developed by Intel. Here, the fin itself acts as a channel and terminates on both sides of the source and drain. A metal gate is formed over the Si substrate, which controls the channel. Straddling of a metal gate over a Si-fin gives efficient gate-controlled characteristics compared to MOSFET. Since the gate straddles the fin, the length of the channel is the same as the width of the fin. As there are effectively two gates around the fin, the width of the channel is twice the height of the fin. The height of the FinFET is equivalent to the width of the MOSFET. In order to attain the same area efficiency, the height of the fin should be half the fin pitch width.



(a) 3D Structure (b) Cross-sectional View

Fig. 1. Structure of Intel's tri-gate FinFET [6].

With the introduction in 2012 of the third generation core processors, Intel introduced the FinFET technology commercially [7]. Memory design [8], [9] and digital design [10], [11] with FinFETs has been explored quite exhaustively, while their feasibility for analog design has been relatively less explored. This paper presents a FinFET study for mixed-signal design at the circuit level. A Voltage Controlled Oscillator (VCO) is chosen as a case study and the FinFET and CMOS implementations of the same oscillator are compared.

The notations and definitions used in this paper are given in Table I. The rest of the paper is organized in the following manner: Section II discusses the novel contributions of this paper. Related prior research is presented in section III. The proposed novel methodology for FinFET VCO design is discussed in section IV. Section V presents discussions related

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to the design and center frequency of the VCO, with respect to 45 nm CMOS and 15 nm FinFET technologies. Modeling and comparison of the $f-V$ characteristics are presented in section VI. Section VII presents the process variation study. A width quantization-aware model for FinFET VCO optimization is presented in section VIII. This is followed by conclusions and directions for future research in section IX.

TABLE I
NOTATION AND ACRONYMS USED IN THIS PAPER

V_{DD}	: Supply voltage
V_{tune}	: Tuning voltage of VCO
V_{Th}	: Threshold voltage
H_{fin}	: Fin Height
T_{oxf}	: Oxide thickness of front gate of FinFET
T_{oxb}	: Oxide thickness of back gate of FinFET
T_{Si}	: Body Thickness
$freq_{CMOS}$	: Frequency of CMOS VCO
$freq_{FinFET}$	: Frequency of FinFET VCO
$freq(V_{tune}^{i})$	: Frequency response at point V_i of the tuning voltage of the VCO
$\widehat{freq(V_{tune}^{i})}$	: Predicted frequency response at point V_i of the tuning voltage of the VCO
χ^2	: Chi-squared test statistic
RMSE	: Root Mean Square Error
R^2	: Coefficient of Determination
c_v	: Coefficient of Variation
N	: Number of Measurements
N_{fin-p}	: Number of fins in P-type FinFET
N_{fin-n}	: Number of fins in N-type FinFET
N_{ch}	: Channel Doping Concentration
σV_{Th}	: Standard Deviation of V_{Th}
L	: Channel length
W	: Channel width

II. CONTRIBUTIONS OF THIS PAPER

The major contribution of this paper is the process variation analysis of FinFET VCO characteristics. The variation of FinFET device parameters which are impacted by the manufacturing processes are considered. Guided by the process variation analysis, device parameters are considered for optimization of the VCO. Overall, the *novel contributions* of this paper can be summarized as follows:

1) A comparison between a nano-CMOS VCO and a FinFET-based VCOs is performed.
2) A Current Starved VCO has been used for this comparison. Comparisons are drawn with respect to center frequency, frequency-voltage characteristics, and process variation. Qualitative and quantitative discussions are presented.
3) Models of frequency-voltage characteristics are developed for the nano-CMOS VCO and the FinFET-based VCO.
4) A width quantization aware polynomial model of the FinFET VCO is presented.
5) A surface model for width quantization-aware optimization is presented for the FinFET VCO.

The FinFET models used in the design and simulations in the current paper are obtained from the NCSU free Process Design Kit (PDK) for 15 nm (FreePDK15). This PDK was developed by NCSU in collaboration with Mentor Graphics® [12], [13] for highly accurate modeling. The PDK has been made available for free for academic usage and research. In addition, a cell library based on this PDK [14] is used in this work.

III. RELATED PRIOR RESEARCH

In [15] a novel design flow was presented for simultaneous Power minimization, Performance maximization and Process variation tolerance (P3) of nano-CMOS SRAM cells. Process variation analysis of the optimized cell considering twelve device parameters was also conducted. In [16] a novel fast and unified mixed signal design methodology is proposed by incorporating manufacturing process variation awareness in power, performance, and parasitic optimization. The design of a process variation aware 90 nm VCO is demonstrated as case study. In [17], a design flow for a P4VT (Power-Performance-Process-Parasitic-Voltage-Temperature) aware VCO was presented. The process-voltage variation is performed on 5 parameters assuming a normal distribution on each of the parameters.

In [18] the tunability feature of double gate MOSFET circuits due to back-gate bias is employed in analog circuits and VCOs [19], but process variation is not taken into account. In [20] different configurations of a double gate fully depleted SOI based FinFET current mirror are explored for process variation resiliency. In [21] the enormous potential of source/drain extension (SDE) regions in FinFETs for ultra-low-voltage (ULV) analog applications was analyzed. Results show that SDE region optimization provides an additional degree of freedom apart from device parameters (fin width and aspect ratio) to design future nanoscale analog devices.

In [22] a novel design methodology for design of an optimal and robust current starved voltage controlled oscillator (CSVCO) circuit was presented. In [23] a novel flow for parasitic and process-variation aware design of radio-frequency integrated circuits (RFICs) has been proposed. A nano-CMOS CSVCO circuit has been designed using this flow as a case study. The proposed design flow could bring the oscillation frequency within 4.5% of the target, leading to convergence of the complete design in only one design iteration. In [24] the design of a P4 (Power-Performance-Process-Parasitic) aware VCO is presented. Performance optimization of the VCO along with a dual-oxide power minimization technique was performed in the presence of worst case variation. The results show 25% power (including leakage) minimization with only 1% degradation in center frequency compared to the target frequency, in the presence of parasitics and worst-case process variation.

IV. THE PROPOSED METHODOLOGY FOR THE FINFET BASED VCO

The proposed methodology is represented in Fig. 2. The proposed flow ensures that the resulting physical design is not only resistant to nanoscale process variations but is also highly accurate. The baseline VCO is designed and then the netlist is parameterized for the device geometry parameter set $D = (N_{fin-n}, N_{fin-p})$, where N_{fin-n} signifies the number

of fins in the n-type device and N_{fin-p} signifies the number of fins in the p-type device. An accurate process variation analysis is performed on the FinFET VCO.

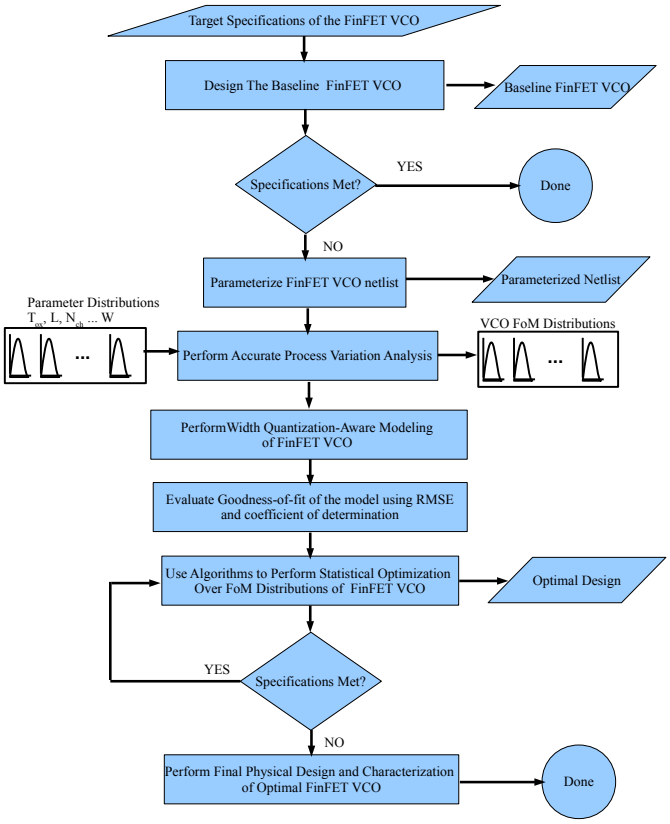


Fig. 2. Proposed methodology for FinFET based VCO.

A width quantization aware polynomial model of the FinFET VCO relating D the to the frequency ($freq_{FinFET}$) of the FinFET VCO is developed. This model may be used in discrete optimization techniques. The model is evaluated using the Root Mean Square Error (RMSE) and the coefficient of determination R^2. The parameterized netlist is then subjected to a process variation aware statistical optimization loop in order to meet the specifications. Once the parameter values (D) are obtained, the physical design of the VCO is performed using these values.

V. Design of a Current-Starved FinFET VCO

In this section, a 45 nm CMOS SVCO is designed as a baseline for a comparative perspective with a FinFET based CSVCO. Currently, early design with FinFETs is done using TCAD simulators (MEDICI, Sentaurus, ATLAS, etc.), which limit design flexibility and are computationally expensive. The models, PDK and cell library developed by NCSU were used for the simulation of the FinFET circuit. The key parameter values for bulk CMOS and FinFET models are shown in table II.

The body thickness (T_{Si}) of a single fin equals the silicon channel thickness. The current flows from source to drain along the wafer plane. Each fin provides $2 \times H_{fin}$ of device width, where H_{fin} is the height of each fin. For FinFET devices, widths are quantized into units of the fins. Large width devices are obtained by using multiple fins [25].

TABLE II
Device Parameter Values for the Transistors.

Parameter	Bulk CMOS	FinFET
Oxide Thickness T_{ox} (nm)	1.4	1.5
Threshold voltage V_{Th} (V)	V_{Thn} = 0.22, V_{Thp} = - 0.22	V_{Thn} = 0.31, V_{Thp} = - 0.25
Channel doping N_{ch} (cm^{-3})	2.8×10^{18}	2×10^{16}
Fin-Height H_{fin} (nm)	–	26
Body Thickness T_{Si} (nm)	–	8.4

The circuit diagrams for the CSVCOs using 45 nm bulk CMOS and 15 nm FinFET are shown in Figs. 3 and 4, respectively. The supply voltage (V_{DD}) is kept at 1 V. An inverter is formed by devices PM1 (FP1) and NM1 (FN1). The current sources are formed by PM2 (FP2) and N2 (FN2), which limit the current available to the inverter, hence "starving" the inverter for current. The tuning voltage (V_{tune}) sets the drain currents in the devices PM11 (FP11) and NM11 (FN11), which form the input stage. The currents in PM11 (FP11) and NM11 (FN11) are mirrored in each inverter/current source stage.

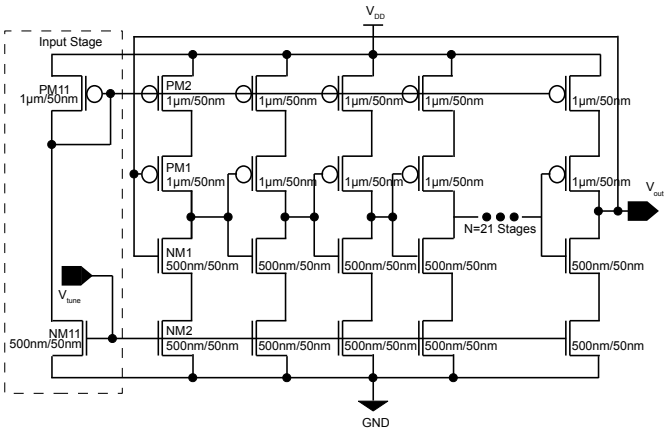


Fig. 3. Schematic diagram of a 45nm CMOS VCO circuit.

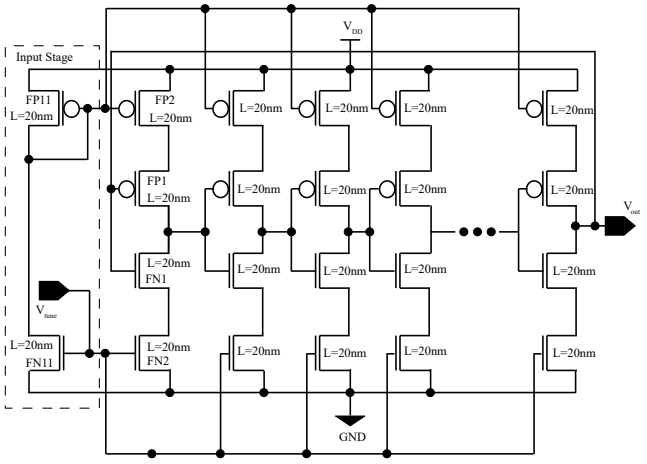


Fig. 4. Schematic diagram of a 15nm FinFET based VCO circuit.

The oscillation frequency of a CSVCO when $V_{tune} = V_{DD}/2$ (also called the center frequency) is given by the following [1]:

$$freq_{VCO} = \frac{I_D}{nC_tV_{DD}}, \quad (1)$$

where I_D = drain current, n = number of stages, C_t = total capacitance on the drains of PM1 and NM1, and V_{DD} is the supply voltage. In this design $n = 21$, I_D=10μA and C_t=4.7 fF are chosen for a target frequency of 100 MHz. The total capacitance C_t is $C_{tot} \times$ (area of the device). For a CMOS device, C_{tot}=C_{ox} (gate-oxide capacitance of the device). For a FinFET based device, C_{tot} is calculated as the series combination of three terms as follows:

$$\frac{1}{C_{tot}} = \frac{1}{C_{Si}} + \frac{1}{C_{gate}} + \frac{1}{C_{ox}}, \quad (2)$$

where C_{Si} is the capacitance of the carriers in the channel, and C_{gate} is the depletion capacitance of the gate electrode. This leads to smaller intrinsic gate capacitance in a FinFET, resulting in higher oscillation frequency. A center frequency of 1.8 GHz has been achieved for the FinFET VCO.

VI. Mathematical Modeling of VCO Frequency-Voltage ($f-V$) Characteristics

Fig. 5 represents the flow for modeling the $f-V$ characteristics of the VCO. First, both VCOs are simulated to plot the $f-V$ characteristics. Using curve fitting techniques, the mathematical models for the CMOS VCO and the FinFET VCO are then developed. The output frequency vs. tuning voltage (V_{tune}) characteristics are plotted for both CMOS and FinFET VCOs in Fig. 6.

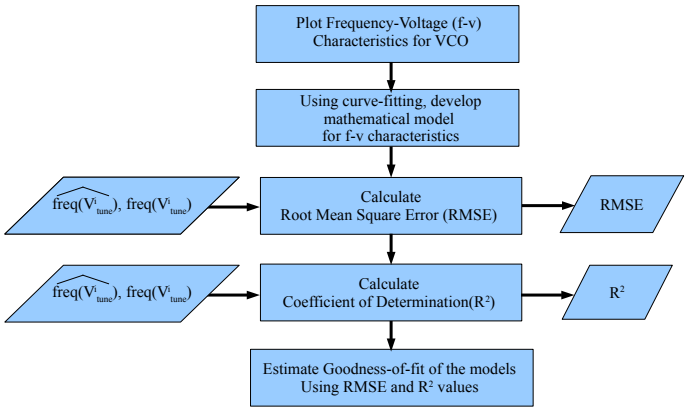


Fig. 5. Design flow for modeling the $f-V$ characteristics of the VCO.

The goodness-of-fit of the model is evaluated using the Root Mean Square Error (RMSE) and the Coefficient of Determination (R^2). The RMSE is normally used to measure the differences between the predicted model and an already present one. The RMSE represents the standard deviation of the predicted model's values from the original values. A smaller value will indicate an accurate model [26]. An RMSE of 8.369 MHz for the CMOS $f-V$ characteristics model was

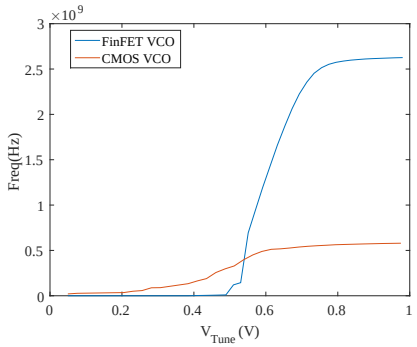


Fig. 6. Tuning curves of CMOS and FinFET VCOs.

obtained. The RMSE is calculated according to the following formula:

$$\text{RMSE} = \sqrt{\frac{1}{N}\sum_{i=0}^{N}(freq(V_{tune}^i) - \widehat{freq(V_{tune}^i)})^2}, \quad (3)$$

where N is the number of measurements, $freq(V_{tune}^i)$ and $\widehat{freq(V_{tune}^i)}$ are the measured and predicted frequency responses respectively at point V_{tune}^i of the tuning voltage (V_{tune}) data observations. R^2 measures the proportion of the variation of the tuning voltage data observations around the mean that is explained by the fitted regression model. R^2 is the statistical measure which is mainly used to predict future outcome values of the particular model. The advantage of using R^2 is that its scale is intuitive, and an improvement in the model results in proportional increase in R^2. The closer R^2 is to 1, the greater the degree of association between variables V_{tune} and the response. R^2 is calculated as follows:

$$R^2 = 1 - \frac{\sum_{i=0}^{N}(freq(V_{tune}^i) - \widehat{freq(V_{tune}^i)})^2}{\sum_{i=0}^{N}(freq(V_{tune}^i) - \overline{freq(V_{tune}^i)})^2}, \quad (4)$$

To obtain the $f-V$ characteristics for both VCOs, curve fitting technique was used. For the CMOS VCO the best-fit curve is obtained as the sum of 2 normal curves:

$$\begin{aligned} freq_{CMOS}(V_{tune}) = & a_0 \exp\left(-\frac{V_{tune}-b_0}{c_0}\right)^2 + \\ & a_1 \exp\left(-\frac{V_{tune}-b_1}{c_1}\right)^2, \end{aligned} \quad (5)$$

where a_0, b_0, c_0, a_1, b_1 and c_1 are fitting parameters. The values of these fitting parameters are shown in table III. An R^2 value of 0.9992 for the CMOS $f-V$ characteristics model was obtained.

For the FinFET VCO, a 3rd degree polynomial is chosen as best-fit in the form of:

$$freq_{FinFET}(V_{tune}) = p_0 + p_1V_{tune} + p_2V_{tune}^2 + p_3V_{tune}^3, \quad (6)$$

where p_0, p_1, p_2 and p_3 are curve-fitting parameters. The values of these fitting parameters are shown in table IV. RMSE is 6.21 MHz and R^2 is 0.9997 for the FinFET $f-V$ characteristics model.

TABLE III
CURVE FITTING PARAMETER VALUES FOR 45 NM CMOS VCO.

Parameter	Value
a_0 (MHz)	581.4
b_0 (V)	0.914
c_0 (V)	0.436
a_1 (MHz)	148.0
b_1 (V)	0.601
c_1 (V)	0.130

TABLE IV
CURVE FITTING PARAMETER VALUES FOR 15NM FINFET VCO.

Parameter	Value
p_0 (GHz)	-19.67
p_1 (GHz/V)	34.27
p_2 (GHz/V^2)	-12.98
p_3 (GHz/V^3)	0.99

VII. PROCESS VARIATION ANALYSIS OF THE FINFET VCO

Fig. 7 shows the flow of the process variation analysis for the FinFET VCO. In the analysis, 500 Monte Carlo simulations are performed. The probability distribution function (pdf) and the cumulative distribution function (cdf) are plotted for both VCOs. From this data, the mean (μ) and standard deviation (σ) are calculated. The chi-square (χ^2) goodness-of-fit is also performed using $freq_{CMOS}$ and $freq_{FinFET}$. Then the coefficient of variation (c_v) is calculated. c_v is defined as the ratio of the standard deviation and the mean σ/μ.

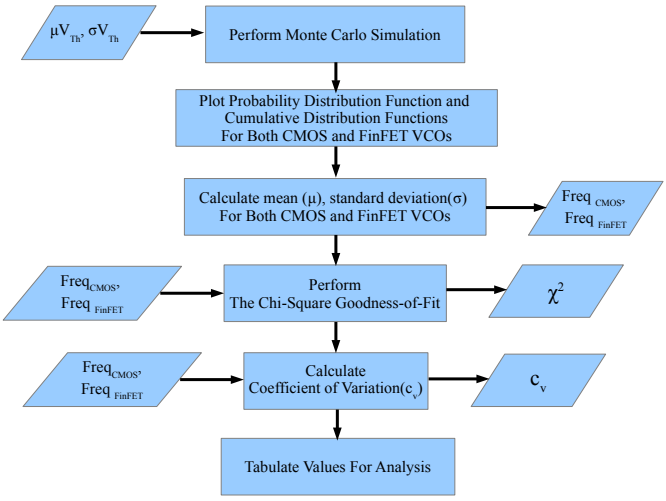


Fig. 7. Flow of process variation analysis of the FinFET VCO.

Eqn. 7 shows how the threshold voltage standard deviation (σV_{Th}) varies with gate oxide thickness (T_{ox}), channel dopant concentration (N_{ch}) and channel length (L) and width (W) [27]:

$$\sigma V_{Th} = \left(\frac{\sqrt[4]{4q^3\epsilon_{Si}\phi_B}}{2}\right)\left(\frac{T_{ox}}{\epsilon_{ox}}\right)\left(\frac{\sqrt[4]{N_{ch}}}{\sqrt{WL}}\right), \quad (7)$$

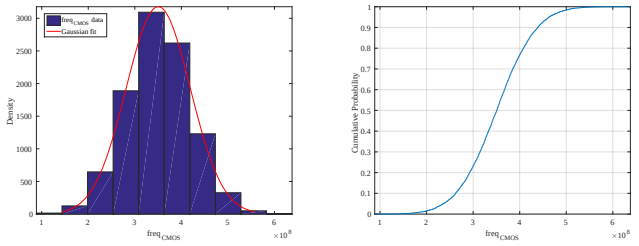
where $\phi_B = 2\kappa_B T \ln(N_{ch}/n_i)$ (with κ_B Boltzmann's constant, T the absolute temperature, n_i the intrinsic carrier concentration, q the elementary charge), and ϵ_{ox} and ϵ_{Si} are the permittivity of oxide and silicon, respectively. The above expression is consistent with observations that σV_{Th} is inversely proportional to the square root of the device area. Since (from Eqn. 7) the variation in device geometry (length, width and oxide thickness) and doping profile parameters can be translated into the effective variation in threshold voltage [28], threshold voltage fluctuation is considered as the major source of process variation when the performance impact of the parameter fluctuations are investigated. V_{Th} variations are assumed as having a normal distribution with mean values as specified in Table II and standard deviation (σV_{Th}) as 10% of the mean, assuming the same range of parameter variation for bulk CMOS and FinFET devices. The authors have tried extensively to locate PDKs that are as complete as possible, from many sources: both freely available as well as those provided by commercial entities. In both cases either there isnt any statistical information at all or, the only available information is in the form of "slow", "typical", and "fast" spice models. These are useful for corner analyses but not useful at all for obtaining distribution results, as is required by the modeling/optimization methodology presented in this paper. The selection of a standard deviation of 10% was guided by experience with real processes. Typically, a process with 10% σV_{Th} is not considered very good. For an in-control process 2%-3% σV_{Th} is acceptable. The point to be made in the following discussion is that with even such large variability, the modeling and optimization approach presented in ths paper can bring the design in control.

From Eqn. 7, it is seen that for bulk CMOS, both the random dopant fluctuations (N_{ch}) and gate workfunction (ϕ_B) are responsible for σV_{Th}. However, in the case of FinFET technology, due to the very lightly doped channel, there are no significant random dopant fluctuations, hence only ϕ_B is responsible for σV_{Th} [29]. Hence, the contributing factors are different [30]. Therefore, for ease of comparison, the range of variation is taken to be the same [31]. 500 Monte Carlo simulations are run. Figs. 8(a) and 8(c) show the pdfs of the center frequency for the VCOs, while Figs. 8(b) and 8(d) present the cdfs. It is observed that the distributions follow a normal trend.

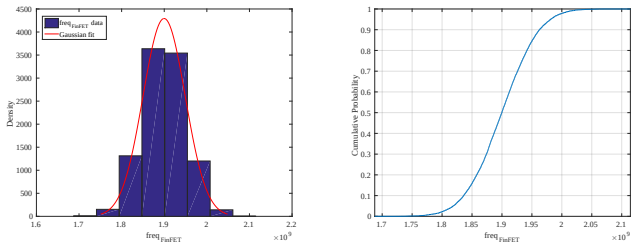
The chi-square goodness of fit [26] has also been evaluated with a 5% significance level, which satisfies the *null hypothesis* that $freq_{CMOS}$ and $freq_{FinFET}$ follow a normal distribution. The chi-square test statistic is given by the following:

$$\chi^2 = \sum_{i=1}^{N} \frac{(O(freq)_i - E(freq)_i)^2}{E(freq)_i}, \quad (8)$$

where $O(freq)_i$ are the observed counts and $E(freq)_i$ are the expected counts. For comparison of the CMOS and FinFET VCOs in the context of process variation, the coefficient of variation c_v, as defined earlier was calculated. It is a measure of the extent of variability in relation to the mean of the population. Hence, a low c_v indicates a higher process variation tolerance. From the values obtained in Table V, it



(a) pdf for CMOS VCO (b) cdf for CMOS VCO



(c) pdf for FinFET VCO (d) cdf for FinFET VCO

Fig. 8. Statistical distribution functions for CMOS and FinFET VCO

is seen that the FinFET VCO shows a 2.6% variability, as opposed to 19.7% variability in the CMOS VCO. The bulk CMOS VCO design is more vulnerable to process variation than the FinFET VCO design.

TABLE V
PROCESS VARIATION DATA FOR CMOS AND FINFET VCO

Measurement	μ	σ	$c_v = \sigma/\mu$ (%)
$freq_{CMOS}$	350 MHz	68.9 MHz	19.7
$freq_{FinFET}$	1.92 GHz	49.5 MHz	2.6

VIII. PROPOSED WIDTH QUANTIZATION-AWARE MODELING OF FINFET VCO

Fig. 9 shows the flow of the proposed width quantization aware modeling of the FinFET VCO. First, a regression model of second order is developed, given by Eqn. 9. This equation relates the frequency of the FinFET VCO to the device geometry. Using the coefficients obtained from the model, the matrix of coefficients p_{ij} is created. Then the goodness-of-fit is estimated for the model using the RMSE and R^2. A surface plot is plotted using the matrix p_{ij} relating the oscillation frequency to the number of fins. Detailed explanation of this procedure follows.

As discussed in section V, each fin provides $2 \times H_{fin}$ of device width. The size of each fin determines the increments in device widths available to the circuit designer and multiple fins are required to obtain large widths in a device. For the FinFET technology under consideration, each fin provides a width of 100 nm. So, the FinFET VCO has N_{fin}=10 fins (W=$2 \times H_{fin} \times N_{fin}$=1$\mu$m). In traditional CMOS, the transistor widths are treated as continuous variables which are subjected to continuous optimization techniques [4]. However, in FinFETs the width can only be increased in increments of N_{fin} making it a discrete optimization problem [3].

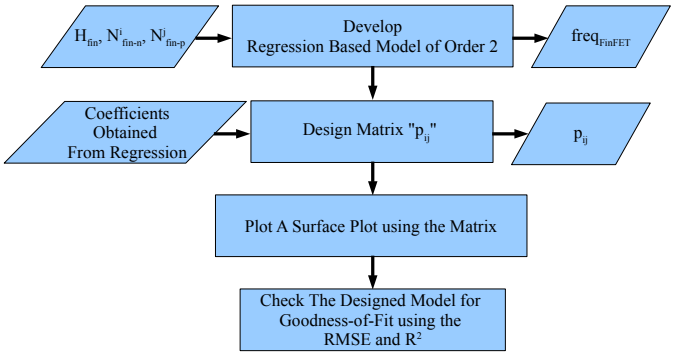


Fig. 9. Flow of proposed width quantization aware modeling of FinFET VCO.

This section presents a width quantization-aware model relating the device geometry to the $freq_{FinFET}$ of the FinFET VCO. This model may be used in discrete optimization techniques. A full-factorial, 4-level experiment for data sampling is used resulting in 2^4=16 runs. Table VI shows the data collected for the full factorial run.

TABLE VI
FULL FACTORIAL RUN FOR THE FINFET VCO

N_{fin-n}	N_{fin-p}	$freq_{FinFET}$
2	6	0.977 GHz
4	6	1.23 GHz
6	6	1.55 GHz
8	6	1.92 GHz
2	8	1.82 GHz
4	8	2.03 GHz
6	8	2.24 GHz
8	8	2.41 GHz
2	10	2.16 GHz
4	10	2.29 GHz
6	10	2.38 GHz
8	10	2.42 GHz
2	12	2.29 GHz
4	12	2.34 GHz
6	12	2.41 GHz
8	12	2.53 GHz

A regression model of order 2 in each of the variables N_{fin-n} and N_{fin-p} is developed, of the form:

$$freq_{FinFET} = 2H_{fin} \sum_{i,j=0}^{2} p_{ij} N^i_{fin-n} N^j_{fin-p}, \quad (9)$$

where p_{ij} is the matrix of coefficients obtained from regression, N_{fin-n} is the number of fins in the n-type FinFET, and N_{fin-p} is the number of fins in the p-type FinFET. As the number of fins can only take an integer value, this becomes a discrete model, which can be used for optimization. The coefficient matrix obtained is given in Eqn. 10. Fig. 10 shows the corresponding surface plot.

$$p_{ij}(freq_{FinFET}) = \begin{bmatrix} 2.366 \times 10^9 & -2.918 \times 10^8 & -4.859 \times 10^6 \\ 5.276 \times 10^8 & 8.692 \times 10^7 & -2.709 \times 10^6 \\ -1.455 \times 10^7 & 7.422 \times 10^6 & -1.072 \times 10^6 \end{bmatrix} \quad (10)$$

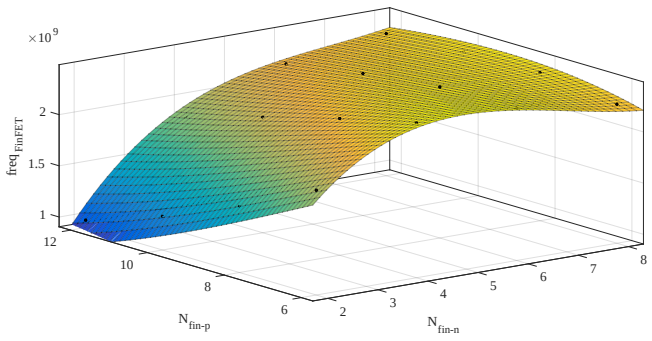


Fig. 10. Surface plot relating oscillation frequency to number of fins.

Similar to section VI, RMSE and R^2 are used to report the goodness-of-fit of the model. Eqn. 11 shows the formula used for calculating RMSE:

$$\text{RMSE} = \sqrt{\frac{1}{M \times N}\sum_{i=0}^{M}\sum_{j=0}^{N}(freq(N^i_{fin-n}, N^j_{fin-p}) - \widehat{freq(N^i_{fin-n}, N^j_{fin-p})})^2}, \tag{11}$$

where $M \times N$ are the data points of the N_{fin-n} and N_{fin-p} parameters selected in the design domain, $freq(N^i_{fin-n}, N^j_{fin-p})$ and $\widehat{freq(N^i_{fin-n}, N^j_{fin-p})}$ are the frequency responses at points (N^i_{fin-n}, N^j_{fin-p}) of the data point observations and the regression based model, respectively. An RMSE of 9.5 MHz for the model was calculated.

R^2 is calculated using Eqn. 12:

$$R^2 = 1 - \frac{\sum_{i=0}^{M}\sum_{j=0}^{N}(freq(N^i_{fin-n}, N^j_{fin-p}) - \widehat{freq(N^i_{fin-n}, N^j_{fin-p})})^2}{\sum_{i=0}^{M}\sum_{j=0}^{N}(freq(N^i_{fin-n}, N^j_{fin-p}) - \overline{freq(N^i_{fin-n}, N^j_{fin-p})})^2}, \tag{12}$$

where $\overline{freq(N^i_{fin-n}, N^j_{fin-p})}$ is the mean of the response at points (N^i_{fin-n}, N^j_{fin-p}) of the data point observations. An R^2 value of 0.9942 for the model was calculated.

IX. Conclusions and Future Research

This paper discusses the process variation and optimization of a FinFET circuit for mixed signal design at nanometer scale. A comparison between two VCOs designed using FinFET and CMOS is presented. The FoMs under consideration are center frequency, $f - V$ characteristics and process variation. The FinFET VCO has a higher center frequency that is 7 times that of the CMOS VCO due to smaller intrinsic gate capacitance. Models have been developed for the $f - V$ characteristics of the CMOS and FinFET VCOs. A width quantization aware model for the FinFET VCO is developed. Process variation analysis models were presented with high accuracy. From the process variation analysis, it is observed that the FinFET VCO shows 2.6% variability due to V_{Th} fluctuations, as compared to 19.7% variability in the CMOS VCO, making it more process variation tolerant. A comparative summary of the proposed VCO with existing VCOs in the literature is presented in Table VII. A direct comparison is not possible as the different works all use CMOS (or derivative) technologies at various node lengths. Moreover these designs cover a wide range of center frequencies. In spite of these differences, Table VII indicates that the current FinFET design is competitive with traditional designs in terms of frequency obtained vs. power expended. As part of future research, thermal effects will be examined, as FinFETs suffer from self-heating. Width quantization-aware models for power consumption will be developed, and discrete multi-objective optimization will be performed using FinFET based mixed signal circuits.

TABLE VII
Summary of VCO Designs from Existing Literature

Research	Technology	Performance (GHz)	Power (mW)	Efficiency (GHz/mW)
Troedsson [32]	250 nm	2.4	5.5	0.44
Dehghani [33]	250 nm	2.5	2.6	0.96
Kwok [34]	180 nm CMOS	1.4	1.5	0.93
Long [35]	180 nm CMOS	2.4	1.8	1.33
Ghai [23]	90 nm CMOS	2.5	–	–
Kaya [19]	50 nm DG MOSFET	6.59	–	–
Current Paper	15nm FinFET	1.8	0.43	4.2

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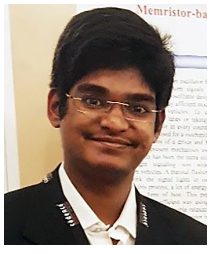

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