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SPECIAL SECTION ON NANO DEVICES, CIRCUITS AND SYSTEMS

SPECIAL SECTION ON NANOELECTRONIC DEVICES AND CIRCUITS FOR NEXT GENERATION SENSING AND INFORMATION PROCESSING

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IEEE

Guest Editorial -- Special Issue on Nanoelectronic Devices and Circuits for Next Generation Sensing and Information Processing

The next generation paradigm of information processing may involve a network of interconnected physical objects such as computers, mobile phones, sensors, actuators, wearable devices, vehicles, homes, buildings, and even energy systems, in which continuous sensing and computing takes place. In such a computing paradigm the vision is to connect a large amount of objects, allow them to collect and exchange data through network connectivity, and consequently utilize the enormous data for analytics and operation. Such as infrastructure provides increasingly smart, reliable and secure services among different things for different users. It has been extensively applied to diverse application domains, such as environmental monitoring, security surveillance, smart power grids, energy-efficient buildings, and interconnected vehicles. To enable next generation sensing, control, and computing, in reality, advanced nanoelectronic devices and circuits must be developed and co-optimized across multiple hierarchical levels in order to sense, process and transmit data, while satisfying the demanding performance requirements for high speed, low power, flexible reconfigurability, high reliability etc. In addition, with the increasing complexity and data volume of sensing and computing, novel designs must be explored to improve design efficiency, enhance reliability and reduce time-to-market. For these reasons, there is an immediate need to re-think the conventional design strategies for implementing the next-generation sensing, control, and computing paradigm.

This special issue focuses on novel device technology and circuit designs to implement smart, efficient, reliable and secure sensing, control, and computing paradigm. The paper submissions were from various venues such as the following: (1) the IEEE-CS Symposium on VLSI (ISVLSI) 2016, (2) the IEEE International Symposium on Nanoelectronic and Information Systems (iNIS) 2015, and (3) open domains. All the submissions have been reviewed rigorously following the guidelines of IEEE Transactions on Nanotechnology (TNANO) through the ScholarOne at https://mc.manuscriptcentral.com/tnano. A majority of the reviewers represent expertize in their fields who provided high quality reviews for the papers. The papers selected through a rigorous reviews process for this Special Issue are briefly discussed in the rest of this guest editorial.

The spin transfer torque magnetic random access memory (STT-MRAM) is considered as a potential nonvolatile memory candidate in the next-generation computer architectures in the emerging computing systems. The major concerns of STT-MRAM include energy consumption and delay. Kang, et al. in "Modeling and Exploration of the Voltage Controlled Magnetic Anisotropy Effect for the Next-Generation Low-Power and High-Speed MRAM Applications" present models and switching strategies for low-power high-speed applications.

In addition to the energy consumption and delay, security is a key issue of emerging computing systems. Due to the global design and manufacturing chain, hardware components of the computing system will have security related challenges including piracy, cloning, counterfeiting, and reverse engineering. The new security primitive called Physical Unclonable Function (PUF) is being explored as a solution of many issues. PUF relies of the process variations of nanoelectronic devices of the hardware components. Uddin et al. in "Robustness Analysis of a Memristive Crossbar PUF Against Modeling Attacks" present design consideration of memristive crossbar based PUFs. The paper considers resilience to two specific machine learning attacks the use of linear regression and support vector machines.

Variability mitigation has been a challenging task for design engineers to enhance the design yield. Process-Voltage-Temperature (PVT) variations mitigation is a required for a good design closure for nanoscale circuits. Chatterjee et al. in "A sub-1V, 120 nW, PVT-variation Tolerant, Tunable and Scalable Voltage

Reference with 60 dB Supply Noise Rejection" present an architecture and design implementation of PVT-variation tolerant voltage reference generator which can operate at extremely low-power.

The graphene nanoribbon tunnel field-effect transistor (GNR-TFET) are getting attention as the future generation nanoelectronic devices for the realization of high-frequency low-leakage integrated circuits. Rawat et al. in "Performance Evaluation of Bilayer Graphene Nanoribbon Tunnel FETs for Digital and Analog Applications" present methods for design and optimization of bilayer GNR-TFET. The device performance is analyzed by quantum transport simulation, based on self-consistent solutions of 2-D Poisson's equation and non-equilibrium Green's function formalism.

The resistive short defects including resistive short defects to supply and resistive short defects to ground are critical for fully-depleted silicon-on-insulator (FDSOI) technology. Karel et al. in "Influence of Body-Biasing, Supply Voltage and Temperature on the detection of resistive short defects in FDSOI technology" present accurate analysis of body biasing, supply voltage, and temperature on the resistive short defects in FDSOI technology.

The three-dimensional (3D) architectures are being explored for future generation circuits and systems for the advantages they provide. Technology like perpendicular-Nano Magnetic Logic (pNML) can enhance the design of large 3D digital circuits. Turvani, et al. in "Towards Exploration of 3D pNML Architectures" present analysis and modeling of pNML circuits for their fast and accurate simulations.

Finally, we thank the authors for their patience and dedication at all stages of the review process. Each manuscript was assigned at least to three reviewers and has undergone multiple rounds of peer-review process. The team of guest-editors sincerely hope that this special issue will be an important reading for contemporary researchers worldwide. The guest editors would like to sincerely acknowledge the Editor-in-Chief of IEEE Transactions on Nanotechnology (TNANO) Dr. Fabrizio Lambardi and his editorial team. The guest editors are extremely thankful to the reviewers for their timely reviews of the submitted manuscripts.

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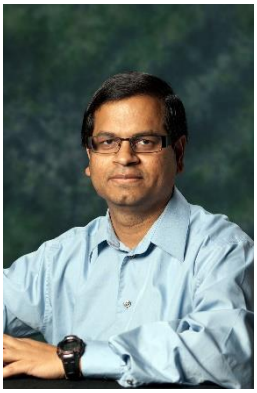

Saraju P. Mohanty (SM'08) is Professor at the Department of Computer Science and Engineering (CSE), University of North Texas (UNT), where he directs the NanoSystem Design Laboratory (NSDL). He obtained a Ph.D. in Computer Engineering from the University of South Florida (USF) in 2003, a Master's degree in Systems Science and Automation (SSA) from the Indian Institute of Science (IISc), Bangalore, India in 1999, and a Bachelor's degree (Honors) in Electrical Engineering from Orissa University of Agriculture and Technology (OUAT), Bhubaneswar, India in 1995. Prof. Mohanty's research is in "Energy-Efficient High-Performance Secure Electronic Systems". Prof. Mohanty received 2016 PROSE Award for best Textbook in Physical Sciences & Mathematics from the Association of American Publishers. He received 2016-17 UNT Toulouse Scholars Award for sustained excellent scholarship and teaching achievements. Prof. Mohanty's research has been funded by the National Science Foundation (NSF), the Semiconductor Research Corporation (SRC), and the USA Air Force. Dr. Mohanty is an inventor of 4 USA patents. Prof. Mohanty is an author of 220 peer-reviewed research articles and 3 books. The publications are well-received by the world-wide peers with a total of 3000 citations leading to an h-index of 27 and i10-index of 80 (from Google Scholar). His latest book titled Nanoelectronic Mixed-Signal System Design is published by McGraw-Hill in 2015 is a best seller. Prof. Mohanty has been serving on the editorial board of several peer-reviewed international journals, including IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), ACM Journal on Emerging Technologies in Computing Systems (JETC), and IET Circuits, Devices & Systems Journal (CDS). He is currently the Editor-in-Chief (EiC) of the IEEE Consumer Electronics Magazine (CEM). He serves as a founding Editor-in-Chief (EiC) of the VLSI Circuits and Systems Letter (VCAL). He has been serving as a guest editor for many prestigious journals including ACM Journal on Emerging Technologies in Computing Systems (JETC) and IEEE Transactions on Emerging Topics in Computing (TETC). Prof. Mohanty currently serves as the Chair of Technical Committee on Very Large Scale Integration (TCVLSI), IEEE Computer Society (IEEE-CS) to oversee a dozen of IEEE conferences. He serves on the steering, organizing, and program committees of several international conferences. He is the founding steering committee chair for the IEEE International Symposium on Nanoelectronic and Information Systems (iNIS) and steering committee vice-chair of the IEEE-CS Symposium on VLSI (ISVLSI). Prof. Mohanty has supervised 8 Ph.D. dissertations and 26 M.S. theses. Eight of these advisees have received outstanding student awards at UNT. He has received Honors Day recognition as an inspirational faculty at the UNT for multiple years. He has also received UNT Provost's Thank a Teacher recognition for multiple years. He is a senior member of IEEE and ACM. More about him is available at: https://www.smohanty.org.

Xin Li (F'17) is currently a Professor in the Department of Electrical and Computer Engineering, Duke University, Durham, NC. From 2007 to 2016, he was a faculty in the Department of Electrical and Computer Engineering, Carnegie Mellon University, Pittsburgh, PA. In 2005, he co-founded Xigmix Inc. to commercialize his PhD research, and served as the Chief Technical Officer until the company was acquired by Extreme DA in 2007. In 2011, Extreme DA was further acquired by Synopsis (Nasdaq: SNPS). From 2009 to 2012, he was the Assistant Director for FCRP Focus Research Center for Circuit & System Solutions (C2S2), a national consortium of 13 research universities (CMU, MIT, Stanford, Berkeley, UIUC, UMich, Columbia, UCLA, among others) chartered by the U.S. semiconductor industry and U.S. Department of Defense to work on next-generation integrated circuit design challenges. From 2014 to 2015, he was the Assistant Director for the Center for Silicon System Implementation (CSSI), a CMU research center with 20 faculty members working on

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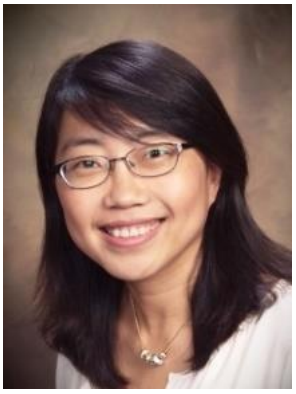

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Dr. Cao was a recipient of the 2012 Best Paper Award at IEEE Computer Society Annual Symposium on VLSI, the 2010, 2012, 2013, 2015 and 2016 Top 5% Teaching Award, Schools of Engineering, Arizona State University, 2009 ACM SIGDA Outstanding New Faculty Award, 2009 Promotion and Tenure Faculty Exemplar, Arizona State University, 2009 Distinguished Lecturer of IEEE Circuits and Systems Society, 2008 Chunhui Award for outstanding oversea Chinese scholars, the 2007 Best Paper Award at International Symposium on Low Power Electronics and Design, the 2006 NSF CAREER Award, the 2006 and 2007 IBM Faculty Award, the 2004 Best Paper Award at International Symposium on Quality Electronic Design, and the 2000 Beatrice Winner Award at International Solid-State Circuits Conference. He has served as Associate Editor of the IEEE Transactions on CAD, and on the technical program committee of many conferences. He is a Fellow of IEEE.