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Simscape® based Ultra-Fast Design Exploration: Graphene-Nanoelectronic Circuit Case Studies

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Abstract SPICE has been the corner stone of integrated circuit simulation since the 1970s. The device-level options that are available for SPICE/analog simulators to simulate a circuit netlist are typically compact models and/or Verilog-A structural and behavioral models. Though these simulations are very accurate, for large and complex circuits/systems they are extremely slow and even computationally infeasible. Thus, as a paradigm shift of the conventional design simulation flow, this paper presents a complete Simscape® based design and simulation flow for ultra-fast design exploration of graphene based nanoelectronic systems. A behavioral model for a dual gate Graphene Field Effect Transistor (GFET) is modeled in Simscape® based on the drift-diffusion conduction mechanism. The kink region of the $I-V$ characteristic is modeled via a displacement current. For case study design circuits, an all graphene based low noise amplifier (LNA) and an LC-tank Voltage Controlled Oscillator (VCO) are presented. The results show that the proposed design alternative to simulate analog circuits and systems is a viable option in addition to the existing SPICE, VHDL-AMS or Verilog-A based flows and can open the way to true device-level system design exploration and optimization. To the best of the authors' knowledge, this is the first ever paper to explore a Simscape® model of a GFET device and design a GFET based radio-frequency (RF) circuit using Simscape®.

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1 Introduction

With the growing demand for integration and shrinking process technology, more and more analog circuits are added into a single chip. It is estimated that at 45 nm and below, more than 60% of SoC designs are re-spined due to mixed signal errors, particularly when crossing domains. Each of these re-spins is expensive in terms of cost ($5-10M) and time-to-market (8-10 weeks delay). Thus from an industrial perspective, it becomes essential to shorten these delays and minimize the cost as much as possible. It would not be an overstatement to say that all AMS-SoC designs undergo through a series of SPICE simulations, at least for the analogue blocks. SPICE has been the obvious choice since the 1970s due to its capability to accurately simulate integrated circuits (ICs) at schematic level (without parasitics) and at layout level (with parasitics) [9]. However there are some trade-offs associated with SPICE simulation in terms of accuracy, cost and complexity. Major drawbacks of SPICE simulations are:

1. Prolonged design times due to heavy computational requirements. This increases the non-recurrent design cost of the chip.
2. Need of fab data or TCAD simulation for accurate compact modeling, which may not always be available especially for new and emerging technologies.
3. Design optimization support is very limited.

In order to overcome these difficulties associated with the SPICE based design flow, this paper proposes a non-traditional design flow which is based on Simscape® and offers two distinct advantages over conventional SPICE simulation:

1. The device level modeling is done using the basic physics and semiconductor principles. Thus, it does not need any fab data for modeling the components, which is very advantageous for emerging technologies, where fab data may not yet be available.
2. It provides fast and easy optimization at system level.

These advantages result in significant reduction in the design cycle time and hence the cost of ICs. The above discussion can be summarized in the following observation: In industrial design, MATLAB® /Simulink® occupy a distinct tool space than SPICE/Verilog-A(AMS). Granted, they are all computational engines but their domain of applicability is very different: MATLAB® /Simulink® is a high level system and design exploration tool as opposed to SPICE/Verilog-A(AMS) which are heavy-duty, device-level, ultra-accurate verification engines. It is practically impossible to perform design space exploration and optimization for the complex designs of today using SPICE: itвЃ™s just too slow even when various “fast-SPICE” approaches (such as table-based models) are used. MATLAB® /Simulink® have traditionally been considered as lightweight approaches while SPICE has always been a true EDA workhorse. This perception is not only erroneous but also quantifiable: MATLAB® /Simulink® costs at least and order of magnitude less than a single commercial SPICE license, without any addons such as RF analyses, behavioral and mixed-signal modeling which come either free at very low cost with MATLAB®,

In this paper, a low-noise amplifier (LNA) is modeled using Simscape® [2] behavioral models of a GFET. The LNA has significant applications in real-life circuits and systems. The model accuracy is verified with data available from MATLAB® [19], SPICE [7], VHDL-AMS [30] or Verilog-A [14] models presented in the existing literature.

The rest of this paper is organized in the following manner: Section 2 discusses the novel contributions of the current paper. Section 3 presents discussions on GFETs and GFET based circuits. Section 4 presents the Simscape model that was developed as part of this work. Section 5 presents a GFET based RF circuit where LNA design is used as the first case study. Section 6 presents a GFET based LC-tank oscillator which is the second case study circuit used in this paper. Section 7 discusses the conclusions and possible directions of future research.

The notations used in the current paper are presented in Table 1.

2 Novel Contributions of this Paper

This paper introduces the first ever Simscape® based design flow for graphene based nanoelectronics. Simscape® is an integral part of the MATLAB® / Simscape® modeling and simulation framework [20, 1, 3]. It is a MATLAB® based, object-oriented language which is designed for modeling physical systems consisting of multiple physical disciplines including electrical, mechanical, optical and hydraulic. The signal-flow modeling approach used in Simscape® is very helpful for high-level system modeling compared to other modeling frameworks. Like the Verilog-A behavioral language, it is capable of modeling conservative systems through a large set of libraries of predefined components which enable rapid model construction while custom designed libraries built using Simscape® help model new emerging components. This facilitates the model-based design exploration at an early developmental stage. Furthermore, Simscape® allows integration and extension of the design scope to multi-discipline designs such as Micro-Electromechanical Systems (MEMS) which is not currently possible with other hardware description languages. Furthermore, optimization options available in the MATLAB® environment assist the selection of critical parameters much more easily than the conventional SPICE simulation tools. By proposing a Simscape® GFET model, an attempt is made to accelerate the research and design exploration processes for multi-discipline, multi-domain design.

Thus, in this paper, a Simscape® [2] behavioral model of a GFET is presented. The model accuracy is verified with data from available MATLAB® [19], SPICE [7] and VHDL-AMS [30] models presented in the literature. The same simulation framework is also used to perform design exploration of two case study RF circuits: a low-input, low-noise amplifier and an LC-tank oscillator.

To the best of the authors' knowledge, this is the first paper ever to present GFET models written in the MATLAB® Simscape® physical modeling language. The novel contributions of this paper to the state-of-art in nanoelectronics based system simulation are the following:

1. A Simscape® based ultra-fast design exploration flow which is non-traditional and a paradigm shift from conventional flows.
2. Modeling of graphene FET devices using Simscape®.
3. Modeling of a GFET based LNA using the Simscape® graphical environment.

Table 1 Notations and definitions used in this paper

Notations used for GFET modeling	
C_e	oxide capacitance
C_q	quantum capacitance
C_{top}, C_{back}	top gate and back gate parasitic capacitance
E	electric field
E_c	critical electric field
$\hbar$	Planck's constant
H_{sub}	substrate thickness
I_{disp}	displacement current
$Ion/Ioff$	transistor ON/OFF current
K	dielectric constant
L	graphene channel length
μ	carrier charge mobility
n	electron concerntration
q	electron charge
R_s	source resistance
t_{ox}	thickness of oxide layer between the top-gate and the substrate
V_0	threshold voltage
V_{bs}, (V_{ds})	back-gate to source (drain to source) voltage
V_{bs}^0, (V_{gs}^0)	back-gate to source (top-gate to source) voltage at the Dirac point
V_{ds-sat}, (I_{ds-sat})	saturation drain to source voltage (current)
υ_{drift}	electron drift current
ν_F	Fermi voltage
υ_{sat}	saturation velocity
W	width of the graphene layer
Notations used in LNA case study	
α , β	weights used in the optimization problem for P_{LNA} and G respectively
C_{in}	input capacitance of LNA circuit
ε	acceptable margin in the perturbation of f_T
E_g	bandgap of bare graphene
$\triangle f_T$	difference in the bandwidth
f_T	bandwidth of LNA
G	gain of LNA
G_1, G_2	load transistor and common source amplifier transistor
g_d	output conductance of transistor G_2
g_m	small-signal transconductance
κ	proportionality constant
L_1, L_2	channel length for G_1 and G_2
P_{LNA}	power consumption
R_L	load resistance of transistor G_1
V_{ch}	channel voltage
W_1, W_2	graphene nanoribbon width for G_1 and G_2
Notations used in LC-VCO case study	
f	cut-off frequency
g_{active}	transconductance of the active device
g_{tank}	total tank conductance
I_{bias}	bias current
L, C	inductance and capacitance in the LC tank circuit
R	resistive loss of the tank due to the parasitic resistance of the inductor
V_{tank}	output voltage swing

4. Experimental validation of the Simscape® device level models with existing VHDL-AMS or Verilog-A models.
5. Characterization of GFET based case study circuits and comparison with Verilog-A based designs.

3 Graphene based Nanoelectronic Circuits

3.1 Graphene FET: Structure

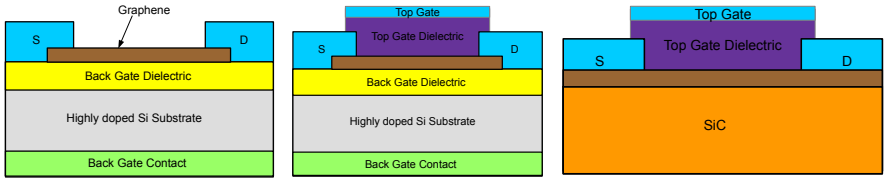
In recent years, several graphene transistor structures have been studied: back-gated graphene transistors, dual-gate graphene transistors and epitaxial graphene from SiC, as shown in Fig. 1 [15]. In the back-gated graphene transistor, as shown in 1(a), the graphene flake is deposited on the top of the substrate making a channel between source and the drain. The substrate acts as a back gate. Since there is no other layer above the graphene (except the passivation layer), it is very likely that the Dirac point mobility and the hysteresis profile of the transistor will vary due to the environment [16]. In Fig. 1(c), graphene is synthesized on silicon carbide wafers (SiC) in order to gain high structural integrity. The biggest advantage of this technique is a precise control of the thickness of graphene at the wafer scale [23].

In this paper, the dual-gate graphene transistor shown in Fig. 1(b) is considered because of two important advantages over other structures: (1) RF performance improves with decrease in gate length by controlling the access resistance through the back gate. This results in an increase in the transconductance. (2) Higher bandgap (200meV). Fig. 1(b) shows a cross-sectional view of such a GFET structure. A single layer of graphene is placed on top of a SiO_2 substrate, which is separated from the top gate by a thin layer of oxide. A back gate lies below the substrate which controls the resistance of a symmetric source-drain arrangement. By applying an electric field perpendicular to the graphene channel, a tunable bandgap can be opened which can then be modulated by the gate voltage. There have been three regions of operation identified for a bilayer GFET: triode region, unipolar saturation region and the ambipolar saturation region. The drain-source $I-V$ characteristics for the triode and the unipolar saturation region are equivalent to that of the MOSFET. However in the ambipolar saturation region, with increase in the drain voltage there is an increase in the drain current. Such a behavior in the ambipolar region is referred as a second linear region. Ambipolar condition occurs when the electrons and holes have the same contribution to the total current whereas in other regions, either electron or hole dominates the total current.

In the following discussion, L denotes the graphene channel length, W represents the width of the graphene layer, t_{ox} denotes the thickness of the oxide layer between the top-gate and the substrate and H_{sub} denotes the substrate thickness. Hafnium oxide (HfO_2) is used as the top-gate dielectric with dielectric constant $K = 16$ and SiO_2 is used as the substrate with $K = 3.9$.

3.2 Graphene FET: Device-Level Models

The two electrodes, namely the top and back gates, act as a parallel plate capacitor with a dielectric layer in between them. This creates an equivalent series parasitic



(a) Back gate graphene transistor (b) Dual gate graphene transistor (c) Epitaxial graphene from SiC and transistor structure

Fig. 1 Different GFET configurations. After [15]

capacitance C_{top} and C_{back}, consisting of top and back components respectively [30,26, 28]. The top component is given by:

$$C_{top} = \left(\frac{C_e C_q}{C_e + C_q}\right), \tag{1}$$

where C_e=ε_{ox}/t_{ox} is the oxide capacitance and C_q is the quantum capacitance. This quantum capacitance is an extra capacitance which originates from the low density states of graphene around the Dirac point. It can act as a barrier in scaling of graphene devices. Due to its linear band structure, the quantum capacitance increases with the square root of the charge density, as given by [19,30]:

$$C_q = \left(\frac{q^2\sqrt{\frac{n}{\pi}}}{v_F \hbar}\right), \tag{2}$$

where q is the electron charge, n is the electron concentration, $v_F \sim 10^8$ cm s^{-1}, and $\hbar$ is Planck's constant. The drain-source current (I_{ds}) of a GFET is given by [30,27]:

$$I_{ds} = W q n v_{\text{drift}}. \tag{3}$$

In the above expression v_{drift} is the electron drift velocity expressed as follows [30,19, 28]:

$$v_{\text{drift}} = \left(\frac{\mu E}{1 + \frac{\mu E}{v_{\text{sat}}}}\right), \tag{4}$$

where E is the electric field, μ is the carrier mobility and v_{sat} is the saturation velocity. $V_{g0} = V_{gs} - V_0$ shows the relation between gate voltage and the threshold voltage, V_0, which is given by the following expression [30,19]:

$$V_0 = V_{gs}^0 + \frac{C_{back}}{C_{top}}(V_{bs}^0 - V_{bs}), \tag{5}$$

where V_{gs}^0 is the top-gate voltage and V_{bs}^0 is the back-gate voltage at the Dirac point which is defined as the point in the electronic band structure of graphene where charge neutrality is obtained [36]. Taking into consideration the source resistance (R_s) and

combining (3)–(5), when $V_{ds} > V_{sat}$ for high negative back gate voltage while forming a p-channel, the drain-source current can be expressed as [30, 19, 28]:

$$I_{ds} = \frac{1}{4R_s}\left(V_{ds} - V_c + I_0R_s + \sqrt{(V_{ds} - V_c + I_0R_s)^2 - 4I_0R_sV_{ds}}\right), \tag{6}$$

where

$$I_0 = 2\left(\frac{W}{L}\right)\mu V_c C_{top}\left(V_{gs} - V_0 - \frac{V_{ds}}{2}\right). \tag{7}$$

In the above expression, $V_c = E_cL$ and E_c is the critical electric field.

For the condition, $V_{ds} \leqslant V_{sat}$,

$$I_{ds} = I_{ds-sat} + I_{\text{disp}}, \tag{8}$$

In the above expression, I_{disp} is the displacement current [30] and the critical voltage V_{ds-sat} is given by the following [30, 27]:

$$V_{ds-sat} = \frac{2\gamma V_{g0}}{1+\gamma} + \frac{1-\gamma}{(1+\gamma)^2}\left(V_c - \sqrt{V_c^2 - 2(1+\gamma)V_cV_{g0}}\right) \tag{9}$$

where γ is a coefficient given by:

$$\gamma = R_s\left(\frac{W}{L}\right)\mu C_{top}V_c. \tag{10}$$

The saturation current I_{ds-sat} is given by [30, 27]:

$$I_{ds-sat} = \frac{\gamma}{R_s(1+\gamma)^2}\left(-V_c + (1+\gamma)V_{g0} + \sqrt{V_c^2 - 2(1+\gamma)V_cV_{g0}}\right). \tag{11}$$

In the above expression, the displacement current I_{disp} is expressed as follows [30]:

$$I_{\text{disp}} = \left(\frac{W}{L}\right)\mu C_{back}\left(\mid V_{bs} - V_{bs}^0 \mid\right)\frac{V_{ds}}{10}\left(\frac{V_{ds}}{V_{ds-sat}} - 1\right)^2. \tag{12}$$

3.3 Graphene FET Based Circuits

The unique properties of graphene, such as high carrier mobility and saturation velocity, high stability, and low noise, make graphene a good candidate for high frequency electronic applications. Since the I_{on}/I_{off} ratio of graphene is very low, its application in digital circuits has been questionable but recent results have suggested that using sophisticated technology, these GFETs can also be used for digital circuits. For example, dual-gate and bi-layer GFETs in [34] were measured to have an I_{on}/I_{off} ratio of 100. These GFETs have been used in all analog, digital as well as RF circuits such as inverters [11, 25, 29], frequency multipliers [33, 31, 24], an RF mixer [32], amplifiers [35, 10], a photo detector [21], and low-noise amplifiers (LNAs) [5, 4]. The concept of wafer scalable analog circuits was verified with an RF mixer example in [18]. Apart from these analogue, digital and RF applications, graphene is also considered crucial in bioelectronics due to its large surface-to-volume ratio, excellent electrical and optical properties, high thermal conductivity, carrier mobility and density [22, 6].

In the current work, an LNA and an LC oscillator are chosen as case study circuits for GFET based circuit design utilizing the Simscape graphene model. Both are important components in wireless communication systems. They are employed to amplify weak signals and are located close to the antenna in order to minimize loss and maximize signal-to-noise ratio (SNR).

4 Simscape® Modeling of Graphene FET

The proposed Simscape® GFET model is based on the VHDL-AMS model from [30] or the Verilog-A model from [14] so that previously published results can be used for the validation of the new models.

This subsection briefly explains the GFET modeling in the Simscape® environment. A physical component is designed in Simscape® using three sections: declaration section, setup section and an equation section, as shown in Fig. 2.

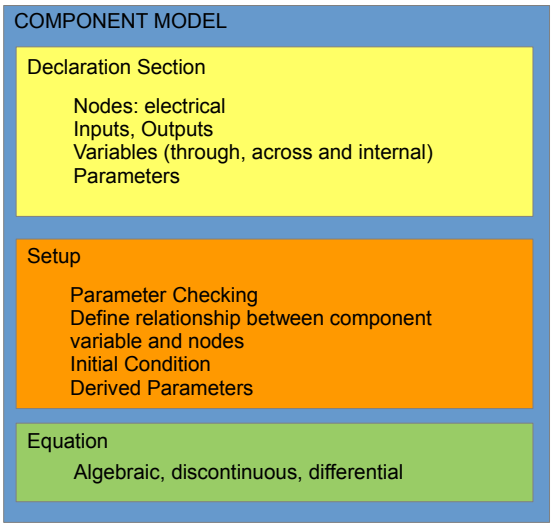


Fig. 2 Simscape simulation setup for GFET device simulation. After [2].

The declaration section starts with the keyword "component" which specifies that a component is being designed in the Simscape® built-in domain. In this section, component members (like nodes, inputs, outputs, variables, parameters) are declared. The nodes define the physical ports and reuse the Simscape® physical domain to create domain compatible components. The GFET has four nodes defined as S, G, D, BG for source, gate, drain and back gate respectively. Variables are then defined, which are used in the equation sections. The last part in the declaration section are the parameters, which are the values that users can change. Both variables and parameters are needed to be defined along with their units.

The next section is the setup section, which is used to validate parameters, compute derived parameters, set initial conditions and define relationships between nodes and variables. The "across" and "through" variables are also defined here. This section is executed once per component instance during model compilation, using regular MATLAB®.

The final section is the equation section, which establishes mathematical relationships among component variables, inputs, outputs, time and time derivatives. The set of equations from 1 to 12 are used order to model the GFET in Simscape®. In the equation part, conditional statements can be defined using "if" statements as used

in MATLAB®. The "==" operator is used to specify the symmetrical mathematical relationship and has nothing to do with assignment or logical operation.

Once the model is written in Simscape®, it needs to be built for later use in Simulink®, where the circuit/system is designed using that component, as shown in Fig. 3. In order to build the component in Simscape®, two conditions need to be satisfied: (1) the packet directory must begin with the "+" sign, and (ii) the parent of the top level directory must be in the MATLAB® path. After satisfying these two requirements, the model can be built using the "ssc_build" command in the MATLAB® command window, which then generates the .mdl model in the parent of the top level directory. The complete proposed Simscape® model for the GFET is presented in Algorithm 1.

In order to compare the proposed Simscape® model with other well accepted models, this work considers the GFET model based on the VHDL-AMS model from [30] and the Verilog-A model from [14]. The Simscape® simulation results show good agreement with the prior results presented in [30,27,26,13,19].

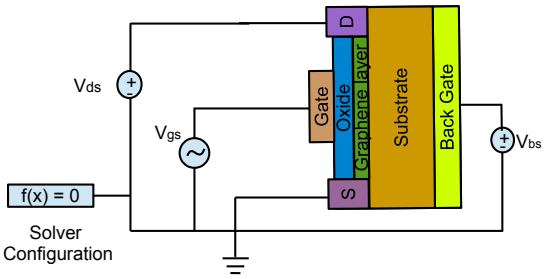


Fig. 3 Simscape simulation setup for GFET device simulation.

In order to demonstrate the applicability and accuracy of the Simscape® based design simulation flow, the following two sections demonstrate two test circuits as case studies.

5 Case Study 1: GFET based Amplifier Circuit

5.1 Theoretical Perspective

In its simplest form, an LNA consists of a common source amplifier and a load. Fig. 4 shows the schematic diagram of such a simple, all-graphene LNA [4]. In this circuit, G_1 acts as a load and G_2 acts as a common source amplifier transistor. The graphene nanoribbon widths W_1 and W_2 for devices G_1 and G_2 are chosen as the design variables. The gain (G), bandwidth (F_T) and power consumption (P_{LNA}) are considered as the figures-of-merit (FoMs) of the LNA. Due to its simplicity, this circuit is amenable to exhaustive design exploration and is one of the reasons for its adoption: as a test case to validate the Simscape® model presented in Section 4 within the MATLAB® /Simulink® framework. For brevity, the design of the matching pair is not presented.

I_{ds} vs. V_{gs} and I_{ds} vs. V_{ds} characteristics of device G_2 in the LNA are shown in Fig. 5(a) and 5(b), respectively. The results obtained from the simulation for the amplifier

Algorithm 1 Proposed model for a GFET.

```
component GT
    nodes
    p1 = foundation.electrical.electrical; % S:top
    p2 = foundation.electrical.electrical; % G:top
    p3 = foundation.electrical.electrical; % D:top
    p4 = foundation.electrical.electrical; % BG:bottom
    end
    parameters
            Rs = {800, 'Ohm'};
            mu = {700,'cm^2/s/V' };
            Ec = { 4.5e5,'V/m' };
            Cgio = { 0.8072,'1' };
            Hsub = { 285.0e-9,'m' };
            tox = { 15e-9, 'm' };
            L = { 1e-6, 'm' };
            W = { 2.1e-6, 'm' };
            ntop = { 2.1209e16,'cm^-3' };
            Vgs0 = { 1.45, 'V' };
            Vbs0 = { 2.7, 'V' };
            k = { 16, '1' };
            k_sub = { 3.9, '1' };
            pi = { 3.1415926, '1' };
            q = { 1.60e-19, 'c' };
            eps0= { 8.854187817e-12, 'F/m' };
            h= { 6.62606876e-34, 'J*s' };
            vf={1e6,'m/s'};
    end
    variables
            Vds= {1,'V'};
            Ids={1,'A'};
            Vgs= {1,'V'};
            Vbs= {1,'V'};
            Ctop ={1,'F/cm^2'};
            Cback ={1,'F/cm^2'};
            Vo ={1,'V'};
            Vg0 ={1,'V'};
            Vc ={1,'V'};
            Rc ={1,'Ohm'};
            Gamma ={1,'1'};
            Vdsat ={1,'V'};
            Io={1,'A'};
     end
     function setup
        across(Vds, p3.v, p1.v);
        through(Ids, p3.i, p1.i);
        across(Vgs, p2.v, p1.v);
        across(Vbs, p4.v, p1.v);
     end
     equations
        let
            Cq = q^2*(ntop/pi)^0.5/(vf*(h/(2*pi)))
            Ce = Cgio*eps0*k/tox;
        in
            Ctop == Cq*Ce/(Cq+Ce);
        end
        Cback == eps0*k_sub/Hsub;
        Vo == Vgs0 + (Cback/Ctop)*(Vbs0 - Vbs);
        Vg0 == Vgs - Vo;
        Vc == Ec*L;
        Rc == 1.0/((W/L)*mu*Ctop*Vc);
        Gamma == Rs/Rc;
     Vdsat == (2*Gamma*Vg0/(1+Gamma)+ (1-Gamma)/(1+Gamma)^2*(Vc-(Vc^2-2*(1+Gamma)*Vc*Vg0)^0.5));
        Io == 2.0*(W/L)*mu*Vc*Ctop*(Vgs-Vo-Vds/2.0);
        if (Vds > Vdsat)
            Ids == 1/4/Rs*(Vds-Vc+Io*Rs + ((Vds-Vc+Io*Rs)^2 - 4*Io*Rs*Vds)^0.5);
        else
           if (Vds <= Vdsat)
          Ids == (Gamma/Rs/(1+Gamma)^2*(-Vc+(1+Gamma)*Vg0+(Vc^2-2*(1+Gamma)*Vc*Vg0)^0.5) +
              mu*Cback*abs(Vbs-Vbs0)*Vds*W/L/10*(Vds/Vdsat -1)^2);
           else
              Ids == 0.0;
           end
        end
    end
end
```

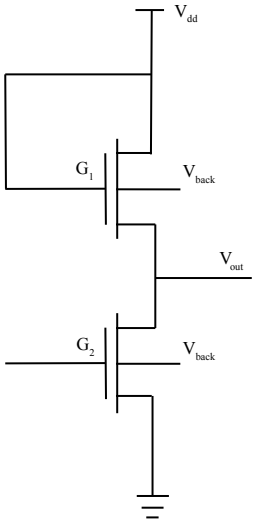
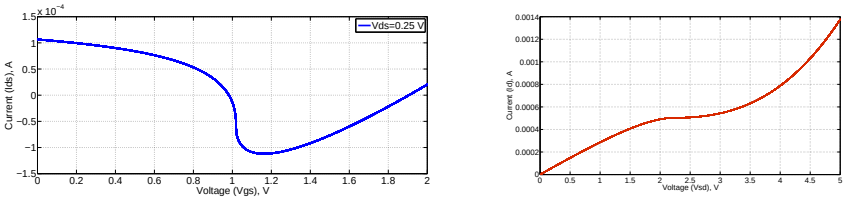


Fig. 4 Schematic of a GFET based LNA circuit. G_1 is the load transistor and G_2 is the amplifier.

transistor closely match published data [5, 19]. In particular, the kink in I_{ds} is accurately modeled by the inclusion of a displacement current.



(a) I_{ds} vs. V_{gs}. (b) I_{ds} vs. V_{ds}.

Fig. 5 GFET charasteristics (amplifier device G_2 in the LNA).

5.2 Simscape® Modeling of the LNA

For simulation of the LNA, the transistor configuration is modified. The Simscape® based simulation setup is presented in Fig. 6. In the LNA simulation, GFETs with $T_{ox} = 1$ nm, $H_{sub} = 2.85$ nm, and $L = 50$ nm were used. W was varied for both transistors for all simulations. Fig. 7 shows the relation of R_L, E_g, and g_m with the width of the transistor. From the result, it can be observed that R_L, E_g, and g_m are inversely proportional to W.The results match those presented in [4].

The result in Fig. 8 shows the inverse relationship between the bandgap and gain as demonstrated in [4]. Similarly, Fig. 9 shows the relationship between bandwidth and the load resistance under constant gain G=15.75 dB. Finally, as shown in Fig. 10, the

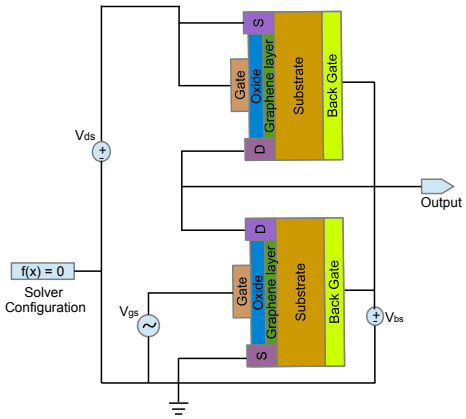
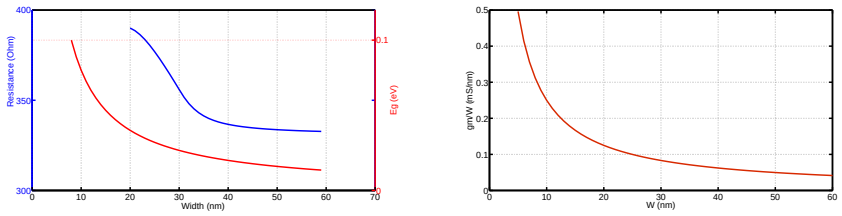


Fig. 6 Simscape® Experimental setup for LNA simulation.



(a) R_L and E_g vs. W (b) g_m/W vs. W

Fig. 7 GFET based LNA charasteristics.

GFET based LNA is shown to have a small-signal bandwidth of 3.119 GHz. Table 2 summarizes the basic characteristics of the LNA for two different transistor sizes.

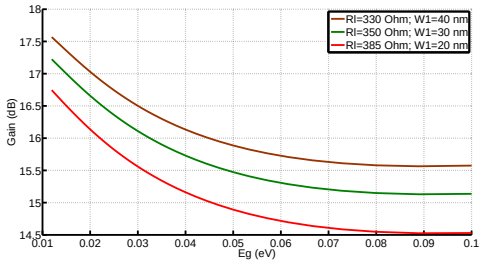


Fig. 8 Gain (G) vs. E_g at different R_L values.

6 Case Study 2: Graphene based Oscillator Design

The second case study circuit considered is an oscillator circuit.

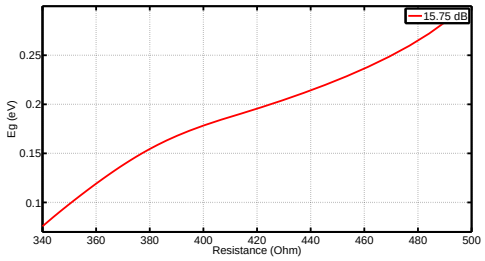


Fig. 9 E_g vs. R_L at constant $G = 15.75$ dB.

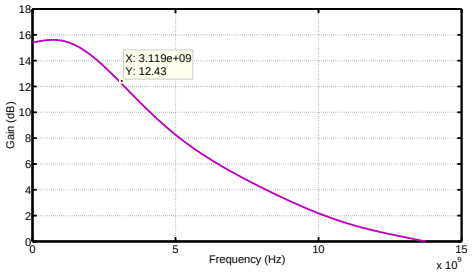


Fig. 10 The simulated frequency characteristics of the GFET based LNA.

Table 2 GFET based Amplifier Figures-of-Merit

Parameter	Value 1	Value 2
W_1	20 nm	30 nm
W_2	10 nm	15 nm
Gain (G)	14.54 dB	15.41 dB
Bandwidth (f_T)	3.12 GHz	3.12 GHz
Power (P_{LNA})	23.8 mW	27.2 mW

6.1 Theoretical Perspective

Oscillators are widely used in data communication systems and are the most important components of Phase-Locked Loops (PLLs) [8]. Due to their high carrier mobility even at room temperature, GFETs can be used for high speed and high frequency communication systems. In order for GFETs to be useful as building blocks for analog and digital electronics, they must exhibit intrinsic gain (i.e. ratio of transconductance to output conductance) greater than 1. However recent reports have shown that over-unity voltage gain has been achieved at room temperature, which enabled the use of GFETs in analogue electronics [25]. [17] shows that GFETs with a cut-off frequency of 100-300 GHz have been fabricated. An LC oscillator oscillates at a frequency given by the following expression:

$$f = \left(\frac{1}{\sqrt{LC}}\right). \tag{13}$$

Fig. 11 shows the schematic of the cross-coupled oscillator considered in this paper. NFETs are used to set an appropriate bias point. Back gate and top gate voltages are applied to control the threshold voltage following equation (5) [30]. In order to

create an n-type channel, the top gate voltage is biased positively as compared to the threshold voltage and to create a p-type channel, the top gate voltage is biased negatively compared to the threshold voltage [27]. Fig. 12(a) and Fig. 12(b) show the $I-V$ characteristics of NFETs for different top gate voltages.

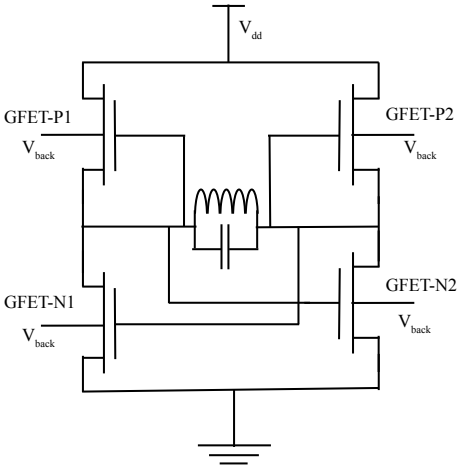
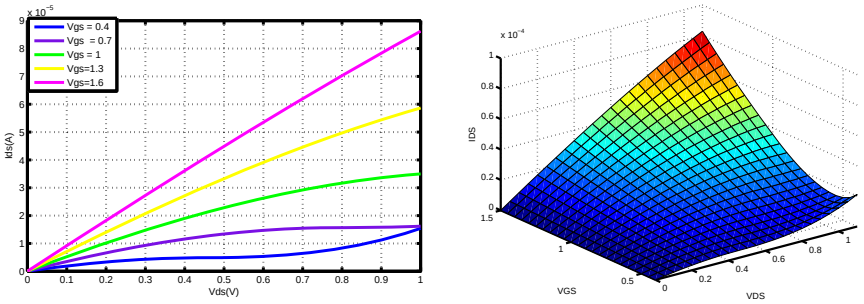


Fig. 11 Schematic of LC oscillator using GFET



(a) I_{ds} Vs V_{ds} (b) I_{ds} Vs V_{ds}

Fig. 12 (a) $I-V$ characteristic of NFET for different top gate voltages. (b) Surface plot showing $I-V$ curve for continuous change of the top gate voltage.

In order to start the oscillation, the transconductance of the active device should follow the following expression:

$$g_{active} \geq \left(\frac{RC}{L}\right), \tag{14}$$

where R is the resistive loss of the tank due to the parasitic resistance of the inductor. The transconductance of the active device is controlled by modifying the parameter W while keeping the channel length of both PFET and NFET fixed. The relationship

between transconductance and width W is illustrated in fig. 7(b). This relationship also depends on the operating region. In the current limited region, the output voltage swing is defined by:

$$V_{tank} = \left(\frac{I_{bias}}{g_{tank}}\right), \tag{15}$$

where I_{bias} denotes the bias current and g_{tank} is the total tank conductance. When the oscillator enters the voltage limited region, the output voltage amplitude is limited by supply voltage and the operating region of active device.

6.2 Simscape® Modeling of the Oscillator

To configure the n-channel transistor, the critical electric field (Ec) is set to 15 KV/m [34]. The back gate voltage and width of the channel are characterized to obtain the desired bias point. Fig. 13 shows the Simscape® based simulation setup. In order to perform accurate simulation, the solver used in this paper is ODE14X (Extrapolation), which has the minimum possible step size. The PFETs are arranged in a cross coupled topology and are characterized to operate close to the saturation region, as shown in Fig. 14(a). In order to achieve over unity intrinsic gain, the source to drain conductance is reduced. The back gate voltage is set to obtain the appropriate charge neutral point and so the desired bias point.

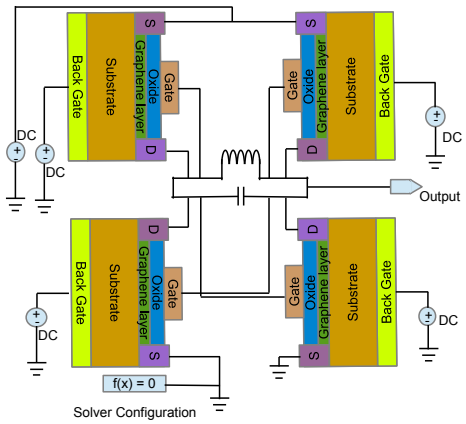


Fig. 13 Simscape® model of GFET based oscillator.

Figs. 14(b), 14(c), 14(e), and 14(f) illustrate the desired curves to obtain the required transconductance and drain conductance parameters. Fig. 14(d) shows the obtained drain current and drain voltage curve. Table 6.2 summarizes the basic features of the oscillator. The oscillator is designed to operate at an 1.8 GHz frequency having tank voltage swing 1.286 V(p-p), as shown in Fig. 15. Eqn. 15 suggests that the tank amplitude should be higher but the operation region of the active device limits this amplitude. Since in a GFET saturation does not persist for large operating regions, to keep the output voltage swing in the inductive limited region, either the bias current has to be increased or the tank conductance has to be reduced. But if either step is

taken, oscillation does not start up. Hence this can be cast as an optimization problem and will be examined in future research. The Simscape® based LC-VCO results are consistent with the Verilog-A results discussed in [14]. Thus, the proposed Simscape® based design flow generates consistent results as the well-proven traditional design flows.

Table 3 GFET based Oscillator characterization.

GFET Oscillator Characteristics	Estimated Values
f	1.8 GHz
$V_{tank}(p-p)$	1.286 V
I_{bias}	4.6 mA
g_{tank}	0.1336 mS
g_{active}	4.6787 mS
g_{ds}	1.7238 mS

7 Conclusions and Future Research

A Simscape® based behavioral model of graphene FETs, suitable for design exploration at high levels of abstraction has been presented in this paper. The model has been verified by extensive $I-V$ characterization of the GFET. As a case study, two circuits (LNA and LC-VCO) are considered and the results are compared with well-accepted traditional models. The results obtained in this paper show that the Simscape® based model can be used as a substitute for more detailed but time consuming traditional simulations such as SPICE with Verilog-A and VHDL-AMS models. Thus the ability to perform mixed high-level (behavioral) and transistor-level simulations for RF systems with an integrated design environment provides RF designers with unique design exploration and verification tools.

As an extension of this research, complete designs (such as the matching circuit of the LNA) and additional functionalities for noise, transfer function and non-linear RF analyses such as periodic and quasi-periodic steady state can be incorporated within the Simscape® model. Optimization techniques using particle swarm-based optimization (PSO) algorithms such as artificial bee colony and ant colony optimization for GFET based circuits will be explored within MATLAB® /Simscape®.

Acknowledgments

A shorter version of this research is presented in the following paper: [12]. The authors would like to thank UNT graduates Dr. G. Zheng, Mr. M. Gautam, and Mr. A. Khan for their help and inputs on this paper.

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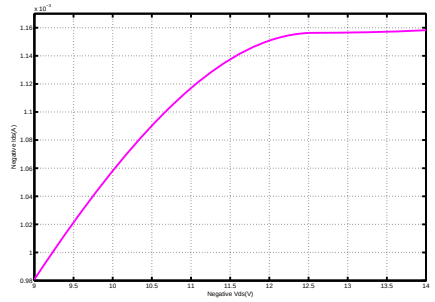
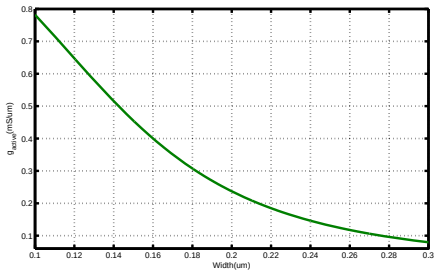
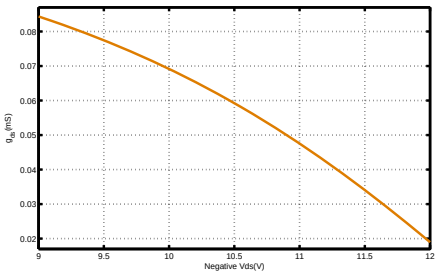


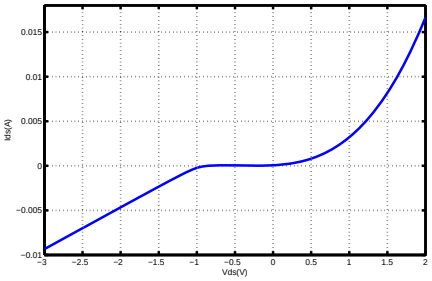
(a) I_{ds} Vs V_{ds}



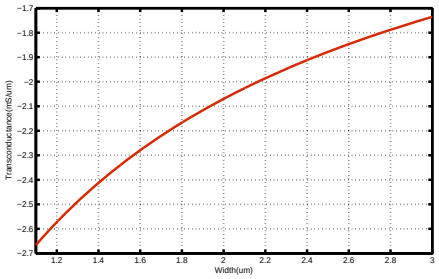
(b) g_{active} Vs W



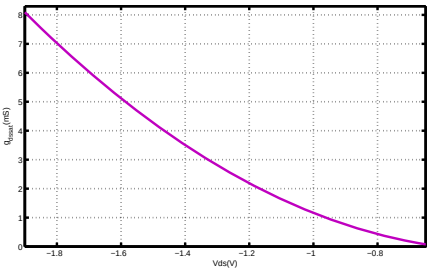
(c) g_{ds} Vs V_{ds}



(d) I_{ds} Vs V_{ds}



(e) g_{active} Vs W



(f) g_{active} Vs V_{ds}

Fig. 14 (a) $I-V$ characteristic of PFET around operating point. (b) Transconductance of PFET for variation in width. (c) Drain to source conductance of PFET encompassing operating point. (d) $I-V$ characteristic of NFET around operating point. (e) Transconductance of NFET in saturation for different widths. (f) Drain to source conductance of NFET in saturation.

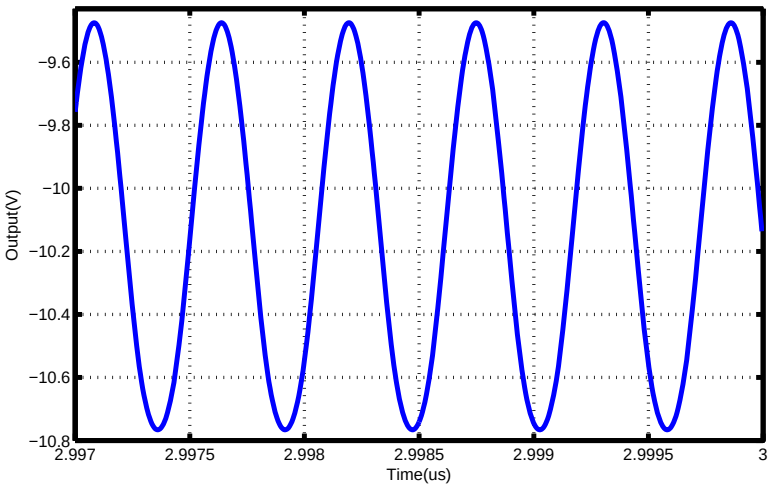


Fig. 15 Simulation of the Simscape® based GFET oscillator.

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