Impact of Channel Hot Carrier Effect in Junction- and Doping-free Devices and Circuits

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***Abstract*—In this brief, we have investigated the time dependent performance degradation of digital benchmark circuits due to channel hot carrier (CHC) stress in junction- and doping-free devices. For device-circuit interaction, we have developed the look-up table based Verilog-A models of both devices for circuit simulations. At device level, the drain current of conventional n-type junctionless (JL) FET is degraded by 20-25%, however, dopingless JLFET experiences 10-15% degradation in drain current due to CHC stress of different time spans. The circuit level simulations of digital benchmark circuits, such as standard six-transistor static random access memory (SRAM) cell, and ring oscillator (RO) have large impact of CHC stress. For example, operating frequency of RO designed with conventional JLFET is degraded by 3.3 to 5 times due to CHC stress of 2000s and 6000s. Similarly, read and write delays of SRAM cell are also degraded by CHC stress conditions.**

***Index Terms*- Junctionless FET, Dopingless FET, Channel Hot Carrier (CHC), Verilog-A Models, SRAM, and Ring Oscillator.**

I. Introduction

The electrical characteristics of junctionless field effect transistors (JLFETs) have outpaced the conventional MOSFETs on many fronts, such as better scalability and gate controllability, and simplified fabrication process [1]. Apart from that n-type JLFET has also been investigated for the time dependent performance degradation due to channel hot-carrier (CHC) stress and experimentally found less sensitive than conventional inversion mode MOSFETs [2], [3]. The CHC stress in JLFETs is mainly triggered by the impact ionization phenomenon due to high electric field in the channel near drain region. The high energetic electrons and holes generated by impact ionization are injected into the gate-dielectric region near the drain side, thereby interface states are generated that degrades the electrical characteristics of JLFETs [4]. However, higher doping concentration to meet driving current requirement and higher gate workfunction to turn-off the device properly for JLFET poses severe challenges, among them impact ionization and threshold voltage variability due to random dopant fluctuations (RDFs) are critical [5], [6].

In that pursuit, dopingless (DL) JLFET has recently been proposed as a potential candidate that relaxes the aforementioned requirements, and preserves all the benefits of conventional JLFET. The DL-JLFET employs intrinsic silicon nanowire for formation of source and drain regions through charge-plasma [7], thereby, provides better immunity towards process variation induced RDFs [8]–[10]. In this brief, a comparative investigation of time dependent performance degradation due to CHC stress at device and circuit level is performed for both JLFET (junction free device with heavy doping) and DL-JLFET (free from external doping as well as junctions) using device-circuit co-simulation approach. We have considered the most damaging CHC condition for short-channel devices when $V_G = V_D$ at room temperature, whereas, in long-channel devices it occurs when $V_G = V_D/2$ [11]. Several studies on JLFETs have been performed in the recent past at device level for time dependent degradation [12], [13], however, for the first time we have investigated the impact of CHC stress of different time spans in digital benchmark circuits, such as standard six-transistor static random access memory (SRAM) cell and an 11-stage ring oscillator. For device-circuit co-simulation, we have developed the look-up table based verilog-A models for both devices with pre- and post-CHC stress of different time spans.

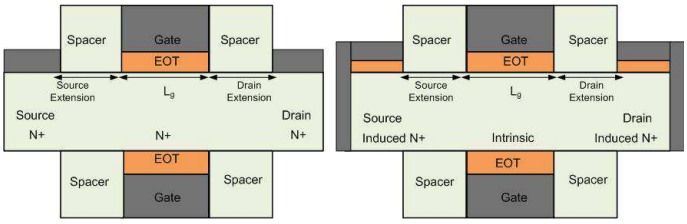

Fig. 1. Cross-sectional views of test devices for CHC stress (a) conventional JLFET [14], and (b) dopingless JLFET [8].

Fig. 1 (a-b) show the cross-sectional views of both conventional and doping-less JLFET. The device dimensions for both devices are kept same except doping concentrations and gate work functions. The parameters used in our simulation are [8], [9]: silicon film thickness (T_{si})=10nm, gate length (L_g)=15nm, effective oxide thickness (EOT) =1nm, and S/D extension (L_{ext})=15nm. The gate metal work function in conventional n-type JLFET is 5.5eV with uniform doping throughout source/channel/drain ($10^{19}cm^{-3}$). Similarly, for n-type DL-JLFET, the gate work function is taken as $4.73eV$ with intrinsic silicon body ($10^{15}cm^{-3}$). In DL-JLFET the doped source/drain regions are formed with different metal electrodes work functions, referred as charge-plasma [8] which are in the range of $\phi_m < \chi_{Si}$+(E_G/2q), where, χ_{Si} is electron affinity of bulk silicon (χ_{Si} = 4.17), E_G is the bulk silicon

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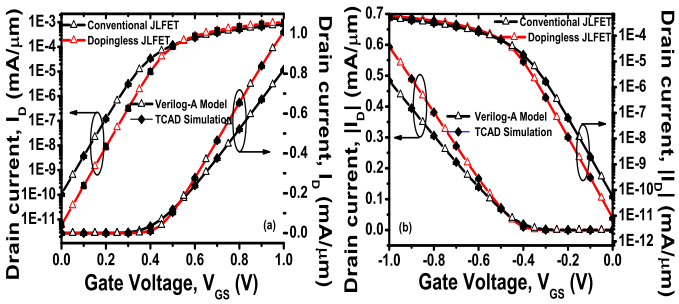

Fig. 2. Calibration of Verilog-A models (open symbols) with TCAD simulations (solid symbols) for transfer characteristics of both conventional (JLFET) and dopingless (DL-JLFET) device (pre-CHC) at V_{DS}= $\pm 1V$ (a) n-type, and (b) p-type.

bandgap, q is elementary charge. The Hafnium (work function = $3.9eV$) metal contact is used to create the source/drain region over a silicon layer of thickness $10nm$. For conventional and dopingless p-type JLFET, we considered the gate work function of 3.96eV and 4.86eV, respectively.

Our device-circuit co-simulation framework comprises of extraction of electrical (I-V and C-V) characteristics through 2-D TCAD simulations and development of look-up table based Verilog-A models. At device level simulations, both conventional JLFET [14] and DL-JLFET [8] are adopted with same device dimensions and parameters as reproduced in Fig. 1 (a-b). Initially, both fresh (pre-CHC stress) devices were simulated with bias conditions varying finely over the operating range. The resulting extracted electrical (I-V and C-V) characteristics of both devices through dc and ac simulations are then used in look-up table based Verilog-A models to perform circuit simulations in Cadence (Spectre). The fine-granularity TCAD simulations were performed for extraction of I_{DS} (V_{GS}, V_{DS}), C_{GS} (V_{GS}, V_{DS}) and C_{GD} (V_{GS}, V_{DS}) for the development of 2-D look-up table based Verilog-A models. We have calibrated our Verilog-A models with TCAD simulation for both n-type and p-type devices, and reproduced the previously reported transfer characteristics of both conventional JLFET and DL-JLFET, as shown in Fig.2 (a-b). It can be observed that the developed Verilog-A models for both n- and p-type, JLFET and DL-JLFET show very good agreement with TCAD simulations.

II. CHC Stress and Simulation Framework

To study the impact of CHC stress on both devices, we have employed a conventional cumulative measure-stress-measure approach [15]. The CHC stress was applied with V_G = V_D=1.9V for 2000 seconds and 6000 seconds with device degradation models, and drain current variation was monitored. The output characteristics were observed at room temperature before CHC stress (pre-CHC) and at selected time after CHC stress (post-CHC) using TCAD simulations. During CHC stress, the variation of drain current was monitored by sweeping the drain voltage for various gate bias voltages. The

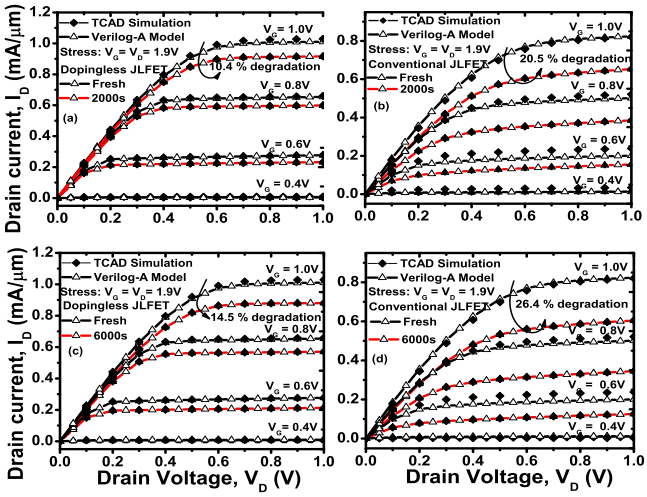

Fig. 3. Output characteristics of conventional and dopingless n-type JLFETs fresh and stressed (V_G = V_D = 1.9 V) for 2000 seconds (a-b), and 6000 seconds (c-d).

resulting stressed device electrical characteristics (I-V and C-V) are then used in look-up table based Verilog-A models for circuit level simulation in Cadence (Spectre).

The output characteristics of conventional and dopingless JLFETs under hot carrier stress (V_G=V_D=1.9V for 2000s and 6000s) were obtained from TCAD simulations (solid symbols), as shown in Fig.3 (a-d). The extracted output characteristics through Verilog-A models (open symbols), we have followed the same look-up table based approach in which resulting stressed device electrical characteristics (I-V and C-V) were incorporated, as shown in Fig.3 (a-d). It can be observed that the Verilog-A models follow TCAD simulations very closely for both fresh and stressed devices. For CHC stress of 2000 seconds, conventional JLFET experiences drain current degradation of 20.5 $\%$ in contrast to dopingless JLFET of 10.4$\%$ for V_G = V_D = 1.9 V, as shown in Fig.3 (a-b). Degradation in drain current for both devices is mainly occurred due to shift in threshold voltage under CHC stress. However, for lower gate biases both devices experienced less degradation in drain current which is consistent as well as in line of applied electric field.

The time dependent degradation in drain current due to CHC stress was also observed for 6000 seconds, where drain current degradation was slightly higher for both devices, as shown in Fig.3 (c-d). From these transfer characteristics, one can inferred that the conventional JLFET experiences higher degradation due CHC stress as compared to its counterpart dopingless JLFET. Higher degradation of drain current in conventional JLFET is due to highly doped channel and high gate work function metal electrode that causes injection of abundant carriers in the drain side oxide region, as a result, significant shift in threshold voltage occurs. However, degradation in drain current of DL-JLFET is comparatively low due to intrinsic channel and lower gate work function metal electrode that leads to reduction in electric field, and thereby ensured high

TABLE I. PERFORMANCE (IN GHZ) OF RING OSCILLATORS (ROS) BASED ON CONVENTIONAL AND DOPINGLESS JLFETS

Stress conditions	Devices (JLFETs)	Supply voltage (V)		
		0.5	0.7	0.9
Without stress	Conventional	2.3	5.4	8.0
	Dopingless	6.1	11.6	16.8
With 2000s	Conventional	0.69	1.8	2.8
	Dopingless	5.0	10.1	15.7
With 6000s	Conventional	0.46	1.2	1.6
	Dopingless	4.5	9.9	15.2

reliability against impact ionization and hot carrier effects.

III. RESULTS AND DISCUSSION

From above simulations and observations, it can be inferred that the time dependent CHC stress degrades the conventional JLFET drain current more severely than dopingless JLFET. However, projection of this device level drain current degradation to circuit level performance estimation may be difficult, so we have developed a device-circuit co-simulation approach that effectively captures the device electrical characteristics. This approach is computationally efficient and allows simulation of complex circuits. Here, we have considered two benchmark circuits for evaluation of both devices under pre- and post-CHC stress for different time spans. An 11-stage ring oscillator (RO) was designed with both devices by incorporating their Verilog-A models. Fig.4 (a-b) shows the simulated transient (1ns) output characteristics of ROs for dopingless and conventional JLFETs under pre- and post-CHC stress of 2000s. The operating frequency of a conventional JLFET based RO is reduced by the factor of 3.3 in contrast to fresh device (pre-CHC stress), whereas, RO based on dopingless JLFET has insignificant (18%) effect of CHC stress.

Similarly, for a CHC stress of 6000s the performance of conventional JLFET based RO is degraded by 5× in contrast to fresh device, whereas, RO based on dopingless JLFET has only exhibited a degradation of 26% due to CHC stress, can be seen from Fig.4 (c-d). Table I also summarizes the performance of RO realized with convectional and dopingless JLFETs for pre- and post-CHC stress at different supply voltages. It can be observed that the operating frequency of RO degrades significantly from fresh (pre-CHC) to post-CHC stress of 2000s for both devices. However, for longer time stress (6000s) the performance of RO degraded less due to less shift in threshold voltages. Therefore, degradation in drain current of 20-25% in conventional JLFET and 10-15% in dopingless JLFET have sever impact on the operating frequency of ring oscillator due to CHC stress.

Another benchmark circuit that we have considered is a standard six-transistor static random access memory (SRAM) cell realized with conventional and dopingless JLFETs. For successful realization of any technology node or device structure SRAM cell is crucial circuit designed under several constraints. In this brief, we have only considered the transient analysis of a RO and SRAM cell. However, static analysis of

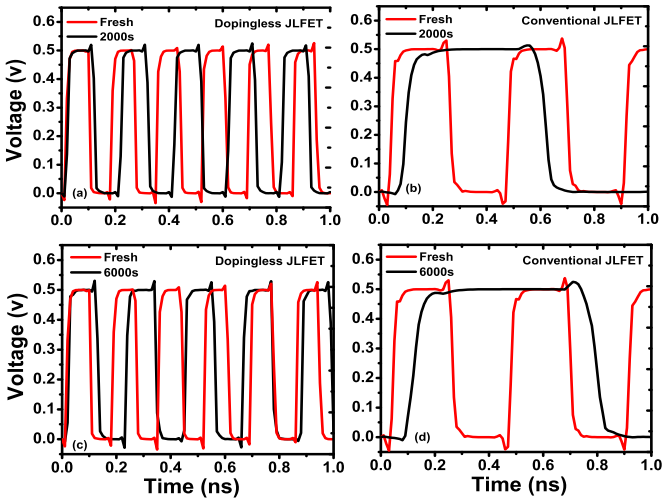

Fig. 4. Transient output characteristics of ROs based on conventional and dopingless JLFETs. Performance degradation of ROs due to CHC stress condition (V_G=V_D=1.9 V) for 2000s and 6000s, dopingless JLFET based RO (a-c), and conventional JLFET based (b-d).

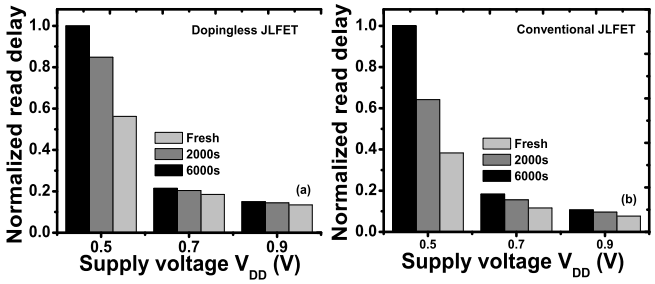

Fig. 5. Normalized read delay for dopingless and conventional JLFET based SRAM cells at various supply voltages and CHC stresses.

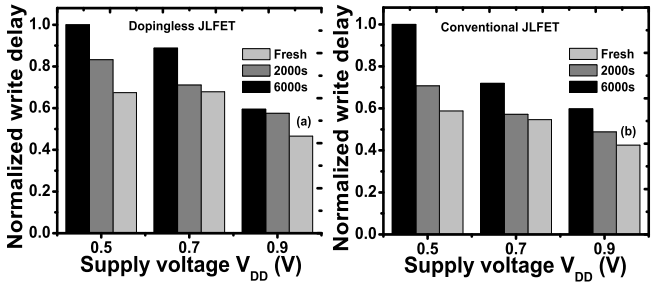

Fig. 6. Normalized write delay for dopingless and conventional JLFET based SRAM cells at various supply voltages and CHC stresses.

SRAM cell is equally important which includes estimation of hold, read, and write static noise margins [9]. So, transient read and write delays performance parameters of SRAM cell were observed under pre- and post-CHC stress conditions of different time spans and supply voltages. The dopingless JLFET based SRAM cell experiences 43% degradation in read delay, whereas, conventional JLFET based SARM cell read delay degraded by 62% for CHC stress of 6000s and supply voltage of 0.5V, as shown in Fig.5 (a-b). Similarly, write delay of SRAM cell based on dopingless JLFET degraded by 32%, and for counterpart SRAM write delay is degraded by 41% for CHC stress of 6000s and supply voltage of 0.5V, as shown in Fig.6 (a-b).

IV. Conclusion

We observed that the CHC stress causes significant drain current degradation in conventional JLFET as compared to its counterpart dopingless JLFET. The proposed device-circuit co-simulation offers a computationally efficient and accurate way to translate the device level performance degradation to the circuit level. From TCAD and Verilog-A simulations, it is inferred that the initial phase (2000s) of CHC stress is more crucial than the longer one (6000s) for both devices and circuits. Hence, investigated results at circuit level may provide incentives and guidelines for further exploration of dopingless JLFETs.

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