Guest Editorial

Special Section on Circuit and System Design Methodologies for Emerging Technologies

The demand for ever smaller, portable, energy-efficient and high-performance electronic systems has been the primary driver for CMOS technology scaling. As CMOS scaling approaches physical limits, it has been fraught with challenges that required introduction of newer materials, manufacturing processes and device structures. High-κ oxide and metal-gate stack was introduced to mitigate oxide leakage which became a significant concern for sub-65nm CMOS technologies. Thin body, undoped channels, and multiple-gate structures were introduced to mitigate subthreshold leakage as battery life for mobile devices rose to prominence. 3D transistors such as double-gate FinFET and trigate transistors have been introduced to improve ON current and reduce subthreshold leakage without compromising layout efficiency that is crucial for device density which leads to lower costs. These innovations have allowed sustained scaling of CMOS technology which will continue to dominate semiconductor manufacturing for reasons that are both technological and financial. In CMOS technology, charge conveys logic information. Movement of charge is central to computation and storage, which entails a minimum energy dissipation of the order k_B*T per switching event. It has been argued that energy dissipation defines the fundamental limit of CMOS scaling.

As an alternative to CMOS, a large variety of devices have been proposed for energy-efficiency and performance. Among them are carbon nanotube (CNT) field-effect transistors (CNT-FETs), graphene filed-effect transistors (GFETs), tunnel transistors, graphene nanoribbon tunnel field-effect transistors (GNR-TFET), quantum-dots, and single-electron devices (SET). At the same time newer memory technologies such as resistive random-access memory (RAM), memristors, Spin Transfer Torque Random Access Memory (STT-RAM) have shown promise to revolutionize the design landscape of electronic systems. However for these alternative technologies to become practical, design methodologies that allow efficient modeling, design space exploration, and trade-off analysis is crucial for the success of nanoelectronic circuit and system design. This is the driving motivation for this special section/issue of IEEE Transactions on Emerging Topics in Computing (TETC).

For this special issue, after an intensive peer-review process, a total of 4 papers have been selected. The paper titled “Scaling Effects on Static Metrics and Switching Attributes of Graphene Nanoribbon FET for Emerging Technology” by Yaser M. Banadaki and Ashok Srivastava presents static metrics and switching attributes of GNR FETs for scaling of device the channel length up to 2.5nm. The article “Performance Improvement in SC-MLGNRs Interconnects using Interlayer Dielectric Insertion” by Atul K. Nishad and Rohit Sharma discusses an analytical model for time domain analysis of side-contact multilayer graphene nanoribbons (SC-MLGNRs). The articles titled “Errors and Power when Communicating with Spins” which is authored by Erol Gelenbe focuses on the analysis of error probabilities for bipolar spin based nano-communication between a set of interfering of nodes. The article titled “Powering Up Dark Silicon: Mitigating the Limitation of Power Delivery via Dynamic Pin Switching” by Shaoming Chen, *et al*. introduces techniques to power-up dark-silicon by dynamically switching a portion of I/O pins to power pins. These articles provide significant contributions to the state-of-art in nanoelectronic circuits and system design methodologies. This special issue/section well-serves the community of students and researchers in the field.

The guest editors are indebted to the reviewers for the quality and timeliness of their reviews. The reviewers are experts in their fields and their feedbacks have enhanced the quality of the final submissions for this issue. We thank the authors for their patience, diligence and dedication at all stages of the review

process. We are grateful to Dr. Fabrizio Lambardi, Editor-in-Chief (EiC), IEEE Transactions on Emerging Topics in Computing (TETC), for making this special issue/section possible.

Sincerely,

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Saraju P. Mohanty is a Professor at the Department of Computer Science and Engineering, University of North Texas, where he directs the NanoSystem Design Laboratory (NSDL). Prof. Mohanty's research is in "Low-Power High-Performance Secure Electronic Systems". Dr. Mohanty is an inventor of 4 US patents. Prof. Mohanty is an author of 50 peer-reviewed journal articles, 130 peer-reviewed conference publications, and 3 books. The publications are well-received by the world-wide peers with a total of 2,300 citations leading to an h-index of 24 and i10-index of 60 (from Google Scholar). Prof. Mohanty currently serves as the Chair of Technical Committee on Very Large Scale Integration (TCVLSI), IEEE Computer Society (IEEE-CS). He has been serving on the editorial board of several peer-reviewed international journals and magazines. He currently serves on the editorial board of 4 peer-reviewed international journals, IET Circuits, Devices & Systems Journal, Elsevier Integration Journal, Journal of Low Power Electronics, and IEEE Consumer Electronics Magazine. He serves on the organizing and program committee of several international conferences. He was a general chair for IEEE-CS Symposium on VLSI (ISVLSI) 2012 and 2014. Prof. Mohanty is a senior member of IEEE and ACM. Prof. Mohanty has advised/co-advised 6 Ph.D. dissertations and 22 M.S. theses. Seven of these advisees have received outstanding student awards at UNT. He has received Honors Day recognition as an inspirational faculty at the UNT for multiple years. He has also received UNT Provost's Thank a Teacher recognition for multiple years. He is a senior member of IEEE and ACM.

Sandip Kundu is a Professor of the Department of Electrical and Computer Engineering at the University of Massachusetts, Amherst. Previously, he was a Principal Engineer at Intel Corporation and Research Staff Member at IBM Corporation. He has published well over 200 papers and holds 12 patents, given more than a dozen tutorials at conferences. He was the Technical Program Chair of ICCD in 2000, Program Co-Chair of ATS in 2011, ISVLSI in 2012 and 2014, DFTS in 2014 and General Chair of ICCD in 2001 and Co-General Chair of VLSI in 2005 and DFTS in 2015. He is a Fellow of IEEE and JSPS. He has also been a distinguished visitor of the IEEE Computer Society. He has served as an associate editor of the IEEE Transactions on Computers, IEEE Transactions on VLSI and ACM Transactions on Design Automation. Currently, he serves as an associate editor of the IEEE Transactions on Dependable and Secure Computing.