Incorporating Manufacturing Process Variation Awareness in Fast Design Optimization of Nanoscale CMOS VCOs

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***Abstract*— This paper proposes a novel fast and unified mixed-signal design methodology by incorporating manufacturing process variation awareness in power, performance, and parasitic optimization. The design of a process variation aware Voltage Controlled Oscillator (VCO) at nano-CMOS technologies is demonstrated as case study. Through accurate simulations it is shown that process variations have a drastic effect on performance metrics such as the center frequency of the VCO. In the presence of worst-case process variation, performance optimization of the VCO is applied, along with a dual-oxide technique for power minimization. The final product of the proposed process-variation aware methodology is an optimal physical design. The proposed methodology achieves 25% power reduction (including leakage) with only 1% degradation in center frequency compared to the target, in the presence of worst-case process variation and parasitics, with a 41% area penalty.**

***Index Terms*— Nanoscale CMOS, Manufacturing Process Variations, Low-Power Design, Voltage Controlled Oscillator (VCO).**

I. Introduction and Motivation

The design cycle of analog and mixed-signal circuits is complicated by the impact of process variation on performance due to the use of state-of-the-art nanoscale CMOS technologies [1]. Such variations are caused by the imperfections in the nanoscale CMOS fabrication processes, such as sub-wavelength lithography, lens aberration, and chemical-mechanical polishing [2], [3], [4]. The process point, which is the center of the distribution of the parameters for a given process, may not be the best design point for maximizing yield of the circuit being manufactured. There is a pressing need to optimize the design such that it operates as specified across the entire process and operating environment to enhance the yield and reduce cost.

Meeting simultaneous low power and high performance objectives is a daunting challenge [5], [6]. Acceptability, reliability, and profitability of the circuits depend on variation tolerance, power efficiency, and performance along with yield. Power dissipation has significant impact on every budget of circuit design, whether technological or financial. Existing applied low-power design methods targeted to reduce power consumption may lead to penalties on the circuit performance. On the other hand, power-aware design refers to maximizing performance metrics, subject to a power budget. One of the many issues for mixed-signal circuits is that the exact performance prediction is very challenging due to the presence of large parasitics [5], [6]. Unfortunately, before the circuit is implemented and layout is obtained, it is difficult to estimate the parasitic effects. The objective of this paper is to present a novel design methodology that incorporates manufacturing process variation awareness in power and performance, and produces a parasitic-optimal design for general nano-CMOS mixed-signal components.

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The Voltage-Controlled Oscillator (VCO) is an important part of wireless communication systems, especially in frequency synthesizers and Phase-Locked Loops (PLLs). To demonstrate the proposed process-variation aware design flow, a current-starved topology based nano-CMOS VCO is designed along with its physical design and full parasitic re-simulation and characterization. The center frequency is one of the most critical performance parameters of a VCO. Thus, this paper deals with the optimization of the center frequency as a VCO performance parameter.

The rest of the paper is organized as follows: The novel contributions of this paper are summarized in Section II. Related prior research is discussed in Section III. Section IV presents the proposed flow for optimal design of the VCO. A new fast process variation aware statistical analysis method is presented in Section V. Section VI discusses the baseline design of the VCO for a 90 nm CMOS technology. The proposed algorithm for optimization of the VCO is presented in Section VII. The paper is concluded with discussions on future research in Section VIII.

II. Novel Contributions of this Paper

To appreciate the serious problem of process variation, refer to Fig. 1 for a 90nm CMOS VCO. As can be seen from the bottom curve, a degradation of 43.5% is observed when the VCO is subjected to *worst-case process variation*. In this analysis, the logical design of a 90 nm VCO is first performed for a target oscillation frequency $f_0 \geq 2$ GHz, and its frequency-voltage characteristics are obtained through analog transistor-level simulation. Then the physical design of this 90 nm VCO follows and its frequency-voltage characteristics are also obtained using the same simulator on the fully parasitic netlist extracted from the layout. Due to parasitics, the frequency-voltage characteristic of the physical design shows a 22% degradation compared to the logical design which further degraded to 43.5% when the VCO is

subjected to worst-case process variation. Thus, there is a need for design methods to account for this degradation at an early stage in the design cycle to achieve the highest possible yield.

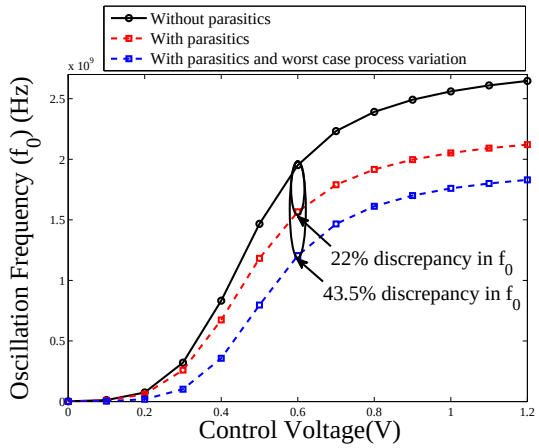


Fig. 1. Frequency-voltage characteristic degrades when the parasitic-extracted physical design is subjected to worst-case process variation.

The key idea of the proposed solution explored in this paper is depicted in Fig. 2. The important point is to obtain information of process variation and perform statistical modeling of Figures-of-Merit (FoMs) of the design. The models are then used for statistical estimation and optimization of the circuit during the design flow. For example, based on manufacturers' data, the device parameters are modeled as probability density functions (PDFs) such as $L(\mu, \sigma)$, $W(\mu, \sigma)$ and $V_{th}(\mu, \sigma)$ and the FOMs are estimated as PDFs such as Power(μ, σ) and Frequency(μ, σ) over which design optimization is performed.

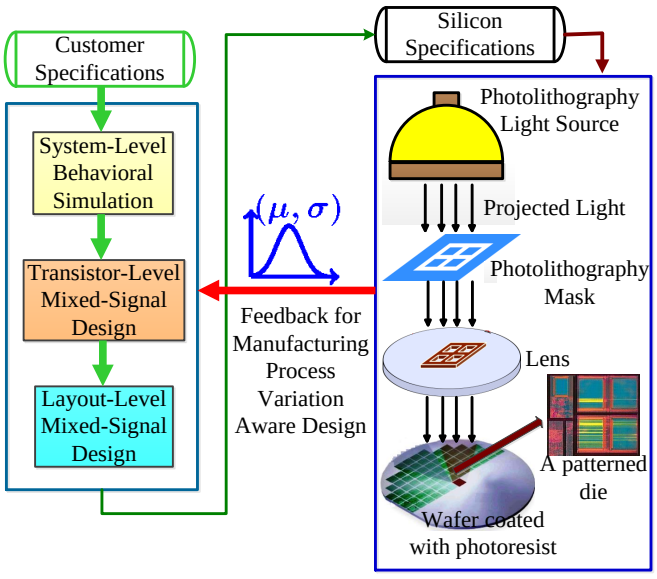


Fig. 2. Incorporating manufacturing process variation in early design to enhance chip yield.

The **novel contributions** of this paper to advance the state-of-the-art are as follows:

1) A process variation aware design flow is proposed in the context of power, performance, and parasitic optimization of nano-CMOS mixed-signal circuits. The significance of this novel process variation aware methodology is that it achieves an optimal layout in one design iteration, compared to multiple iterations in traditional layout design. Thus, it can be used for fast design optimization of nano-CMOS mixed-signal circuits. This is extremely significant for the reduction of time-to-market in the current highly competitive semiconductor industry.
2) A novel statistical analysis flow for fast and accurate estimation of characteristics while accounting for process variation. The flow is based on a design of experiments (DOE) assisted Monte Carlo technique to perform fast statistical analysis with minimal accuracy trade-off.
3) An algorithm is proposed for process variation aware optimization of VCOs over the statistical FoMs expressed as probability density functions.
4) Power optimization of the VCO has been achieved using a dual-oxide process approach. Although the dual-oxide technique has been explored for digital circuits, it is relatively new for analog circuits [7].
5) As a specific case study of the proposed process variation aware design flow, design and characterization of a 90 nm CMOS VCO is presented.

III. Related Prior Research

Process variation in analog circuits [8] and power-aware design is on the research forefront. In [9], a PVT-tolerant PLL design is proposed. In [10], an analysis of the process parameters affecting a ring oscillator's frequency performance is presented. In [1], a current-controlled oscillator has been subjected to process variations. The process mismatch of an ADC is discussed in [11]. PVT-tolerant phase noise minimization of an LC-VCO is presented in [12]. Parasitic aware design to overcome degradations due to device and package parasitics to achieve optimal performance are presented in [6]. Simulated annealing is used for synthesizing RF power amplifiers in [13]. In [14], an LC-VCO has been subjected to parasitic-aware synthesis. A simulation-based circuit synthesis example is given in [15] but does not include the layout parasitics in the design.

The power consumption of VCOs has received much attention due to their significance in RF circuits and systems. In [16], low-power consumption is achieved using two cross-coupled fully integrated high-inductance VCO cores. In [17], a transformer-feedback based VCO is proposed to achieve low-power designs at sub-threshold voltages. When power and performance (oscillation frequency) are compared, the nano-CMOS VCO resulted from our proposed methodology shows excellent performance compared to other VCO designs reported in the recent literature (Table I).

IV. Proposed Process Variation Aware Fast Design Methodology

To mitigate process variation effects in nanoscale design a novel design flow that incorporates such effects in early phases is discussed. The flow includes a novel analysis method for quantifying the impact of process variation with respect to

TABLE I
POWER AND PERFORMANCE OF SELECTED CURRENT-STARVED VCOS.

Research	Technology	Performance	Power
Ham [18]	350 nm	1.91 GHz	10 mW
Tiebout [16]	250 nm	1.8 GHz	20 mW
Dehghani [19]	250 nm	2.5 GHz	2.6 mW
Hajimiri [20]	250 nm	1.8 GHz	6.0 mW
Long [21]	180nm	2.4 GHz	1.8 mW
Kwok [17]	180 nm	1.4 GHz	1.46 mW
Ghai [5]	90 nm	2.54 GHz	–
This Paper	90 nm dual-oxide	2.3 GHz	158 μW

oscillation frequency in which the worst-case process variation is identified. The flow also includes a process variation aware optimization algorithm for statistical optimization.

The proposed design flow is presented in Fig. 3. The design flow ensures that the resulting physical design is not only resistant to nanoscale process variations, but also is a low-power design and is highly accurate as the parasitic effects are also accounted for. The proposed flow is a major advancement from our previous research [5] in terms of the new fast statistical analysis methods as well a new process variation aware optimization algorithms.

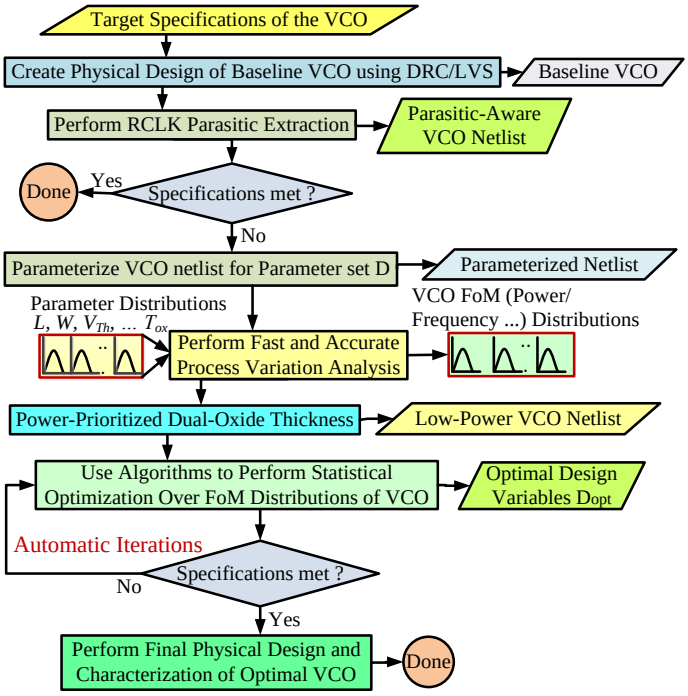


Fig. 3. The proposed novel process variation aware design flow which obtains an optimal physical design of a VCO in a single manual iteration compared to multiple manual iterations of a standard flow.

Once the logical design is performed to meet the required specifications, an initial physical design is made as presented in Section VI. This layout is subjected to parasitic ($RCLK$) extraction that includes resistance (R), capacitance (C), self-inductance (L) and mutual inductance (K) for the interconnect as well as the active devices. The parasitic netlist is then parameterized for the parameter set D (widths of transistors and T_{oxpth}, T_{oxnth}). At this stage, a worst-case process variation analysis of the physical design with respect to VCO performance (e.g. center frequency) is performed using the new methodology presented in Section V.

This is followed by a circuit-level low-power technique: "power-prioritized dual-oxide assignment" is used to minimize power consumption of the VCO circuit. In this approach, a thick-oxide assignment (T_{oxpth}, T_{oxnth}) is performed to the power-hungry transistors (NMOS, PMOS) of the VCO for power and performance tradeoff. However, other circuit-level low-power techniques (or combinations thereof) can also be used at this step. The parameterized-parasitic netlist is then subjected to a process variation aware statistical optimization loop discussed in Section VII in order to meet the specifications (power and performance) in a worst-case process-variation environment. Other algorithms can also be used at this step for optimization. Once the parameter values for which the specifications are met are obtained, a final physical design of the VCO is created using these parameter values.

In this design flow, a *single design iteration approach* is followed, in which the layout is performed only twice. Once before the optimization, and once with modifications, after the optimization. The *elimination of manual steps is very significant* for design cycle time and non-recurrent cost minimization. It reduces chances of layout errors that manual steps would more easily generate. Thus, the proposed flow can handle large and complex nanoscale mixed-signal designs in reasonable time with minimal resource usage.

V. DESIGN-OF-EXPERIMENT ASSISTED MONTE CARLO FOR FAST PROCESS VARIATION ANALYSIS

In the proposed flow, the identification of worst-case or average process variation effects with respect to characteristics of the VCO is important. Traditional Monte Carlo simulations typically used in current practice are very slow. For example, a 1000 Monte Carlo run over an 180 nm CMOS PLL with full parasitics takes 5 days even in a high-end server. So, a new method called Design-Of-Experiments assisted Monte Carlo (DOE-MC) is proposed here for fast statistical analysis as shown in Fig. 4. A worst-case or average process variation statistical analysis of the physical design is performed using the parameterized parasitic-aware layout-netlist. In the DOE-MC approach, a very small number of Monte Carlo runs are used for each trial of DOE. For n number of process parameters a full factorial design has 2^n trials. Then 2^n intermediate probability density functions $\text{PDF}_i\,(\mu_i, \sigma_i)$ are obtained. The PDF of the target figure-of-merit (FoM) is calculated as the average of the intermediate PDFs. In other words μ_{FoM} is the average of μ_is and σ_{FoM} is the average of σ_is.

As a specific example, four process parameters, along with the power supply, are considered in this design: (1) V_{DD}: supply voltage, (2,3) $V_{t(n,p)}$: (N,P)MOS threshold voltage, (4,5) $T_{ox(n,p)}$: (N,P)MOS gate oxide thickness. For the identification of the worst-case process variation, a *five factor, two level full factorial experiment* is performed, where *level 1:* nominal-10% (represented by '$-$') and *level 2*: nominal+10% (represented by '$+$'). "Nominal" is the nominal value of the parameter specified in the process design kit (actual values

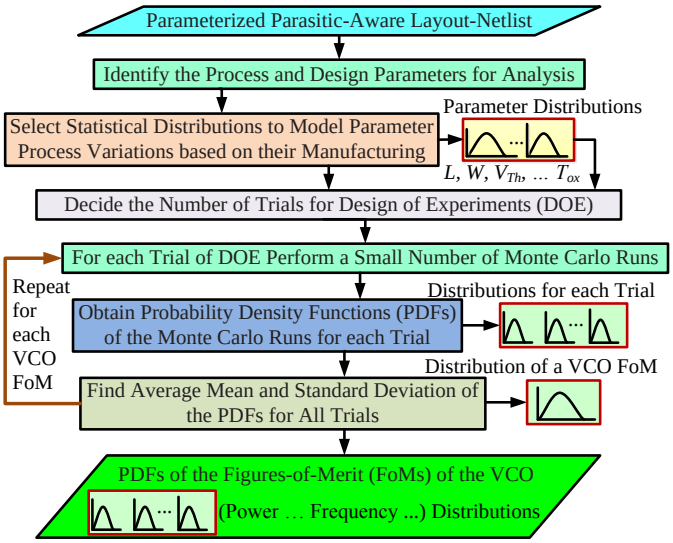


Fig. 4. Proposed Design-of-Experiment assisted Monte Carlo (DOE-MC) for fast process variation analysis.

are shown in Table III). Considering that typical CMOS manufacturing processes at 90 nm have a standard deviation of 3-5% of the mean, a 10% value results in a 2σ - 3σ coverage. Two levels were selected since the objective of the experiment is *screening* (i.e., identification of the important factors) rather than modeling, in which case 3 or more levels could be used. The value of f_0 is recorded for every trial. Fig. 5 shows the values of f_0 for the 32 trials. The points have been grouped to indicate the effect of one factor, T_{oxp} and each pair of points corresponding to the $+$ and $-$ settings for T_{oxp}, with all other factors constant, is termed a "Run", for a total of 16 runs as shown in Fig. 5. Similar plots can be generated for the other factors. Table II shows the parameter settings for each trial of the experiment. For example, the two endpoints of Run 1 in Fig. 5, correspond to the two settings shown in Table II for Run 1. From the above experiment, the worst-case process variation for f_0 is identified to be the one in which V_{DD} is reduced by 10%, and all the other process parameters (V_{tn}, V_{tp}, T_{oxn}, T_{oxp}) are increased by 10%, causing a degradation of 43.5% in f_0. The worst-case process-variation values of these characteristics are presented in Table III for the 90 nm CMOS based VCO whose design is discussed in Section VI.

VI. Design and Characterization of a 90 nm CMOS based Current-Starved VCO

A. Design of the 90nm CMOS Baseline VCO

The current-starved VCO topology shown in Fig. 6 comprises of three stages: 1) An input stage consisting of two transistors with high impedance. 2) An odd numbered chain of inverters along with two current-source transistors per inverter, which limit the current flow to the inverter. 3) An output buffer stage.

The operating frequency of the VCO, f_0 is determined using the following expression [22], [23]:

$$f_0 = \left(\frac{I_{inv}}{NC_{inv}V_{DD}}\right), \tag{1}$$

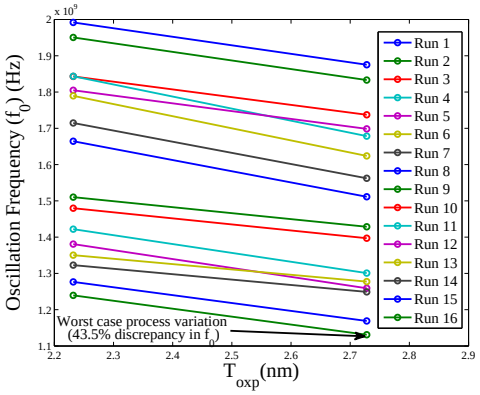


Fig. 5. Effect of parameter variation on oscillation frequency (f_0) of the VCO for the parameter T_{oxp}.

where V_{DD} is the supply voltage, I_{inv} is the current flowing through each identical inverter, N is the odd number of inverters and C_{inv} is the total capacitance given by the sum of the input and output capacitances of each inverter stage. f_0 can be mainly controlled by an applied DC input voltage, which adjusts the current I_{inv} through each inverter stage. C_{inv} is given by [22]:

$$C_{inv} = \left(\frac{5}{2}\right) C_{ox}(W_pL_p + W_nL_n), \tag{2}$$

where C_{ox} is the gate-oxide capacitance per unit area, W_n and W_p are the widths and L_n and L_p are the lengths of the inverter NMOS and PMOS transistors, respectively. C_{ox} is calculated from [22]:

$$C_{ox} = \left(\frac{\epsilon_{SiO_2}\epsilon_0}{T_{ox}}\right), \tag{3}$$

where ϵ_{SiO_2} is the relative dielectric constant of SiO_2, ϵ_0 is the vacuum dielectric constant and T_{ox} is the gate-oxide thickness. Also, the threshold voltage V_t is affected by the gate-oxide thickness T_{ox} along with other parameters [24]:

$$V_t = V_{fb} + 2\phi_F + \left(\frac{T_{ox}}{\epsilon_{SiO_2}}\right)\sqrt{2q\epsilon_{Si}N_{sub}\,(2\phi_F + V_{bs})}, \tag{4}$$

where V_{fb} is the flat-band voltage, V_{bs} is the body bias, γ_{body} is the body effect coefficient, and ϕ_F is the Fermi level.

Combining Eqn. 1, 2, 3, and 4 the following expression is formulated for f_0:

$$f_0 = \left(\frac{I_{inv}(V_t - V_{fb} - 2\phi_F)}{N\left(\frac{5}{2}\right)\left(\epsilon_0\sqrt{2q\epsilon_{Si}N_{sub}(2\phi_F + V_{bs})}\right)}\right) \times \left(\frac{1}{(W_pL_p + W_nL_n)\,V_{DD}}\right). \tag{5}$$

For the baseline design, f_0 has been kept at a minimum of 2 GHz. The number of stages is fixed to 13 for high frequency requirement. For the baseline design, $L_n = L_p = 100$ nm, $W_n = 250$ nm and $W_p = 2 \times W_n = 500$ nm are chosen. C_{inv} is calculated using Eqn. 3. Finally, I_{inv} is calculated using Eqn. 1, and the current-starved NMOS and PMOS devices are sized to provide the required current I_{inv}. Thus, the sizes $L_{ncs} = L_{pcs} = 100$ nm, and $W_{ncs} = 500$ nm, and $W_{pcs} =$

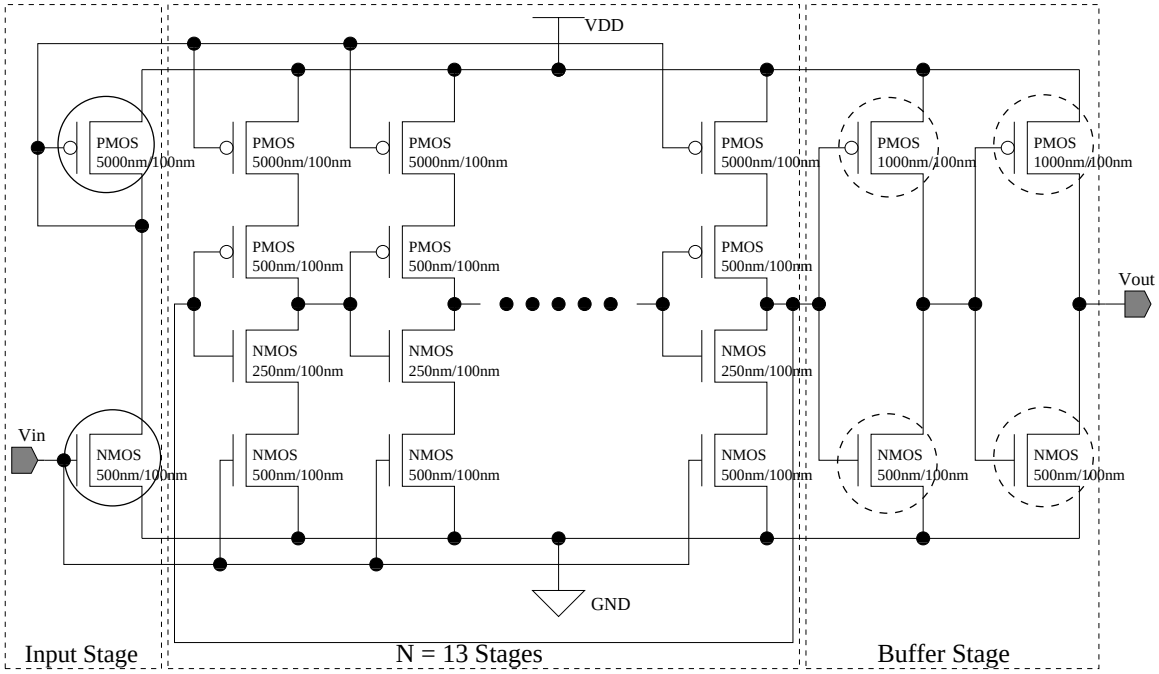


Fig. 6. Logical design of a current-starved VCO. The VCO has 13 stages. The transistor sizes are provided in Section VI. The solid circled transistors consume 48% of the total average power while the dashed circled transistors consume 11.5% of the total average power as discussed in Section VII.

$10 \times W_{ncs} = 5$ μm are obtained, where W_{ncs} and W_{pcs} are the widths and L_{ncs} and L_{pcs} are the lengths of the current-starved NMOS and PMOS transistors, respectively. The initial physical design of the VCO is then performed using these transistor sizes (shown in Fig. 6). The layout of the baseline VCO is shown in Fig. 7. The layout design is performed using a 90 nm 1 poly, 9 metal generic process design kit [25]. The measured performance of the baseline VCO is shown in Table IV.

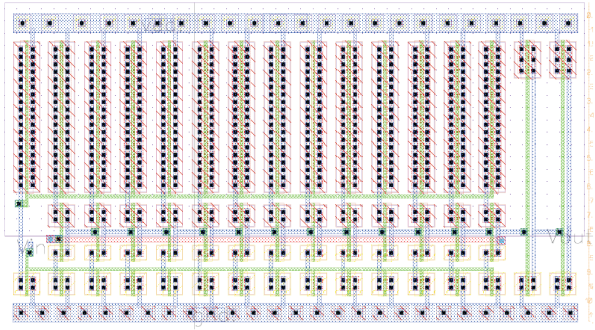


Fig. 7. Physical design of the 90nm CMOS based baseline VCO. The area of the VCO is 228.43 μm^2.

B. Characterization of the 90 nm CMOS Baseline VCO

It can be seen from Eqn. (5) that the oscillation frequency (f_0) shows strong dependence on supply voltage (V_{DD}), threshold voltage (V_t), and gate oxide thickness (T_{ox}). Hence, any variation in these process (V_t, T_{ox}) parameters and supply voltage (V_{DD}) leads to a possible degradation in f_0. Process variations can be modeled by using technology files or analytical formulas. Technology files are process-dependent and can be created from the information provided by foundries. In this research, a technology file based on a 90 nm process design kit is used [25]. The following parameters are identified for statistical process-variation analysis:

- Supply voltage (V_{DD}).
- Threshold voltage of (N,P)MOS transistors ($V_{t(n,p)}$).
- Gate oxide thickness of (N,P)MOS transistors ($T_{ox(n,p)}$).

The DOE-MC methodology of Section V has been used for fast analysis of the effect of process variations on f_0. A *two level full factorial design* is run for the 5 process parameters, where level 1: μ - 2 $\times$ σ, (μ= mean, σ = 10% of μ) and level 2: μ + 2 $\times$ σ. A full factorial run requires 2^5 = 32 trials. Five Monte Carlo replicate runs are run for every trial, and the μ and σ of f_0 are recorded for every trial. Hence we obtain 32 values of μ and σ for f_0, one for every trial. The final μ and σ for f_0 are recorded as the average of the 32 trials. Considering 5 replicates per trial, we get a total of 32 $\times$ 5 = 160 runs. This is substantially less as compared to 1000 runs needed for a typical Monte Carlo. The results for Monte Carlo replicates per trial = 10 and 20 and the percentage error in μ and σ are also presented in Table V.

Table VI presents the effect of statistical process parameter variation on f_0. In particular, four different cases are presented: 1) V_{tn}-only variation, 2) V_{tp}-only variation, 3) simultaneous T_{oxn} and T_{oxp} correlated variation, and 4) simultaneous variation of all 5 parameters. c_v is a dimensionless number that is used to compare different statistical distributions. The corresponding probability density functions (PDFs) are presented in Fig. 8.

VII. Process Variation Aware Optimization of VCO

In this section, it is demonstrated how the performance (f_0) discrepancy caused by the worst-case process variations is

TABLE II

FULL FACTORIAL EXPERIMENTS FOR THE 5 PARAMETERS OF THE VCO. THE 32 TRIALS ARE GROUPED INTO 16 RUNS FOR THE VALUES OF T_{oxp}.

Run	V_{DD}	V_{tn}	V_{tp}	T_{oxn}	T_{oxp}
Run 1	+	−	−	−	−
	+	−	−	−	+
Run 2	+	−	+	−	−
	+	−	+	−	+
Run 3	+	+	−	−	−
	+	+	−	−	+
Run 4	−	−	−	−	−
	−	−	−	−	+
Run 5	+	+	+	−	−
	+	+	+	−	+
Run 6	−	−	+	−	−
	−	−	+	−	+
Run 7	−	+	−	−	−
	−	+	−	−	+
Run 8	−	+	+	−	−
	−	+	+	−	+
Run 9	+	−	−	+	−
	+	−	−	+	+
Run 10	+	−	+	+	−
	+	−	+	+	+
Run 11	−	−	−	+	−
	−	−	−	+	+
Run 12	−	−	+	+	−
	−	−	+	+	+
Run 13	+	+	−	+	−
	+	+	−	+	+
Run 14	+	+	−	+	−
	+	+	−	+	+
Run 15	−	+	−	+	−
	−	+	−	+	+
Run 16	−	+	+	+	−
	−	+	+	+	+

TABLE III

PERFORMANCE DISCREPANCY AND WORST-CASE PROCESS VARIATION FOR A TARGET OSCILLATING FREQUENCY $f_0 \geq 2$ GHz.

Items	With parasitics	With process variations
f_0	1.56 GHz	1.13 GHz
Discrepancy	22%	43.5%
V_{DD}	1.2 V (nominal)	1.08 V (-10%)
V_{tn}	0.169 V (nominal)	0.186 V ($+10\%$)
V_{tp}	-0.136 V (nominal)	-0.150 V ($+10\%$)
T_{oxn}	2.33 nm (nominal)	2.56 nm ($+10\%$)
T_{oxp}	2.48 nm (nominal)	2.73 nm ($+10\%$)

overcome concurrently with power minimization of the VCO using a dual-oxide technique. The following specifications are obtained: 1) Target center frequency f_0 = 2 GHz. 2) Initial physical design center frequency $f_{0\mathrm{p}}$ = 1.56 GHz. 3) Initial physical design center frequency in worst case process variation $f_{0\mathrm{p-p}}$ = 1.13 GHz. 4) Initial average power consumption P_{VCO} = 212 μW.

A. Parameterized Parasitic Netlist Creation

Followed by the dual-oxide assignment, the parasitic-aware netlist generated from the first layout is then parameterized for design parameters. The parameter set includes the widths of PMOS and NMOS devices in the inverter (W_n, W_p), the PMOS and NMOS devices in the current-starved circuitry (W_{ncs}, W_{pcs}), and T_{oxpth}, T_{oxnth}.

TABLE IV

MEASURED PERFORMANCE OF THE BASELINE VCO.

Parameter	Value
Technology	90 nm CMOS 1P 9M
Supply Voltage (V_{DD})	1.2 V
Oscillation frequency	2 GHz
Power	212 μW
Area	228.43 μm^2

TABLE V

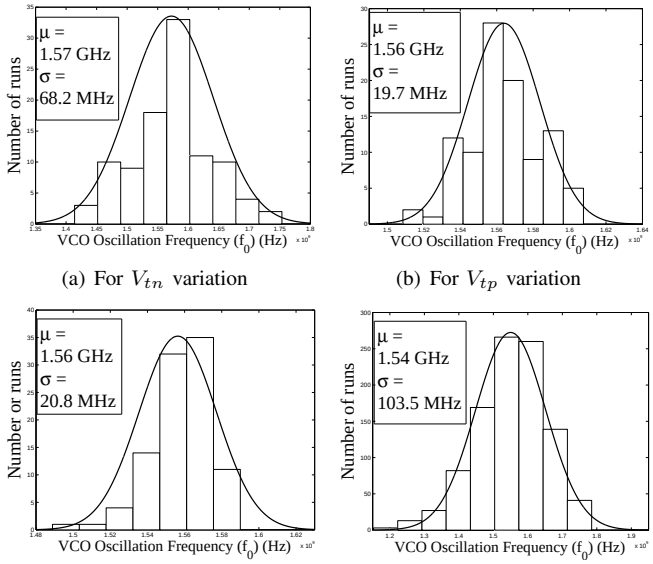
STATISTICAL INFORMATION FROM DOE-MC APPROACH.

MC runs per trial	Total runs	% error (μ)	% error (σ)	Time saving over TMC
5	160	7.47	25.1	6.25×
10	320	6.78	14.7	2×
20	640	5.78	10.3	1.5625×

TABLE VI

EFFECT OF STATISTICAL PROCESS VARIATION ON THE OSCILLATION FREQUENCY (f_0) OF THE 90 NM CMOS BASELINE VCO.

Parameters Varied	$\mu(f_0)$ (GHz)	$\sigma(f_0)$ (MHz)	c_v $\left(\frac{\sigma}{\mu}\right)$
V_{tn}-only variation	1.57	468.2	4.3%
V_{tp}-only variation	1.56	19.7	1.3%
Simultaneous T_{oxn}/T_{oxp}) variation with correlation coefficient of 0.9.	1.56	20.8	1.3%
Simultaneous V_{DD}, V_{tn}, V_{tp}, T_{oxn}, and T_{oxp} correlated variations.	1.54	103.5	6.7%



(a) For V_{tn} variation

(b) For V_{tp} variation

(c) For correlated T_{oxn} and T_{oxp} variation

(d) Simultaneous correlated V_{DD}, V_{tn}, V_{tp}, T_{oxn}, and T_{oxp} variation

Fig. 8. Statistical process variation analysis of the baseline VCO for the individual variation of V_{tn} and V_{tp}, correlated T_{ox} variation, simultaneous correlated V_{DD}, V_{tn}, V_{tp}, T_{oxn}, and T_{oxp} variation. The distribution of f_0 is observed to be Gaussian in all cases.

B. Power-Prioritized Dual-Oxide Assignment

A transient analysis is performed on the physical design of the VCO, and the average power consumed by each of the transistors is measured. The input stage transistors (shown by solid circles in Fig. 6) collectively consume 48% of the total average power of the VCO circuit, hence are most suitable candidates for higher thickness oxide assignment (T_{oxpth}, T_{oxnth}). The buffer stage transistors (shown by dashed circles in Fig. 6) consume 11.5% of the total average power, and hence may be treated to higher thickness oxide, for further power minimization. In this paper, the input stage transistors are subjected to dual-oxide assignment.

C. Process Variation Aware Optimization Algorithm

In this section a particle swarm optimization (PSO) based algorithm is proposed for process variation aware optimization. The PSO algorithm uses multiple particles to obtain a solution based on the cost function [26]. The particle movement is calculated based on the local intelligence of each particle which is offset using global knowledge. The steps of the proposed approach are shown in Algorithm 1. Each particle location information holds a multidimensional location, where each dimension corresponds to a parameter. The algorithm starts at a random location of each parameter for each particle, with random velocity.

Algorithm 1 Particle Swarm Optimization (PSO) for VCO.

```
Initialize N ← number of particles.
Start at a random location with uniform distribution.
Obtain current position x_i and use it initially for best particle position f(p_i) and f(g) = min(p_i).
v_i ~ U(min_p_i, max_p_i).
Initialize iteration ← 0.
Initialize weight for swarm effect ϱ_p.
Initialize weight for swarm effect ϱ_g.
Initialize weight for velocity effect w.
while iteration < max_iterations do
  for each i do
    v_i = ωv_i + ϱ_p τ_p(p_i − x_i) + ϱ_g τ_g(g − x_i).
    x_i ← x_i + v_i.
    if f(x_i) < f(p_i) then
      update position: p_i ← x_i.
      if f(p_i) < f(g) then
        g ← p_i.
      end if
    end if
  end for
end while
```

The candidates for optimization are the widths of the inverters (W_n, W_p) and current-starved transistors (W_{ncs}, W_{pcs}), and the oxide thicknesses (T_{oxnth}, T_{oxpth}) of thick-oxide (input stage) transistors. While the thicker oxide minimizes power consumption, the higher widths of the devices maximize performance. Our specifications include $f_0 \geq$ 2GHz, and P_{VCO} = min. Table VII shows the final characteristics for the process variation optimal VCO.

TABLE VII
FINAL VALUES OF THE PARAMETERS FROM THE OPTIMIZATION.

D	C_{low}	C_{up}	D_{opt}
W_n	200 nm	500 nm	210 nm
W_p	400 nm	1 μm	415 nm
W_{ncs}	1 μm	5 μm	8.5 μm
W_{pcs}	5 μm	10 μm	5 μm
T_{oxpth}	2.48 nm	5 nm	5 nm
T_{oxnth}	2.33 nm	5 nm	3.54 nm

The physical design of the VCO is then modified using these parameter values, and the following results are obtained:

- Target center frequency f_0 = 2 GHz.
- Final physical design center frequency $f_{0\mathrm{p}}$ = 2.3 GHz.
- Final physical design center frequency in a worst case process variation environment $f_{0\mathrm{p-p}}$ = 1.98 GHz.
- Final average power consumption P_{VCO} = 158 μW.

Hence, a final optimized dual-oxide layout is obtained, with 1.98 GHz center frequency under worst-case process variation, and 2.3 GHz center frequency in nominal process conditions with 25% power minimization. For the 90 nm CMOS technology which has been used for the design in this paper, the leakage power can be a significant portion in the total power dissipation. The leakage power for 90 nm CMOS technology is mainly due to subthreshold leakage. In the optimal design with the device sizes obtained from the optimization the leakage power is 23.6 μW as compared to 38.2 μW in the baseline design; thus a reduction of 38% is achieved. However, for sub-65 nm CMOS technology, the leakage power becomes a much larger component of the total power dissipation and the leakage power can have both subthreshold leakage and gate-oxide leakage as significant components [22], [27]. The oscillating frequency versus voltage characteristics show acceptable linearity.

D. Physical Design of the Optimal 90nm VCO

The dual-oxide physical design of the VCO has been performed using a generic 90 nm Salicide 1.2 V / 2.5 V 1 poly 9 metal generic process design kit [25]. At high frequencies, parasitic inductance has a major impact on chip performance. Hence it is necessary to extract self (L) as well as mutual (K) inductance so that the impact of inductive coupling could be assessed and minimized on the layout. The final widths of the process variation optimal circuit and thick oxide transistors are shown in Fig. 9.

E. Characterization of the Optimal VCO

In this section, the results of statistical process variation applied on the process variation optimal VCO are presented. Statistical variations in the process parameters, each assumed to be Gaussian are taken into account by using Monte Carlo simulations, and the effect on oscillation frequency is observed. The 7 parameters considered for process variation in the process variation optimal VCO are: V_{DD}, V_{tn}, V_{tp}, T_{oxn}, T_{oxp}, T_{oxnth} and T_{oxpth}. The different cases experimented with are the following: 1) V_{tn}-only variation, 2) V_{tp}-only variation, 3) simultaneous T_{oxn}, T_{oxp}, T_{oxnth}, T_{oxpth} variation,

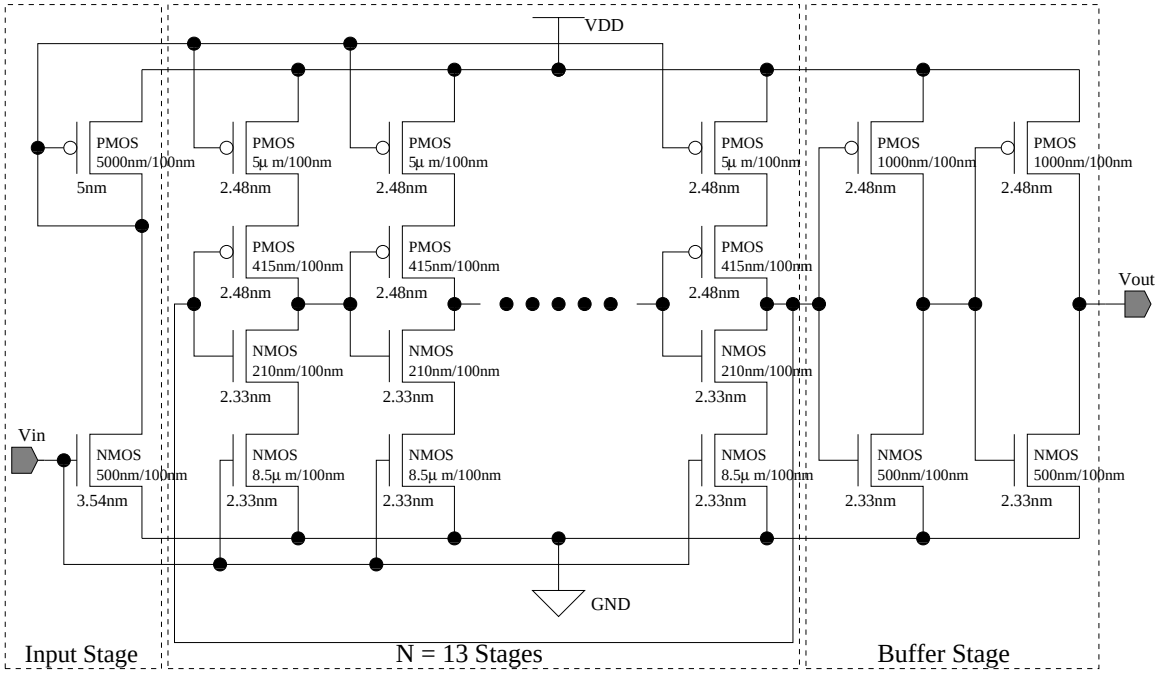
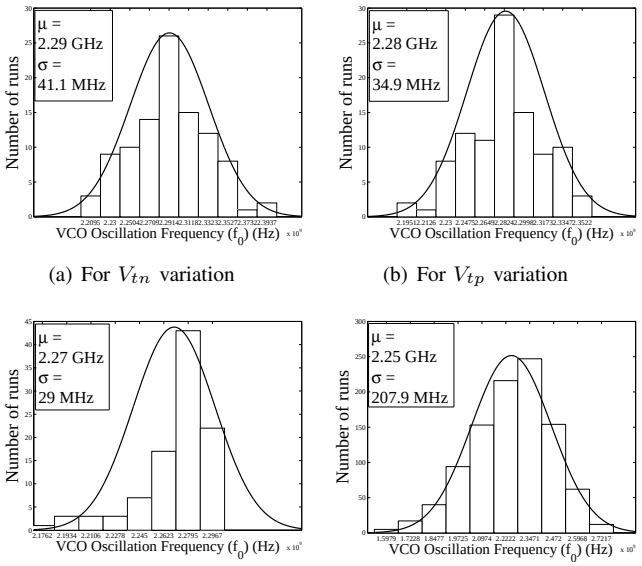


Fig. 9. Final widths and gate-oxide thicknesses of transistors of the process variation optimal VCO.

and 4) simultaneous V_{DD}, V_{tn}, V_{tp}, T_{oxn}, T_{oxp}, T_{oxnth} and T_{oxpth} variation. The corresponding statistical distributions are presented in FIg. 10.

The value of the mean (μ), the standard deviation (σ) and the coefficient of variation $c_v = \sigma/\mu$ of the oscillation frequency for all 4 cases have been recorded in Table VIII. For the process variation optimal VCO, c_v is 1.38 $\times$ higher than the c_v for the baseline design, but is 1.66 $\times$ lower than the c_v of the parasitic-aware design for variation in all parameters. In other words, the process sensitivity of the process variation optimal design is 1.38 $\times$ higher than the baseline VCO, but 1.66 $\times$ lower than the parasitic-optimal VCO.

The frequency-voltage characteristics of the process variation optimal VCO, compared with the baseline design are shown in Fig. 11. It is evident that the objective ($f_0 \geq 2$ GHz) is met with the design optimized for power, process and parasitics. The frequency-voltage characteristics lose their linearity. However, this is not an issue as the loss happens beyond the target frequency range. The performance summary of the process variation optimal VCO is given in Table IX.



(a) For V_{tn} variation

(b) For V_{tp} variation

(c) For correlated (T_{oxn} and T_{oxp}) variation

(d) Simultaneous (V_{DD}, V_{tn}, V_{tp}, T_{oxn}, T_{oxp}, T_{oxnth}, T_{oxpth}) variation

Fig. 10. Statistical process variation analysis of the optimal VCO.

VIII. Conclusions and Future Research

In this paper, a novel design methodology for manufacturing process variation aware nano-CMOS VCOs is presented. The degradation of the center frequency due to process variation effects has been narrowed down from 43.5% to 1%, along with 25% power minimization using a dual-oxide technique, with 41% area penalty. The end product of the proposed design flow is a process variation optimal dual-oxide VCO physical design. Table X presents a comparison of the baseline and process variation optimal VCO with respect to the figures of merit considered in the paper. The process variation aware design methodology is a major step towards handling nano-CMOS mixed-signal circuits in a predictable fashion [28]. The proposed research pushes the state-of-the-art to address ITRS grand challenges (1), (3), and (11) from 2015 goals and grand challenge (31) beyond 2016 goals [29].

The methodology has been investigated for different types of CMOS technologies and many types of circuits. It has been observed that the proposed methodology is scalable to different technologies, transistor counts, and device parameters. For example, for a 45 nm CMOS VCO, the power reduction is roughly the same, in the order of 20–25%. The methodology

TABLE VIII

EFFECT OF STATISTICAL PROCESS VARIATION ON THE OSCILLATION FREQUENCY (f_0) OF PROCESS VARIATION OPTIMAL VCO.

Parameters varied	μ (f_0)	σ (f_0)	c_v (Variation -Optimal)	c_v (Parasitic -Optimal)	c_v (Baseline)
V_{tn}-only variation	2.29 GHz	41.1 MHz	1.79%	2.76%	4.34%
V_{tp}-only variation	2.28 GHz	34.9 MHz	1.53%	1.46%	1.26%
Variation of $(T_{oxn}, T_{oxp}, T_{oxnth}, T_{oxpth})$ (correlation coefficient = 0.9)	2.27 GHz	29 MHz	1.28%	13.21%	1.33%
Simultaneous correlated variation of $(V_{DD}, V_{tn}, V_{tp}, T_{oxn}, T_{oxp}, T_{oxnth}, T_{oxpth})$	2.25 GHz	207.9 MHz	9.24%	15.30%	6.72%

TABLE X

COMPARISON OF METRICS FOR ALL VCO VERSIONS PRESENTED IN THE PAPER

VCO	P_{VCO}	% Change	f_0	% Change	A_{VCO}	% Change	c_v (5 parameters)	% Change
Baseline	212 μW	–	2 GHz	–	228.4 μm^2	–	6.72%	–
Optimal	158 μW	-25.0%	2.3 GHz	+13.0%	389.0 μm^2	+41.0%	9.24%	+1.38 $\times$

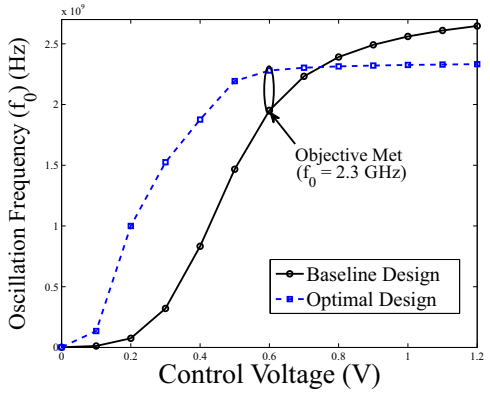


Fig. 11. Frequency-voltage characteristics of the optimal VCO.

TABLE IX

PERFORMANCE OF THE PROCESS VARIATION OPTIMAL VCO.

Characteristics	Values
Technology	90 nm CMOS 1P 9M
Supply Voltage (V_{DD})	1.2 V
Center Frequency (Nominal process)	2.3 GHz
Process Variation and Supply Variation	V_t (+10%), T_{ox} (+10%), V_{DD} (−10%)
Center Frequency (Worst-case Process Variation)	1.98 GHz
Design Parameters	6 $(W_n, W_p, W_{ncs}, W_{pcs}, T_{oxpth}, T_{oxnth})$
Number of Objectives	2 ($f_0 \geq 2GHz$, P_{VCO} = minimum)
Power	158 μW
Area	389.04 μm^2

is currently investigated for double-gate FinFET technology and the preliminary results are promising [30], [31]. It is observed that the results are similar with an interesting note that the variability (i.e. standard deviation of a FoM) is reduced by approximately 14% in the double-gate FinFET circuit, as compared to single-gate CMOS [30], [31].

For future research, the thermal effects in the VCO design will be considered. Phase noise will also be considered concurrently with frequency for optimization. Alternative optimization algorithms such as simulated annealing and genetic algorithms are also being explored and execution-time comparison with these algorithms for the process-variation aware design flow will be performed. The effectiveness of the methodology will also be tested on alternative VCO topologies such as LC-VCO. Also, techniques for area optimization of the process-variation optimal VCO may be explored.

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