Nano-CMOS Thermal Sensor Design Optimization for Efficient Temperature Measurement

Oghenekarho Okobiah[a,1], Saraju P. Mohanty[a,1,*], Elias Kougianos[a,1]

[a] *NanoSystem Design Laboratory (NSDL), University of North Texas, Denton, TX 76207, USA.*
[b] *Department of Computer Science and Engineering, University of North Texas, USA.*
[c] *Department of Engineering Technology, University of North Texas, USA.*

Abstract

We present a novel and efficient thermal sensor design methodology. The growing demand for power management on VLSI systems drives the need for accurate thermal sensors. Conventional design techniques for on-chip thermal sensors in nanometer technologies consume expensive design iterations and result in increased power consumption and area overhead. Power-efficient, high-sensitivity thermal sensors are important for reducing the thermal stress on the systems or circuits which are being monitored. The proposed design flow methodology, which incorporates a stochastic gradient descent (SGD) algorithm, optimizes the power consumption (including leakage) of IC subsystems. An illustration of the proposed design methodology is presented using a ring oscillator (RO) based on-chip thermal sensor which was designed using 45 nm CMOS technology. The RO based thermal sensor has a resolution of 0.097°C/bit. Experimental tests and analysis of the design methodology on a full layout-accurate parasitic netlist of the RO demonstrate the applicability of our methodology towards optimization of the power consumption with temperature resolution as a design constraint. A reduction of power consumption by 52% with a final area of 1389.1μm^2 is obtained.

Keywords: Thermal Sensor, Temperature Measurement, Design Flow, Design Optimization, Stochastic Gradient Descent.

1. Introduction

The increasing complexity and power consumption of Systems-on-Chip (SoCs) continues to grow as technology shrinks due t oscaling. The density of modern integrated chips (ICs) and SoCs results in very high on-chip power densities. The increase in power consumption and power density is a critical issue, directly affecting the thermal stability of SoCs. To mitigate these issues, various thermal management schemes have been explored for efficient control of power density of ICs. Thermal sensors are typically used for controlling the power consumption and to increase the reliability of SoCs. Thermal sensors are needed for effective thermal management which helps to reduce power consumption and increase performance. Approximately 50% of reliability issues are attributed to thermal related causes [1]. To monitor and effectively control the thermal properties of integrated devices, the accuracy of thermal measurements must be ensured. Hence, the importance of on-chip thermal sensors. They are one of the most common methods of measuring the thermal characteristics of ICs [2] and depending on the application, an IC may contain multiple such sensors. The placement of on-chip thermal sensors on an example motherboard is

*Corresponding author
Email addresses: oo0032@unt.edu (Oghenekarho Okobiah), saraju.mohanty@unt.edu (Saraju P. Mohanty), elias.kougianos@unt.edu (Elias Kougianos)
[1] http://nsdl.cse.unt.edu

shown in Fig. 1.

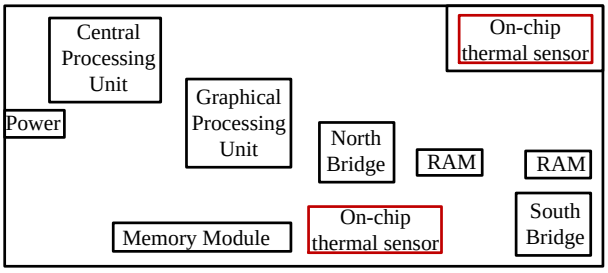

Figure 1: Thermal sensor locations on a motherboard.

The design of thermal sensors for different applications has been widely researched and reported [3, 4, 5, 6, 7, 8]. Such designs using CMOS technology have been reviewed in [8, 7] and extended its applications to on-chip sensors in [4, 5]. Thermal sensors based on CMOS technology utilize the temperature dependent characteristics of MOS transistors for sensing the temperature of the circuit [5]. Oscillator based designs are one of the most common techniques of CMOS based thermal sensors, where the oscillating frequency depends on temperature and is converted to temperature readings. The use of thermal sensors on chips, however, contributes to some problems. Poorly designed sensors can decrease the performance by adding an area overhead and increasing the overall power consumption. In [6], the power consumption of the on-chip thermal sensor significantly increases the overall power consumption. In effect, integrated thermal sensors for SoCs must also be low-power and cost-effective area wise. In addition, the sensors must accurately measure the temperature of the chip which puts more constraints on the low-power specification. Hence, the design of thermal sensors themselves has also become an integral part of reliability designs. Recent research works [4, 5] have proposed solutions for efficient on-chip thermal sensors which are low-power and do not significantly impact the circuit intended for sensing. In designing for low power consumption, other factors such as thermal sensitivity are often traded for optimization. Thermal sensors for on-chip use must be robustly designed to efficiently control the problems of power density without increasing the overall power consumption or incurring more cost from area overhead or degradation of the thermal sensitivity. In the optimization of design for performance objectives, various search algorithms are used for efficient design space exploration. Common search algorithms that have been implemented for the optimization of nanoCMOS circuits include genetic algorithms, swarm intelligence algorithms, geometric programming, simulated annealing, tabu search and gradient search algorithms [9, 10, 11, 12].

In order to mitigate the problems of on-chip temperature measurement, this paper proposes a design optimization flow methodology for the design of efficient on-chip thermal sensors. The proposed methodology incorporates a stochastic gradient descent based (SGD) algorithm. The use of optimization algorithms to increase the speed of explorative search designs has also been widely reported. The use of an SGD algorithm improves the design process by reducing the design space exploration time for optimization. The modified SGD algorithm also eliminates the problem of local optima. The design flow is presented using a 45 nm thermal sensor as case study circuit. In illustrating the effectiveness of the design flow, the power consumption of the thermal sensor is reduced using the accuracy of the temperature measurements as a constraint.

The rest of this paper is organized as follows. The novel contributions of this paper are presented in Section 2. A brief review of selected related research is presented in Section 3. In Section 4, a description of the baseline design of a thermal sensor circuit using 45 nm CMOS technology is presented. The proposed design optimization flow methodology is presented in section 5. The experimental setup, results and analysis are presented in section 6. In Section 7, conclusions and future research directions are discussed.

2. Novel Contributions of this Paper

This paper presents a novel design flow methodology incorporating the use of a Stochastic Gradient Design (SGD) based algorithm for the efficient design optimization of analog circuits. An on-chip thermal sensor using a 45 nm technology is used as an illustrative case study. The schematic and physical designs of the sensor are presented. The sensor is based on a ring oscillator (RO) architecture that uses a binary counter and registers for accurate temperature measurement. The SGD based algorithm also presented here is applied on nano-CMOS circuit designs for the first time. The standard SGD algorithm has been modified to restart at random points in order to mitigate the issue of local optima of the traditional SGD algorithm. A further analysis of the impact of process variation on the power consumption performance of the thermal sensor is also discussed.

A **summary of the contributions** of the current paper are as follows:

1. A robust design flow is proposed to design and characterize nano-CMOS based thermal sensors.

2. A design optimization methodology is presented for fast design exploration of thermal sensors.
3. A modified Stochastic Gradient Descent (SGD) algorithm is presented for thermal sensor optimization.
4. A 45 nm RO based thermal based sensor is designed at the layout level and optimized.
5. A statistical analysis of the impact of process variation of power consumption was performed on the thermal sensor.

3. Related Research on Temperature Sensors

The design of on chip thermal sensors, including design for accurate temperature estimation and robust performance has been well researched [4, 5, 13, 7, 3, 14]. In [5], a class of thermal sensors based on Differential Ring Oscillators (DRO) is introduced. An implementation using a current starved inverter topology utilizes the sensitivity of the oscillating frequency to temperature for thermal sensing. In [6], a low power thermal sensor has been proposed. It employs an oscillator based on an RS register structure. The output frequency of the oscillator is Proportional to Absolute Temperature (PTAT) and is thus used with a constant pulse generator and a bias calibrator. In [13], another approach is taken to compensate for the effect of noise, process variations and V_{DD} fluctuations on the thermal sensor. A statistical methodology is proposed for estimating the actual temperature reading of the sensor. The temperature is modeled as a variable associated with a probability density function (PDF) that is dependent on the noise, process variations and V_{DD} fluctuations. In [15, 16], a PTAT current source is proposed. The circuit uses the ratio between the drain currents of two current source transistors operating in the subthreshold region which is PTAT for thermal sensing. The source transistors are fed by a reference current which is independent of ambient temperature and the output of the PTAT generator is converted to a corresponding temperature reading with an A/D circuit [16]. In an effort to reduce the effect of process variation and noise on thermal sensors, similar circuits have been proposed in [17]. In [3], a technique implementing inductors and variable capacitors is proposed for thermal sensing of high temperature environments. The temperature reading is telemetrically placed outside of the circuit to isolate it from the high temperatures on the circuit.

A recent design has been proposed in [14] that implements a miniaturized CMOS based thermal probe that significantly reduces the size of comparable sensors allowing it to be easily placed near hot spots for localized real-time temperature mapping. The thermal sensor design presented in this paper is also oscillator based and is motivated by the design presented in [4]. The sensor used is implemented using the conventional ring oscillator topology in contrast to the current starved topology. The thermal sensor is also not operated in the subthreshold region which leads to a decrease in frequency with increasing temperature. The frequency divider and multiplexer are eliminated in our design.

4. Thermal Sensor Design for On-Chip Temperature Measurement

The 45 nm thermal sensor used as an illustrative application of the proposed design flow methodology is presented in this section. Fig. 2 shows the 45 nm thermal sensor which uses a ring oscillator as the major component for thermal sensing. The operational frequency of the ring oscillator is very sensitive and proportionally dependent on ambient temperature and thus the output frequency fluctuates in response to the effect of surrounding temperature. The RO is the primary component of the sensor. The circuit also uses a combination of 10-bit binary counters and 10-bit registers for accurately expressing the temperature readings as a digital output. The temperature measurement is calibrated by sampling the edges of the oscillator output during a sampling period with the binary counter. The count during the period of the RO is proportional to the absolute temperature which is stored in the 10 bit register.

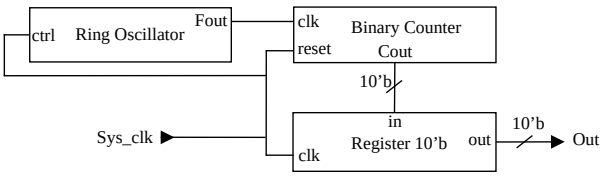

Figure 2: Block diagram of the thermal sensor.

The ring oscillator is shown in Fig. 3. It consists of a cascade of an odd number of inverters that are connected in a loop leading to an unstable state which creates the oscillations. The ring oscillator shown in Fig. 3 has a total of 15 inverters, but the first inverter has been modified as a NAND gate and used to gate the ring oscillator operation. The transistor level schematic is shown in Fig. 4.

The oscillation frequency of the ring oscillator is given by the following expression:

$$f_{osc} = \frac{1}{n(t_{pLH} + t_{pHL})}, \quad (1)$$

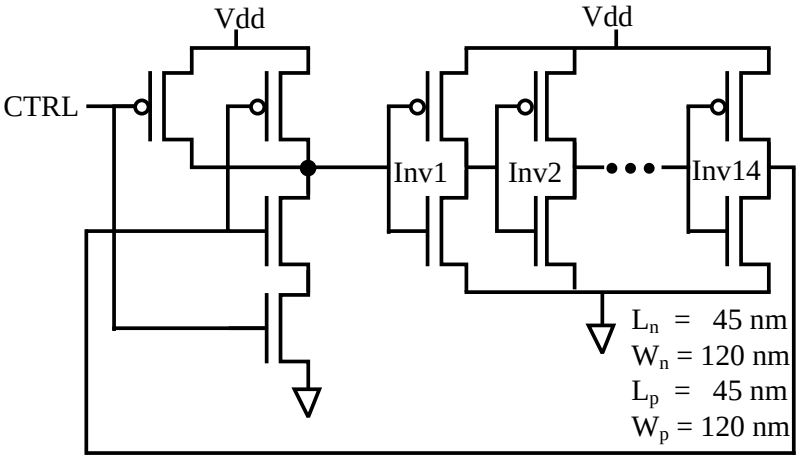

Figure 4: Transistor level schematic of the RO.

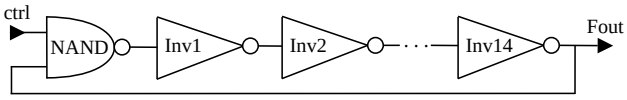

Figure 3: Block diagram of the RO.

where n is the number of stages used in the oscillator and t_{pLH} and t_{pHL} are the low-to-high and high-to-low propagation delays, respectively. The propagation delays can be expressed as [17]:

$$t_{pLH} = \frac{-2C_L V_{tp}}{\kappa_p (V_{dd} - V_{tp})^2} \quad (2)$$

$$+\frac{C_L}{\kappa_p (V_{dd} - V_{tp})} \times \quad (3)$$

$$\ln\left(\frac{1.5V_{dd} + 2V_{tp}}{0.5V_{dd}}\right), \quad (4)$$

$$t_{pLH} = \frac{2C_L V_{tn}}{\kappa_n (V_{dd} - V_{tn})^2} \quad (5)$$

$$+\frac{C_L}{\kappa_p (V_{dd} - V_{tn})} \times \quad (6)$$

$$\ln\left(\frac{1.5V_{dd} + 2V_{tn}}{0.5V_{dd}}\right), \quad (7)$$

where C_L is the capacitive load, V_{dd} is the on-chip power supply and V_{tp} and V_{tn} are the PMOS and NMOS threshold voltages, respectively. The transconductances κ_n and κ_p are calculated by the following expression:

$$\kappa_{n/p} = \mu_{n/p} C_{ox} \left(\frac{W}{L}\right)_{n/p}. \quad (8)$$

In equations (1) - (5), the threshold voltages and mobilities $\mu_{n/p}$ are the factors most sensitive to temperature fluctuations. They are given by [18]:

$$V_t(T) = V_t(T_0) + \alpha_{V_t}(T - T_0), \quad (9)$$
$$\alpha_{V_t} = -0.5 - 3.0mV/^\circ K.$$

$$\mu(T) = \mu_0 \left(\frac{T}{T_0}\right)^{\alpha_\mu} \quad (10)$$
$$\alpha_\mu = -1.2 - 2.0.$$

An increase in temperature leads to an increase in the propagation delay which translates to a decrease in oscillating frequency.

The 10-bit binary counter is shown in Fig. 5 and consists of JK flip-flops, while the 10-bit register is used to store the value from the counter and is also implemented with JK flip-flops.

The thermal sensor shown in Fig. 2 was implemented using a 45 nm CMOS technology library provided by Cadence Design Systems, Inc. The design is able to sense temperatures between 0°C and 100°C. The *Sys_clk* signal set to a 500 KHz frequency is used to enable the thermal sensor. When the *Sys_clk* turns to logic zero, the ring oscillator is disabled, the counter is also reset and the register also stops saving the count, storing the last count value it had before the *Sys_clk* was set to logic "0". The binary counter is used to count the frequency difference between the ring oscillator output and the system clock. The count is stored in the 10-bit register and calibrated to measure the temperature change. The physical design of the thermal sensor is shown in Fig. 6. Temperature readings can be taken using two different methods as follows:

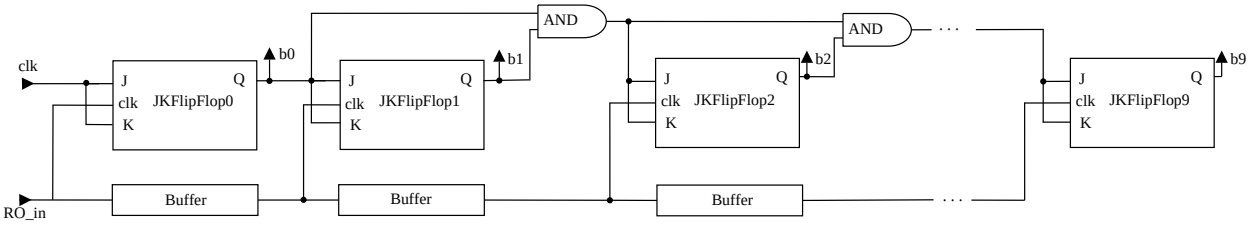

Figure 5: Block diagram of the 10 bit binary counter.

1. Using the count characteristic plot which is shown in Fig. 7. This count is interpreted with a calibration table.
2. Using the formula below which was generated from linear data fitting with an R^2 value of 0.9978.

$$\text{Temperature} = -0.5167 \times \text{Count} + 395.3. \quad (11)$$

This equation can serve as a predictive function which will enable a direct temperature reading from the count value.

Fig. 8 shows a summary of the design steps. It can be broadly divided into three main stages. Stage A involves the actual design of the sensor including the schematic and physical designs. Functional simulation of the thermal sensor is done to investigate and verify its sensing characteristics. The frequency output of the the sensor is observed while varying the temperature. The temperature range calibrated for the thermal sensor was 0°C$\sim$ 100°Cwith a sensitivity of 9.42MHz/°Cfor the physical design with silicon-accurate parasitics. The next stage involves the calibration of the thermal sensor. This is done by measuring the range of the thermal sensor and associating the corresponding frequency output of the RO. The 10 bit counter is then calibrated using the diagram in Fig. 7 or used as a prediction based on extrapolation data. The size of the counter determines the resolution of the sensor. With the 10 bit counter used for this design over a range of 100°C, a resolution of 0.097°C/bit is achieved. The final step of the design is the digital display of the sensed temperature. For this stage, a 10 bit register is used to store the output from the counter. This process could serve as a guideline for designers to reproduce the thermal design and to perform accurate characterization.

The performance and accuracy of the physical design is degraded when compared to the schematic design. This is expected due to parasitic effects from the layout. Table 1 shows a comparison between the schematic and physical designs. Power consumption is increased by 29% while the sensitivity decreases by 44%. This circuit exhibits a linear dependence of oscillation frequency on junction temperature as shown in Fig. 9.

Table 1: Characterization of the 45nm CMOS Baseline Thermal Sensor Circuits.

Sensor Designs	Power (P_{TS})	Sensitivity (T_{TS})	Area (μm^2)
Schematic	293.1 μW	16.88 MHz/°C	-
Layout	379.4 μW	9.42 MHz/°C	1221.37
% Change	+29%	-44%	

As the temperature is increased, the frequency decreases. The schematic frequencies range from 0°C= 5.924 GHz to 100°C= 4.236 GHz. Assuming a 6 GHz max clock rate for the ring oscillator, and a 10 bit counter (1024 max count) the effective resolution is calculated by dividing the temperature range by the number count 100°C/1024 bit which gives a 0.097°C/bit resolution. The range of frequency output is also severely degraded as also seen in Fig. 9. The range drops to 3.867 GHz to 2.986 GHz. The resolution can also be specified in terms of GHz/°C to reflect the degrading effect of parasitics from the physical design. There is a 44% change in frequency/temperature resolution between the schematic and physical designs. The area of the layout is 1221.37 μm^2. Table 2 shows the total count of transistors for each component of the thermal sensor. The oscillator component consists of 32 transistors.

Table 2: Transistor Count for Thermal Sensor Components

Component	Transistor Count
Ring Oscillator	34
10-bit Binary Counter	462
10-bit Register	400
Total	896

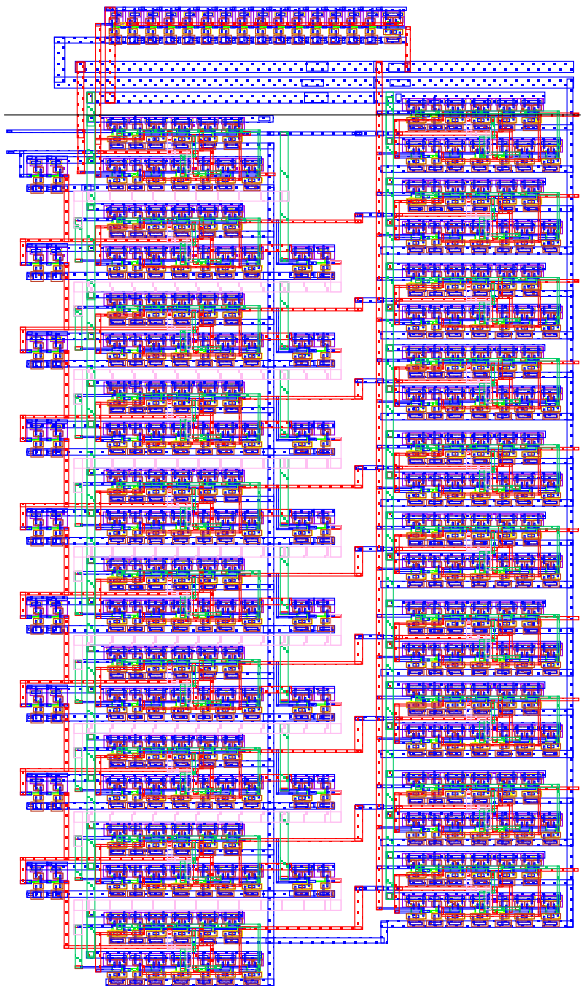

Figure 6: Physical design of the 45 nm thermal sensor.

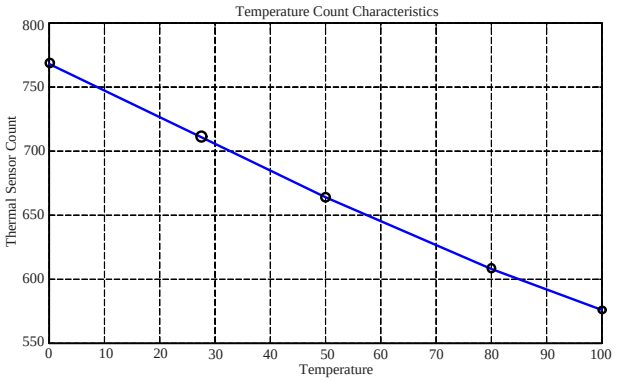

Figure 7: Count characteristics for the thermal sensor from layout.

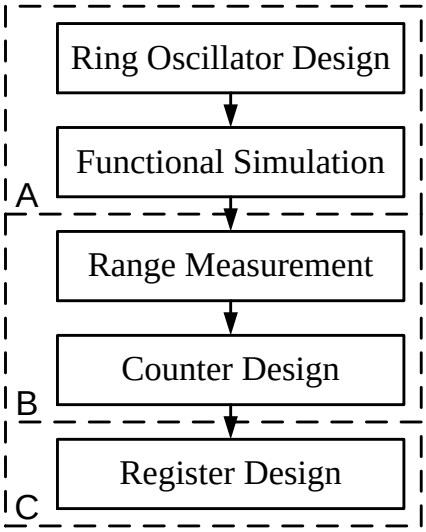

Figure 8: Design flow for the thermal sensor

5. Proposed Methodology for Design Optimization of the Thermal Sensor

One of the major aspects of optimization for thermal circuit designs is the level of power consumption. The average power consumption of the thermal sensor must not burden or impact the overall power consumption of the circuit which it monitors. However in designing for optimal power consumption, the area overhead and the accuracy or sensitivity of the sensor are often compromised. Hence, a design technique is desired which optimizes power consumption without increasing the area overhead or degrading the sensitivity or at least minimizing the impact to both. To this effect, a novel design flow methodology which uses a stochastic gradient descent based algorithm is shown in Fig. 10. The design methodology aims to optimize the power consumption of the sensor using the thermal sensitivity as a design constraint. The SGD influence on the methodology improves the optimization phase by actively exploring the design space for the optimal design objective, in this case the minimal power consumption, while minimizing the impact to the thermal sensitivity. The SGD is modified to have random restarts in order to eliminate the problem of local optima. The following subsection describes in detail the overall design methodology and the SGD based algorithm.

5.1. Design Optimization Flow

The first step in the design flow is to create the baseline schematic design of the circuit that meets the given design specifications. For the case study circuit implemented in this paper common design objectives include power consumption, temperature resolution, and temperature range. After the schematic design has been

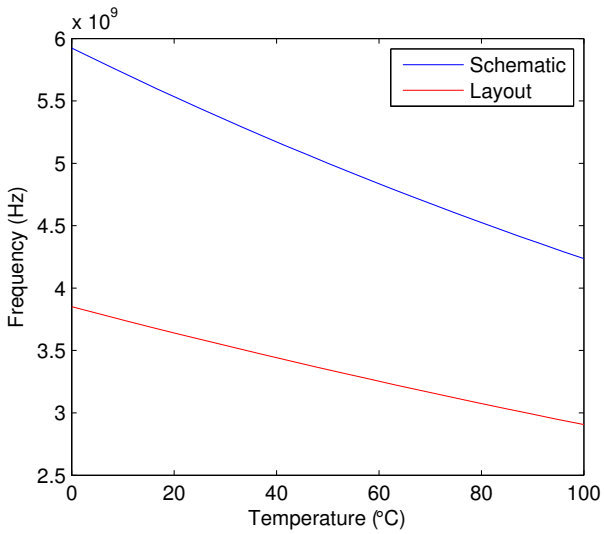

Figure 9: Ring oscillator frequency response versus temperature for both schematic and physical designer.

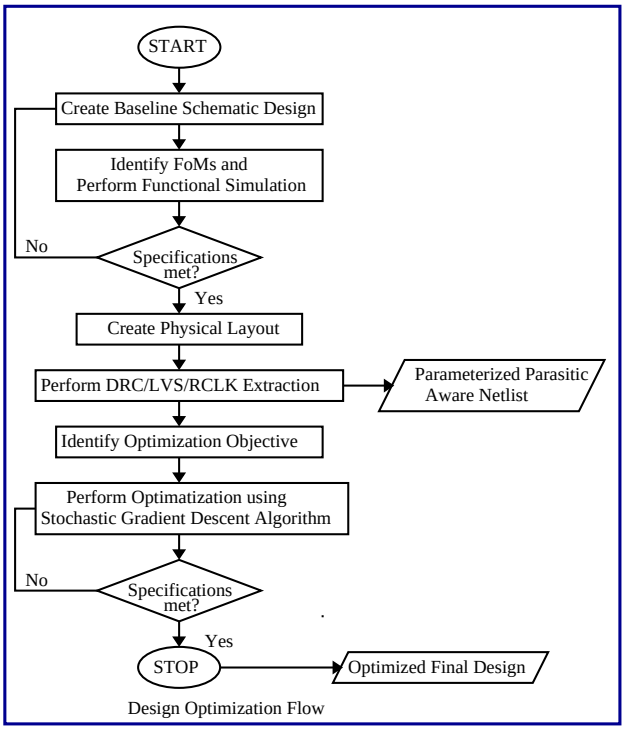

Figure 10: The proposed design optimization flow.

created, a set of performance objectives are identified (Figures-of-Merit, FoMs) and a functional simulation is performed to ensure that the circuit meets initial specifications. If the design specifications are not met, the schematic is reiteratively designed until the specifications are met. The next step is to create the physical layout design of the circuit. The physical layout is validated with Design Rule Checks (DRC), and Layout vs. Schematic (LVS) tests. From the physical layout, a fully parasitic netlist - resistance, capacitance and self and mutual inductance (RLCK) is extracted to ensure the simulation model is as silicon accurate as possible. The parasitic netlist is then parameterized with design and process parameters, including the length and width of the transistors (L, W), threshold voltages (V_t), oxide thickness (T_{ox}), etc. It is only after the optimization is complete that the physical design is redrawn using the parameters obtained from the optimization process. This ensures that the manual design of the physical layout is done at most twice, once before the parasitic extraction of the netlist and modified after the optimization process is complete.

With a fully parameterized parasitic aware netlist and a chosen performance objective, a stochastic gradient descent based algorithm is used to optimize the circuit to obtain the final optimized design. The stochastic gradient takes in as input the parameterized netlist, the design objective and the range of parameter values for the design. The output of the optimization algorithm are the design variable values that give the optimal performance objective. The optimization process is reiterated until the target specifications are met, as seen in Fig. 10. Upon completion of the optimization process, the final parameter values are used to manually redesign the physical layout. In using the parasitic extracted netlist, the process ensures that the design flow is parasitic aware, and the final physical design is implemented to reflect more silicon accurate results. A detailed discussion of the SGD based algorithm is presented in Section 5.2.

5.2. Stochastic Gradient Descent Algorithm for Thermal Sensor Optimization

The stochastic gradient descent (SGD) algorithm is a variation of descent based algorithms that utilize the gradient of functions to search for optimal values. The stochastic gradient descent is a cost function optimization algorithm that has been implemented for many different applications. SGD algorithms can be applied to optimization problems for a function $f(\mathbf{x})$, where $\mathbf{x}$ is the vector of parameters. An example optimization problem is presented as follows:

$$\text{Minimize} F_x(\mathbf{x}), \text{where}(\mathbf{x}) = x_1, x_2, x_3, \ldots, x_n \quad (12)$$

The basic form of the SGD algorithm is given as [19]:

$$x_{i+1} = x_i - \gamma_n \nabla F_x(x_i), \tag{13}$$

where x_i is the set of design variables x at iteration i which minimize the objective function, and are to be estimated. $\nabla F_x(x_i)$ is the gradient of the function $F_x(\mathbf{x})$ to be optimized. γ is a user defined factor that controls the step size of the descent. It is also usually referred to as the *learning rate*. The choice of γ is arbitrary and is commonly set as $\frac{1}{n}$ or some other decaying function with respect to n, where n is the number of iteration steps. A very small γ will result in smaller steps and will increase the convergence time, while a larger γ may lead to an unstable process.

The SGD is very similar to the gradient descent, the difference being that the gradient of the objective function $F_x(\mathbf{x})$ is computed by an estimation, using a subset of the parameter vector which is randomly chosen in each iteration step. In the computation of Gradient Descent, the gradient in each step is calculated using all parameters. For optimization problems with high density parameters, the calculations become infeasible. The estimation of the gradient in each iteration step greatly reduces the computation costs and reduces the time required for convergence, simultaneously speeding up the optimization process. This characteristic makes the SGD very suitable for computational expensive simulations and functions which are not easily differentiable.

The SGD is susceptible at being stuck at a local minimum and is thus effective for local optimization. We propose a technique that reiteratively restarts the algorithm N times, where N is a design factor chosen by the designer, while memorizing the local minima found and the range of parameters traversed. The value of N selected is critical to the effectiveness of the algorithm; a small value may not eliminate the problem of local minima, while a very large value may considerable increase the run time of the algorithm. Hence the choice of a N depends on the topology of the circuit being designed. A response surface of the performance of the circuit being designed can give an insight into the value of N to be used. A termination criterion could also be introduced into the algorithm to exit once an optimization goal has been reached. When the algorithm is restarted with a new random point, it checks to make sure it is a new point which has not been searched, thereby eliminating redundant searches. After the algorithm has been run N times, the optimized point is selected from the set of local minima. A summary of the implementation of SGD for the optimization of the thermal sensor design is seen here:

$$\text{Minimize } P_{TS}(\mathbf{w}), \tag{14}$$

where P_{TS} is the power consumption of the thermal sensor. $(\mathbf{w}) = W_n, W_p, L_n, L_p, V_{th}...$ are the parameter variables used for the design, in this case the width of the transistors. The basic form of the SGD algorithm for this case becomes:

$$w_{n+1} = w_n - \gamma_n \nabla P_{TS}(w_n). \tag{15}$$

The design variables used are W_n and W_p, while the design objective is the power consumption with the thermal sensitivity as a design constraint. The design variables used here are a subset of the design and are chosen to illustrate the effectiveness of the modified algorithm. This methodology can also be applied to an increased parameter set without considerable computational overhead.

Algorithm 1 Stochastic Gradient Descent Optimization for Thermal Sensor.

1: **Input:** Sensor Optimization design objective and design variables with parameterized netlist.
2: **Output:** Optimal design parameters for design objective of the thermal sensor.
3: Initialize max number of iterations as $N \leftarrow Max\_Iter$.
4: **while** $N \geq 0$ **do**
5: Choose random variable w_0, w_0'.
6: Calculate thermal sensor FoM $P_{TS}(w_0)$.
7: Calculate thermal sensor FoM $P_{TS}(w_0')$.
8: **while** $||P_{TS}(w_{n+1}) - P_{TS}(w_n)|| > \epsilon$ **do**
9: Choose a decreasing γ_n.
10: Estimate $\nabla\ P_{TS}(w_n)$ using $P_{TS}(w_n')$.
11: Compute $w_{n+1} = w_n - \gamma_n \nabla P_{TS}(w_n)$.
12: **end while**
13: $W \leftarrow \{w_n, P_{TS}(w_n)\}$.
14: $N \leftarrow N - 1$.
15: **end while**
16: **return** The lowest couple $w_n, P_{TS}(w_n)$ found.

The steps are shown in Algorithm 1. The algorithm shows the modifications to the traditional SGD in optimizing an objective output $P_{TS}(w)$ as a function of design parameters w. First, the maximum iteration number is set as N, then a random starting point is chosen to start the optimization process. For each iteration step in lines 4-8, a set of solutions is stored in vector W, also marking traversed paths. The algorithm is restarted, i.e. reiterated, through lines 4-16 until the maximum iteration is reached or some other stop criteria are met. When a new random point is to be picked, it checks to make sure that this point has not been searched. At the end of the algorithm, the optimized design objective is chosen

as the minimum value in vector W. In this algorithm, we improve the efficiency by monitoring the set of random points to limit the range of parameters picked to only those whose paths have not been traversed. This cuts down on the optimization algorithm time by eliminating redundant searches, i.e. searches that will produce already stored optima or discarded results.

6. Experimental Results and Analysis

6.1. Experimental Setup and Tool Interaction

To demonstrate the efficiency of the proposed flow, it is applied to the design optimization problem of the 45 nm thermal sensor design which was discussed in section 4. Initial design parameters are as follows: V_{dd} = 1 V, and nominal values L of 45 nm and W_n, W_p of 120 nm and 240 nm, respectively, are used. The design temperature range was calibrated for an operational range of 0 – 100°C. This range was chosen for experimental purposes and a feasible range to which on-chip thermal sensors could be expected to be functional. A full blown parasitic (RLCK) netlist of the design was extracted from the layout after the initial baseline design specifications were met. The extracted netlist was then parameterized with the design variables to enable multiple iterations of the design without having to redraw the layout. In implementing the design optimization flow algorithm, several tools were used for simulation and optimization. Cadence Ocean scripts were generated to run the simulations for multiple iterations while varying the design parameters using the extracted, parameterized netlist from the physical design. The scripts and simulations were supervised by MATLAB which drove the design optimization flow. Fig. 11 shows the tool interaction for the implementation.

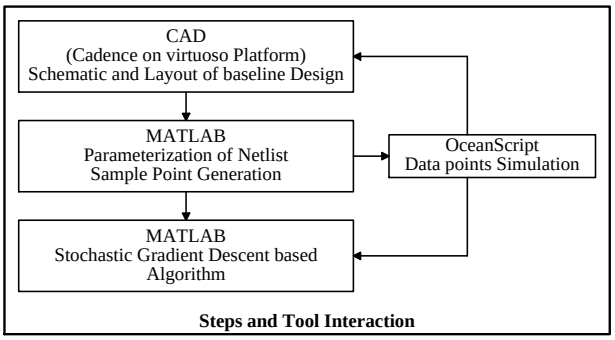

Figure 11: Experimental setup, steps and tool interactions.

6.2. Simulation of Optimization Algorithm and Design Evaluation

The optimization goal for this experiment was to minimize power consumption using temperature resolution (sensitivity) as an optimization constraint. The width of the transistors was used as the design parameter set to be explored. The SGD algorithm in Algorithm 1, was implemented in MATLAB and was used to reiteratively simulate through the design with updated inputs of transistor widths. As was discussed in section 5.2, to mitigate the possibility of the algorithm being stuck at a local minimum, the algorithm was run with N = 20, restarting the algorithm with random start values.

The iteration of the SGD algorithm exploring the design space for the optimal solution is shown in Fig. 12. The points show the solution for each iteration point of the algorithm. The points are the set of outputs obtained from each run of the SGD algorithms. From the figure, the points with higher power consumption values indicate points of local minima. By running the algorithm reiteratively and selecting the minimum output, the problem of local optimizations is eliminated.

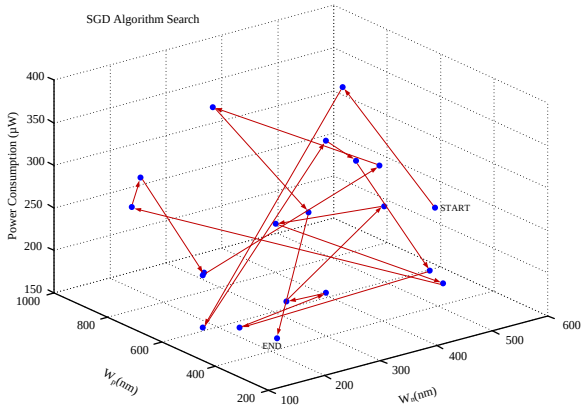

Figure 12: Iterations of the proposed SGD algorithm.

The results of the optimized design compared to the baseline design using W_n only as design parameter are shown in Table 3. The layout power consumption has been reduced by 52% with an optimal parameter point of W_n = 153 nm. The power consumption for this design is relatively higher because it includes the power consumption from the counter and the register. The designs in [4] have been implemented in the subthreshold region which significantly reduces the power consumption. A 13.75% increase in the area of the final physical design is incurred. The increase in area results from an increase of of 27.5% in the final W_n chosen.

Table 3: Experimental Results for the 45nm CMOS Optimal Thermal Sensor Circuit.

Sensor Designs	Power (P_{TS})	Sensitivity (T_{TS})	Area (μm^2)
Schematic	293.1 μW	16.88 MHz/°C	-
Layout	379.4 μW	9.42 MHz/°C	1221.37
Optimal	181.8 μW	9.42 MHz/°C	1389.31
% Change	-52.08%	0	+13.75%

For the proposed design methodology, the optimization goal was the minimization of the average power dissipation of the circuit using the thermal sensitivity as a design constraint. The SGD could also be extended to multi-objective optimization schemes which can minimize both average power dissipation and area overhead. In this case, we do not include the area overhead as a design objective as the improved proposed design already achieves a significantly reduced area by eliminating the frequency divider and multiplexer components from the motivated circuit [4].

The normalized output for the optimal power, sensitivity and area of the thermal sensor is shown in Fig. 13. The results depict the change in design specifications from schematic to layout and the final optimized values. Table 4 shows the final design parameters of the thermal sensor design.

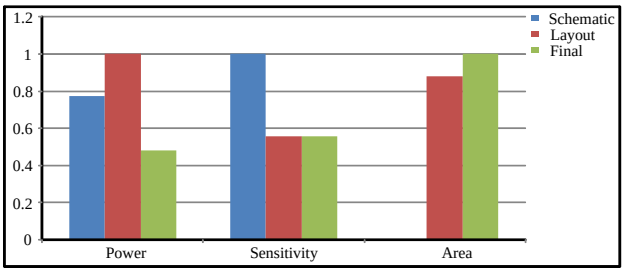

Figure 13: Final Results of the Thermal Sensor Optimization.

Table 4: Final Design Parameters of the Thermal Sensor.

Design Parameter	Initial Baseline	Final Value
$W_{n_{osc}}$	120 nm	153 nm
$W_{n_{ctr}}$	120 nm	153 nm
$W_{n_{reg}}$	120 nm	153 nm
$W_{p_{osc}}$	240 nm	401 nm
$W_{p_{ctr}}$	240 nm	401 nm
$W_{p_{reg}}$	240 nm	401 nm

One of the modifications for the SGD included the storing and checking of previously searched points to eliminate redundant searches. In eliminating the redundant search iterations, the expensive simulation time for iterations can be reduced. A lookup table type structure can be used to store the parameters for fast access compare to a simulation search time of approximately 10 minutes.

6.3. Statistical Process Variation Analysis

Further analysis of the thermal sensor design was done to study the impact of process variation on the operation of the circuit. Fig. 14 shows the probability density function (pdf) of the statistical impact of process variation on the power consumption of the thermal sensor. The simulation analysis was set up with a 1000 Monte Carlo runs. To simulate the effect of process variation as close as possible the design parameters were varied using a normal sampling distribution with a 5 % deviation from the mean. The mean values were chosen based on the optimal parameter design values obtained from the optimization algorithm. The results of the Monte Carlo analysis are shown in Fig. 14. The mean power consumption is 180. 12 μW while the standard deviation is 31.90 μW. The figure shows that the thermal sensor is statistically robust to the effects of process variation on its power consumption.

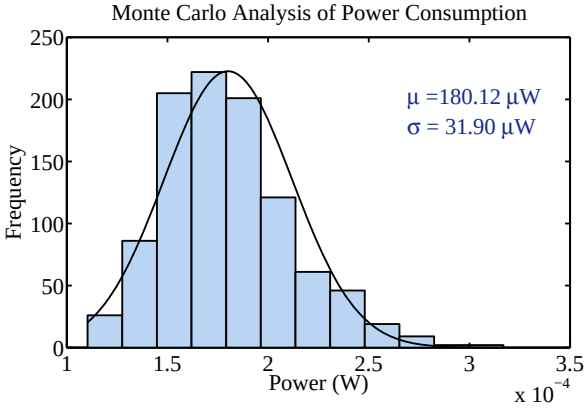

Figure 14: Probability density function of the (pdf)of the power consumption due to process variation

6.4. Comparative Perspective with similar Designs

Similar implementations of thermal sensors for on-chip sensing have been summarized in Table 5. The results from our work compare very well to similar designs for on-chip thermal sensors. The power consumption is higher than [4] which is most closely related to this work. The operating voltage is however 1 V compared to 0.3 V for [4]. Compared to the other selected

Table 5: A Summary of Selected Thermal Sensors in Existing Literature.

Sensor Design	Operating Voltage	Power Dissipation	Sensitivity Sensitivity	Area Area	Range Range	Technology Node
Bakker et al. [8]	2.2 V	7 μW	0.625°C	1.5 mm^2	-40 $\sim$ 120°C	2 μm
Chen et al. [18]	3.3 V	10 μW	0.16°C	0.175 mm^2	0 $\sim$ 120°C	0.35 μm
Datta et al. [5]	1 V	25 μW	2°C	0.04 mm^2	-40 $\sim$ 150°C	45 nm
Shenghua et al. [6]	–	0.9 μW	1°C	0.2 mm^2	27 $\sim$ 47°C	0.2 μm
Sasaki et al. [20]	1 V	25 μW	–	–	50 $\sim$ 125°C	90 nm
Pertijs et al. [21]	3.3 V	–	0.02°C	4.5 mm^2	-55$\sim$ 125°C	0.7 μm
Park et al. [4]	0.3 V	95 nW	0.4°C	0.04 mm^2	-20 $\sim$ 96°C	0.13 μm
Sheng-Huang et al. [22]	1.2 V	11.2 μW	11.9°C	54 μm^2	100 $\sim$ 150°C	65 nm
Luria et al. [14]	1.3 V	–	–	0.002 mm^2	20 $\sim$ 130°C	90 nm
[This Paper]	1.0 V	181.8 μW	0.097°C	0.001 mm^2	0$\sim$ 100°C	45 nm

designs, the power consumption is still fairly high, but the sensor design has the counter and register components which are not in designs for [5], and [20]. To further decrease the power consumption, the register component can be left out of the design. The design presented in this paper has a very high sensitivity of 0.097°Cwhich is higher than the designs presented in Table 5. The thermal sensitivity was intentionally constrained to be high enough for accurate measurements. The area overhead cost of this design is also low compared to other designs. It is noted however, that the thermal sensor was designed using a 45 nm technology compared to other designs using μm technologies.

7. Conclusion

In this paper, a new thermal sensor design for efficient on-chip temperature measurements has been proposed. A design flow optimization methodology incorporating a stochastic gradient descent based optimization algorithm has also been presented. The design flow methodology improves the design process which ensures optimal designs that mitigate some of the inherent problems in existing thermal sensors. The modified SGD algorithm is relatively fast and efficient and eliminates local optima convergence problems. The proposed technique ensures optimal designs with efficient optimization time and is used to optimize a 45 nm thermal sensor design for low power consumption while using the thermal sensitivity as a design constraint. The power consumption was reduced by 52% while maintaining the resolution of the thermal sensor at 0.097 °C. This compares very well to selected optimizations of thermal sensor designs. In future research, the proposed methodology will be extended to multi-objective optimization schemes.

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