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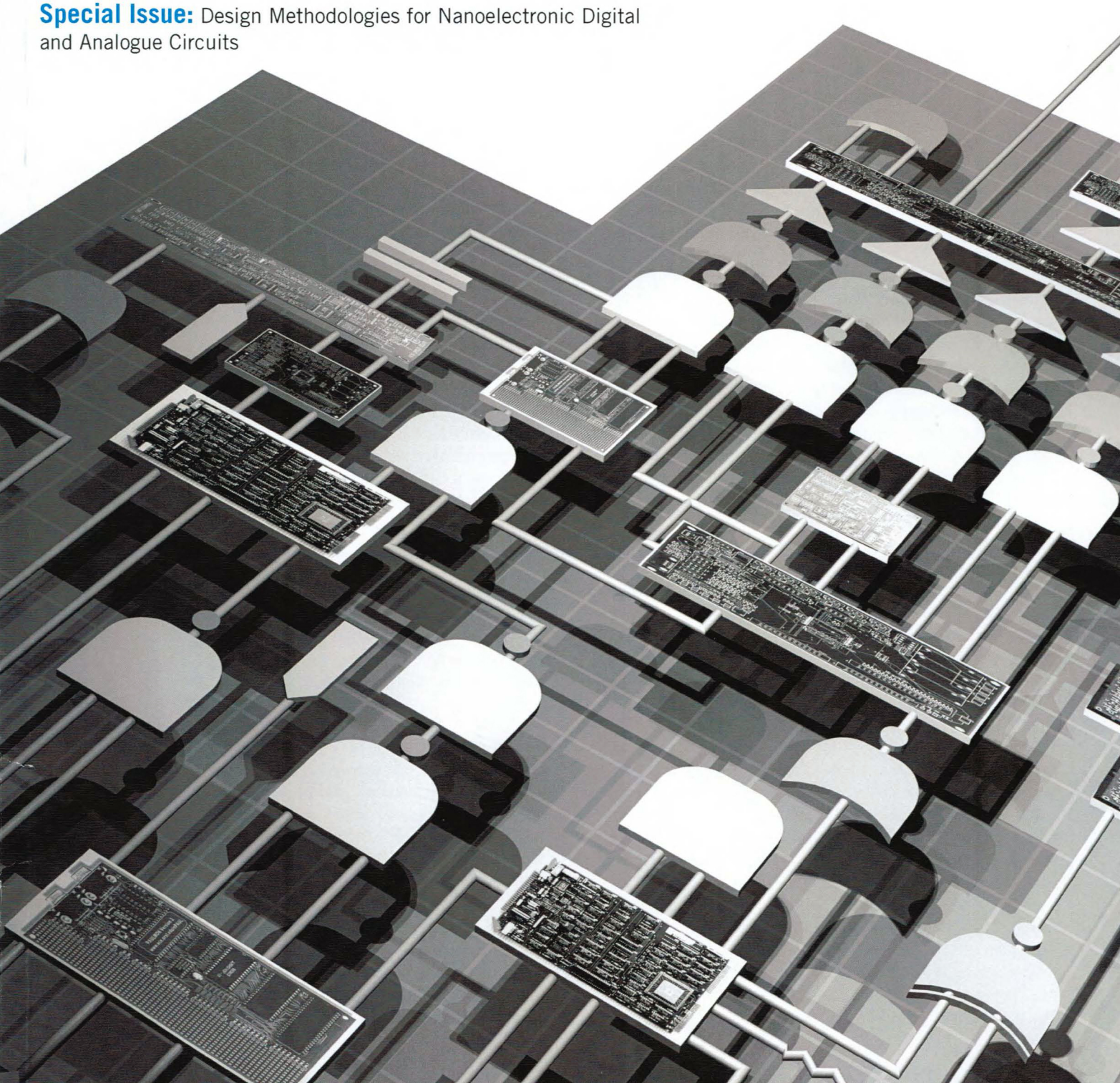
Special Issue: Design Methodologies for Nanoelectronic Digital and Analogue Circuits



Guest Editorial

Design Methodologies for Nanoelectronic Digital and Analog Circuits

Mobile computing systems, multimedia content players, and medical electronics are some of the applications that are driving strong growth in VLSI technology. While the nanoscale CMOS Field Effect Transistor (FET) is going strong with room for further scaling, other nanoelectronics technologies like Multigate FET, Graphene FET, Tunnel FET, are being researched widely as possible successors. While the key issues in design such as managing power consumption, leakage, thermal effects, process variation, reliability and security remain the same, newer technologies provide additional levers to address those problems. However, integrating new solutions with current methodologies, while producing robust and efficient chips with both high design productivity and manufacturing yield remains a challenge. With this context in mind, the special issue on "Design Methodologies for Nanoelectronic Digital and Analog Circuits" has been brought to serve VLSI researchers and design engineers.

Authors were invited to publish their original work in topics ranging from design methodologies for emerging and exploratory technologies to methodologies for system level design. While this special issue was designed to attract papers from the authors of the 2012 IEEE Computer Society Annual Symposium on VLSI (ISVLSI 2012), the submissions were open to all authors. This Special Issue collects contributions that are substantially revised versions of the papers that appeared in the conference proceedings of the ISVLSI 2012. The goal of the ISVLSI conference was to bring together researchers and practitioners working on theory, techniques and applications of VLSI design systems involving circuits, design, synthesis, analysis and system applications of VLSI design principles.

Based on reviewer recommendations, eight leading research papers were accepted for publication in this Special Issue. Consistent with accepted practice, the journal versions of the conference papers were substantially extended, and revised further following the peer-review assessment.

The range of the papers published in this Special Issue address diverse areas from the design applications of emerging technologies, to practical issues faced by current design engineers. The research issues of physical design optimization, circuit-level design exploration for nanoelectronic technology, and system level methodologies for task scheduling on multi-core systems, are covered by this set of papers.

The guest editors are extremely thankful to the reviewers for their timely reviews. A majority of the reviewers were chosen from the program committee of the ISVLSI 2012 conference, representing experts in their fields who provided high quality reviews for the papers. We thank the authors for their patience, diligence and dedication at all stages of the review process: We are grateful to the ISVLSI 2012 conference organizers and Dr. Asim Ray, Editor-in-Chief, IET Circuits, Devices & Systems, for making this Special Issue possible.

Sincerely,

Sandip Kundu, University of Massachusetts –Amherst
Saraju P. Mohanty, University of North Texas
Nagarajan Ranganathan, University of South Florida

Sandip Kundu: Sandip Kundu is a Professor of the Department of Electrical and Computer Engineering at the University of Massachusetts, Amherst. Previously, he was a Principal Engineer at Intel Corporation and Research Staff Member at IBM Corporation. He has published nearly 200 papers and holds 12 patents, given more than a dozen tutorials at conferences. He was the Technical Program Chair of ICCD in 2000, Program Co-Chair of ATS in 2011, ISVLSI in 2012 and General Chair of ICCD in 2001 and Co-General Chair of VLSI in 2005. He is a Fellow of IEEE and JSPS. He has also been a distinguished visitor of the IEEE Computer Society. He has served as an associate editor of the IEEE Transactions on Computers and Transactions on

VLSI. Currently, he serves as an associate editor of ACM Transactions on Design Automation.

Saraju P. Mohanty: Saraju Mohanty is an Associate Professor at the Department of Computer Science and Engineering, University of North Texas, Denton, TX, USA. He is the director of NanoSystem Design Laboratory (NSDL) there. His research is in "Low-Power High-Performance Nanoelectronics". His research is funded by National Science Foundation (NSF) and Semiconductor Research Corporation (SRC). He is an author of 160+ peer-reviewed journal and conference publications and 2 books. He is an inventor of 2 US patents. He has advised/co-advised 24 dissertations and theses. He serves on the organizing and program committee of several international conferences. He was a general chair for ISVLSI 2012. He serves on the editorial board of several international journals. He is a senior member of IEEE and ACM.

Nagarajan Ranganathan: Nagarajan Ranganathan is a distinguished university professor of computer science and engineering at the University of South Florida, Tampa. He has developed many special purpose VLSI circuits and systems for computer vision, image and video processing, pattern recognition, data compression, and signal processing applications. He has coauthored more than 280+ papers in refereed journals and conferences, four book chapters, and co-authored six US patents and three pending. He has edited three books titled VLSI Algorithms and Architectures: Fundamentals, VLSI Algorithms and Architectures: Advanced Concepts, IEEE CS Press, 1993, VLSI for Pattern Recognition and Artificial Intelligence, World Scientific Publishers, 1995, and coauthored a book titled Low Power High Level Synthesis for Nanoscale CMOS Circuits, Springer, June 2008. He was elected as a Fellow of the IEEE in 2002 for his contributions to algorithms and architectures for VLSI systems. He is a member of the IEEE Computer Society, the IEEE Circuits and Systems Society, and the VLSI Society of India. He has served on the editorial boards for several IEEE and ACM journals. He served on the steering committee of the IEEE Transactions on VLSI Systems during 1999-2003 and 2007-10 and as the editor-in-chief for two consecutive terms during 2003-2007. He received the Distinguished University Professor honorific title and the University Gold Medallion honor in 2007. He was a co-recipient of the Best Paper Awards at the International Conference on VLSI Design in 1995, 2004, and 2006, as well as the IEEE Circuits and Systems Society Transactions on VLSI Systems Best Paper Award in 2009.