Guest Editorial

Advanced Techniques for Efficient Electronic System Design

The electronic systems that process signals and multimedia are omnipresent and affect every aspect of current society. Signal and multimedia are processed and stored everywhere and every moment. It can be a video played by a user in a smart mobile phone, an audio played in a car stereo, or even a doctor capturing and checking a X-ray image. Thus, there is always need for techniques for efficient, low-cost, robust, and secure design of the electronic systems efficient storage, communication and embedded processing. This special issue of the journal of *Circuits, Systems, and Signal Processing* on *Electronic System Design (CSSP)* contains a set of papers which present highly interesting state of art methodologies and circuits relating to different important aspects of electronic system design including the multi-standard communication, digital watermarking, memory Integrity detection and protection in embedded systems, information security in systems-on-chip (SoC), and the elliptic curve cryptography and error control coding. This special issue of the journal of *Circuits, Systems, and Signal Processing* on *Electronic System Design* (CSSP) contains five papers which present highly interesting state of art methodologies and circuits relating to different important aspects of electronic system design including the multi-standard communication, digital watermarking, memory Integrity detection and protection in embedded systems, information security in a system-on-a-chip (SoC), and the elliptic curve cryptography and error control coding.

Channelization is an essential computation-intensive function for multi-standard communication. The paper entitled “A Low-Complexity Uniform and Non-uniform Digital Filter Bank Based on an Improved Coefficient Decimation Method for Multi-Standard Communication Channelizers” by Abhishek et al. provides an efficient low-complexity solution for this important function. In this paper, the authors present a novel filter bank (FB) design technique based on the combination of the conventional coefficient decimation method (CDM) and the recently proposed modified coefficient decimation method. It is shown that the proposed FB has superior stop band and transition band characteristics, and involves significantly lower complexity compared with the conventional CDM-based progressive decimation filter bank (PDFB). The proposed approach provides uniform as well as non-uniform subbands to be used for multi-standard channelization in wireless communication receivers. It is demonstrated in this paper that the proposed FB offers 74% reduction in multiplication complexity over the PDFB, when used for non-uniform multi-standard channelization with a fixed frequency channel distribution. If the same FB is used for multi-standard channelization with variable locations of the frequency channels, it reduces the multiplication complexity to half of that of the PDFB.

Identification of ownership of copyright of digital multimedia content has always been a challenging problem. Digital watermarking is a potential solution for copyright protection for multimedia content. Imagine the number of videos being played through YouTube! It is used to embed the copyright information in digital content. The paper entitled "Watermarking Hardware Based on Wavelet Coefficients Quantization Method" by Darji et al. provides hardware assisted watermarking approach to achieve low power consumption, real-time performance, reliability, and easy integration with existing consumer electronic devices. It presents an efficient architecture for transform domain watermarking using quantization approach for very-large scale integration (VLSI) implementation of robust and blind image watermarking.

The article "MEM-DnP a Novel Energy Efficient Approach for Memory Integrity Detection and Protection in Embedded Systems", by Nimgaonkar et al. addresses an important security issue in embedded systems. In this paper the authors present a novel energy efficient approach for memory integrity detection and protection. The key design feature proposed here is that it can adaptively perform the memory integrity verification using on-chip sensors, which significantly reduces the energy overhead imposed on an embedded system over the conventional implementation of memory integrity verification. Simulation results show that the energy consumption of the proposed combined detection and protection mechanism is almost half of that of the existing approach for this function.

Network on Chip (NoC) is being explored as an efficient solution to the existing scalability problems with the SoCs. It is, however, highly vulnerable to security threat that results due to extraction of secret information from IP cores. The paper "A Security Framework for NoC Using Authenticated Encryption and Session Keys" by Kapoor et al. addresses this security concern in SoC. In this paper, the authors present a security framework for NoC based SoC using authenticated encryption. The security infrastructure which is made to reside in Network Interface (NI) of every IP core allows secure communication among those cores. The secure cores can communicate using permanent keys whereas temporary session keys are used for communication between secure and non-secure cores. A traffic limiting counter is used to prevent bandwidth denial and access rights table avoids unauthorized memory accesses. It is shown that the security did not affect the network performance except some initial latency.

The binary finite extension field GF(2^m) is widely used in elliptic curve cryptography (ECC) and error control coding. The paper "An Efficient Look-up Table-Based Approach for Multiplication over GF(2^m) Generated by Trinomials" by Meher et al. provides optimized look-up table (LUT)-based designs of multipliers for GF(2^m) generated by Trinomials. A digit-serial LUT-based design with digit size 4 is proposed in this paper to have lower area-delay complexity. Besides, a digit-parallel LUT-based design is proposed for high-speed applications, using the same LUT as the digit-serial design, at the cost of some additional multiplexors and combinational logic for parallel modular reductions and additions. A simple circuit is proposed here for the initialization of LUT content, which can be used to update the LUT in three cycles whenever required. The proposed digit-serial design involves less area complexity and less time-complexity than those of the existing LUT-based designs. The proposed digit-parallel design offers nearly 28% improvements in area-delay product over the best of existing LUT-based designs. Moreover, in this paper, the authors have designed a reconfigurable multiplier with negligible reconfiguration overhead that can be used for more than one field.

The guest editors are thankful to the reviewers for their timely and high quality reviews, and thank the authors for their patience and co-operation at all stages of the review process. We are grateful to Professor. M. N. S. Swmay, Editor-in-Chief, Springer *Circuits, Systems, and Signal Processing* on *Electronic System Design (CSSP)* Journal, for support and guidance to make this Special Issue possible.

Sincerely,

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Saraju P. Mohanty earned his Ph.D. in Computer Science and Engineering from the University of South Florida in 2003. He obtained Masters degree in Systems Science and Automation from the Indian Institute of Science, Bangalore, India in 1999, and Bachelors degree (Honors) in Electrical Engineering from Orissa University of Agriculture and Technology, Bhubaneswar, India in 1995. He is currently an Associate Professor at the Department of Computer Science and Engineering, University of North Texas (UNT), Denton, TX, USA and the director of NanoSystem Design Laboratory (NSDL) at UNT. His main area of research is "Low-Power High-Performance Nanoelectronics". His research is funded by National Science Foundation (NSF) and Semiconductor Research Corporation (SRC). He is an author of 160+ peer-reviewed journal and conference publications and 2 books. His first book titled "Low Power High Level Synthesis for Nanoscale CMOS Circuits" was published by Springer in June 2008. His publications are well-received by the world-wide peers with a total of 1500+ citations resulting in an H-index of 21 and i10-index of 43 (from Google Scholar). He is an inventor of 2 USA patents. He has advised/co-advised 24 dissertations and theses. Six of these advisees have received outstanding student award at UNT. The students are very-well placed in industry and academia. He has received Honors Day recognition as an inspirational faculty at the UNT for multiple years. He serves on the organizing and program committee of several international conferences. He was a general chair for IEEE-CS Symposium on VLSI (ISVLSI) 2012. He serves on the editorial board of several international journals. He has served as a guest editor for many journals including ACM Journal on Emerging Technologies in Computing Systems (JETC) titled "New Circuit and Architecture Level Solutions for Multidiscipline Systems", in August 2012. He is a senior member of IEEE and ACM.

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