Power, Parasitics, and Process-Variation (P3) Awareness in Mixed-Signal Design

Modern consumer electronic systems such as, smart mobile phones, media players, have profound effect on day-to-day life in the society. These systems consist of multiple heterogeneous components like digital cores, analog circuits, radio-frequency (RF) components, memory, system software, and application software. These, in a unified way, can be called as Analog/Mixed Signal Systems-On-Chip (AMS-SoCs). The aim of this special issue is to cover design techniques and computer-aided design (CAD) techniques that incorporate power, parasitics, and process-variation (P3) awareness in these AMS-SoCs.

Power dissipation has significant impact on every aspect of the AMS-SoCs. Acceptability, reliability, and profitability of these AMS-SoCs depend as much on power efficiency as on performance. The battery technology that can't cope up with the VLSI or software technology can follow the roadmap of AMS-SoC if the power dissipation is minimal. Another issue of the AMS-SoC design is that the exact performance prediction is very challenging due to large parasitic (RCLK) effects of the digital, analog, and RF circuits. The parasitics arise due to interconnects in the circuits as well as due to the active elements. However, it is difficult to estimate the parasitic effects before the circuit is implemented. Therefore, to improve design efficiency and reduce time-to-market, it is crucial to be able to predict parasitic effects for accurate performance and then integrate techniques to compensate the effects. The design cycle of the AMS-SoCs is complicated by the impact of process variation due to the use of state-of-the-art nanoscale technologies for fabrication. The process point, which is the center of the distribution of the process-parameters, may not be the best design point to maximizing yield. Therefore AMS-SoCs need to be designed to perform across the entire process and operating environment to enhance the yield.

This special issue of the Journal of Low-Power Electronics (JOLPE) presents research results that address one or more of these P3 issues in AMS-SoC components. The special issue will be a great reading for researchers, educators, students, and industry personnel, interested in AMS-SoC design. The special issue has 9 papers selected after rigorous review.

The authors in "A Programmable Oversampling CMOS Delta-Sigma Analog-to-Digital Converter for Low-Power Interface Electronics" reduce the power dissipation of ADC useful for wireless sensor networks. The low-power technique relies on programming the ADC to give different output resolution bits. The phase-locked loop (PLL) which is the time keeper of all synchronous systems or circuits is analyzed for hot-carrier effects in "CMOS Phase-Locked Loop Circuits and Hot Carrier Effects". This also includes the low power design of a 3V 30mW PLL frequency synthesizer. The design in "2.4-/5.2-GHz Concurrent Dual-Band Wireless Local Area Network Transmitter", consumes minimal power while generating dual-band. The transmitter's architecture that uses combined direct-conversion and parallel schemes to achieve

concurrent multi-band operation results in power dissipation as well as system size reduction. Authors present a low-power for cardiac infarction in "A Low-Power Instrumentation System for Nano-electro-mechanical-Sensors for Environmental & Healthcare Applications".

The authors in "Accurate Polynomial Metamodeling-Based Ultra-Fast Bee Colony Optimization of a Nano-CMOS PLL" present a methodology for fast design exploration of PLL. The methodology combines polynomial-metamodel representation of AMS-SoC components and intelligent algorithms. Statistical analysis of mixed-signal components for fast statistical process variation analysis of nanoscale circuits is presented in "Enhanced Statistical Blockade Approaches for Fast Robustness Estimation and Compensation of Nano-CMOS Circuits". The method called statistical blockade uses intelligent sampling to speedup traditional Monte Carlo. In "POWER-SIM: An SOC Simulator for Estimating Power Profiles of Mobile Workloads", authors devised a low-power method by combing using application and user profiles.

No matter what, the systems cannot operate without power. The authors in "Implementation of Smart Battery Charger with Low Power PV Energy System Using Synchronous Buck Converter" deal with battery charger. The photo-voltaic battery charger relies on a soft switching DC-DC converter to efficiently charge lithium-ion battery. A futuristic power distribution mechanism is discussed in "An Architecture Using Lighter-Than-Air Platforms for Retail Power Beaming and Communications". The authors envision that the proposed systems can be used to the delivery of power to remote areas and make low-cost communications systems available to wider public in the society.

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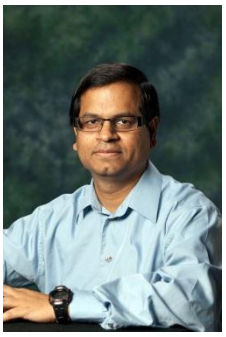
Guest Editor



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