2012
Volume 8, Number 3

ACM Journal on

Emerging Technologies in Computing Systems

ACM Journal on Emerging Technologies in Computing Systems Vol. 8 • No. 3 • 2012 Articles 14-25

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Association for Computing Machinery

Advancing Computing as a Science & Profession

New Circuit and Architecture Level Solutions for Multidiscipline Systems

The demand for ever smaller and portable electronic devices has ultimately driven the scaling of CMOS to its physical and electrical limits. Transistor feature sizes have dramatically shrunk with technology scaling and the gate dielectric thickness has reached the range of just a few mono-layers of SiO_2 in nanoscale CMOS or nano-CMOS devices. Consumer grade chips with 32nm CMOS transistors are everywhere and available at an affordable price. The search for sub-22nm CMOS technology is in full swing. It is expected that 10nm CMOS with a channel consisting of a few layers of electrons will be available soon. At the same time, the search of an alternative to eventually replace CMOS is ongoing in both industry and academia. Alternative nanodevices such as carbon nanotubes, quantum-dots, deoxyribonucleic acid (DNA) transistors, and single-electron devices (SET) have been introduced to replace the classical and ubiquitous CMOS transistors. In addition, manufacturing processes originally developed for the fabrication of silicon-based integrated circuits have been adapted for the development of micro-electro-mechanical systems (MEMS) or nano-electro-mechanical systems (NEMS). The next stage in this progression is the assembly of nanoscale devices and NEMS to build integrated multidiscipline emerging systems. The design of such large and complex multidiscipline systems needs new methodologies. This special issue discusses new research findings in that direction.

Srivastava, Xu, Liu, Sharma, and Mayberry, in “CMOS LC Voltage Controlled Oscillator Design Using Carbon Nanotube Wire Inductors” present the use of carbon nanotubes (CNT) for LC-VCO design. LC-VCO is the component of the phase-locked loop (PLL) that generates a sustained clock signal in synchronous circuits and systems. In the proposed design, the inductor in the LC tank circuit is realized from a Carbon Nanotube (CNT) bundle wire. Single-walled carbon nanotube (SWCNT), and multi-walled carbon nanotube (MWCNT) wires are used. The presented LC-VCO design is symmetrical and has good phase noise and large voltage swing. One attractive feature of the CNT based LC-VCO is that at higher frequencies the CNT interconnect has lower resistance and negligible skin effect. Thus, a CNT based LC-VCO can be used for high-frequency clock generation in synchronous emerging systems.

In the sub-22nm CMOS technology the channel size consists of a few layers of electrons only. Process variation still remains and will remain the most important issue in nanoscale technologies. Mahalingam, Ranganathan, and Hyman in “A Variation Tolerant Circuit Design Technique using Dynamic Clock Stretching”, present a solution that can mitigate process variation problems in synchronous circuits and systems. Most of the existing solutions for nanoscale process variation tolerance are static solutions. The existing solutions use some form of statistical techniques during the design phase so that high-yield circuits can be obtained. In a paradigm shift, the solution proposed by Mahalingam, Ranganathan, and Hyman works on the fly. This is a dynamic solution that stretches the clock in the destination flip-flops dynamic delay detection circuit to identify the uncertainty in delay due to process variation. This solution will work for other nanoscale technologies as it does not rely on a specific technology and is at a higher-level of design abstraction and post-silicon phase.

Roy, Mitra, Bhattacharya, and Chakrabarty, in “Pin-Constrained Designs of Digital Microfluidic Biochips for High-Throughput Bioassays”, propose an important solution to handle the increasing number of external control pins. Bio-chips can be deployed in many applications including environmental pollution control and health care management. The paper presents a new solution for the layered wire-routing for the pin-constrained biochips which can be used for concurrent execution of the same bioassay. This is accompanied by a hierarchical solution to preserve the simplicity of wire routing and the scalability of biochip layout. Thus, the proposed solutions are unique contributions to the MEMS design methodology.

Komerath and Kar in “Retail Beamed Power for a Micro Renewable Energy Architecture: Survey”, discuss multidiscipline systems in a different scale of magnitude and can be envisioned as system of systems. The paper discusses space-based renewable power generation. The law of nature, the simple conservation of energy law, dictates that power/energy dissipation can’t be zero irrespective of the best possible low-power / energy-efficient solutions. There is need for wider and efficient energy-delivery systems at the same time working on low-power or energy-efficient system designs. At the same time restrictions in battery technology do not allow the storage of a large amount of power. The architecture solutions discussed in this paper fill the need. The paper advocates the use of narrow-band power delivery as focused beams from central power plants to rural distribution points and space satellites.

The guest editor would like to sincerely acknowledge the Editor-in-Chief of ACM Journal on Emerging Technologies in Computing Systems (JETC) Dr. Krishendu Chakrabarty. The Association for Computing Machinery (ACM) is acknowledged for the production of this issue. The guest editor thanks all the authors who contributed to the special issue. All the reviewers who contributed their invaluable expertise and time towards this special issue are acknowledged.

Denton, TX, USA — Saraju P. Mohanty

01st March 2012 — Guest Editor