A Comparative Study of Metamodels for Fast and Accurate Simulation of Nano-CMOS Circuits

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***Abstract*—Fast simulation is a bottleneck for design space exploration of complex nanoscale CMOS (nano-CMOS) Analog and Mixed-Signal (AMS) circuits. This paper presents the use of "metamodels" for fast and accurate AMS circuit design exploration. A design process flow that uses metamodels is introduced. Metamodel generation is the most time consuming step of the design flow. Consequently, accurate and fast sampling of the design space is essential for the creation of the metamodel. Different sampling techniques are investigated to minimize the number of samples required. This paper uses two nanoscale CMOS analog circuits: a 45 nm Ring Oscillator (RO) and a 180 nm LC-VCO, as case studies. It is observed that the parasitics generated from the physical design of the circuits have a drastic effect on their performance metrics, such as frequency. Four alternative sampling techniques, both random (Monte Carlo, MC) and uniform (Latin Hypercube Sampling, LHS, Middle Latin Hypercube Sampling, MLHS, and Design of Experiments, DOE), are considered and compared for speed and accuracy. This paper provides a thorough exploration of these sampling techniques to determine which one is more suitable to minimize sampling size for metamodel generation and optimize the design cycle. Experiments show that LHS sampling is best for both circuits, followed by MLHS, MC and DOE. In this paper it is also shown that polynomial metamodels of order higher than two (which are commonly used) provide best accuracy.**

***Keywords*-Nanoscale CMOS, Mixed-Signal Circuits, Metamodeling, Statistical Sampling, Circuit Simulation**

I. Introduction and Motivation

Today's large analog circuits have very long design cycles as accurate continuous time transistor-level simulation is very computationally intensive. This situation is further exacerbated due to the use of compact models with hundreds of parameters in nano-CMOS technology and the need for accurate parasitic estimation in the sign-off netlists [1], [2]. In the optimization stage the original design is usually iteratively tuned by adjusting design parameters of the circuit to meet the target design specifications. Vast amounts of different design possibilities are available due to the large number of design variables. It is an impossible task to do exhaustive design space exploration for complex nano-CMOS circuits to find an optimal solution. Performing a fast search using a *metamodel*, which is an abstracted model of a netlist, or surrogate model, can be used as an alternative to the exhaustive search of the *actual circuit's* design space. Different levels of abstraction are already used in the hierarchy of models for typical circuit design. At the lowest level, transistors are used to create netlists of small design units which are further stitched into subsystems and finally, into complete systems.

The model of a circuit typically includes parasitics which are extracted from the final layout and thus is a very large, hierarchical netlist. An accurate metamodel for that design can be obtained by sampling data from the simulated circuit to find optimal values for the design specifications. The metamodel is a mathematical prediction model which acts as a substitute (surrogate) for the original model [3], [4], [5]. It is vital to generate the closest possible results for a given circuit that can be manufactured with minimal tolerance of error since it is a very expensive process to correct functional and design errors. Circuit simulation tools are used in different design steps to simulate circuits. Simulations for very complex circuits can potentially take days to weeks to complete. Hence the need to minimize the time of the design process and therefore the amount of simulation iterations needed. Since metamodels are mathematical models they introduce a simpler way of understanding the behavior of the circuit and are easier and faster to conduct simulations with multiple iterations, and apply optimization techniques. A designer needs to sample the response of the simulated circuit only a limited number of times, sufficient to construct the metamodel. This work is targeted towards investigating which sampling technique works best for polynomial function metamodels using two different case study mixed-signal nano-CMOS circuits with full parasitic extraction, constructed in two different technologies.

The rest of the paper is organized as follows: Section II discusses the contributions of this paper. Section III discusses prior research relevant to the current paper. Section IV discusses a metamodel-based design flow. Section V discusses a 45 nm CMOS ring oscillator and a 180 nm CMOS LC-VCO which are used as case study circuits in this paper. Section VI introduces the different sampling techniques along with the derived metamodels. Section VII presents the conclusions of this research along with directions for future research.

II. Contributions of this Paper

The *novel contributions* of this paper are as follows:

1) Circuit simulator and language independent metamodeling techniques are proposed, which can be used to accurately represent actual circuits.
2) Four distinct random and uniform sampling techniques are investigated for data sampling for metamodel creation. They include Monte Carlo (MC), Latin Hypercube

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Sampling (LHS), Middle Latin Hypercube Sampling (MLHS), and Design of Experiments (DOE), and are applied to nano-CMOS circuits.

3) The use of these sampling techniques in metamodeling is demonstrated for a 45 nm CMOS ring oscillator and a 180 nm CMOS LC-VCO. The ring oscillator is characterized for frequency, power and jitter, while the LC-VCO is characterized for frequency, power and phase noise. Full RCLK (resistance, capacitance, self and mutual inductance) parasitic extractions are performed and compared to the schematics for both oscillators. The metamodels are generated on the parasitic netlist.
4) Metamodels of different order are generated and compared for speed and accuracy.

III. Related Prior Research

Fast design exploration approaches can be essentially broken down into several distinct groups including macromodeling and metamodeling [6]. Fig. 1 shows a taxonomy diagram of previous published research in each one of these groups. These are discussed in the rest of this section.

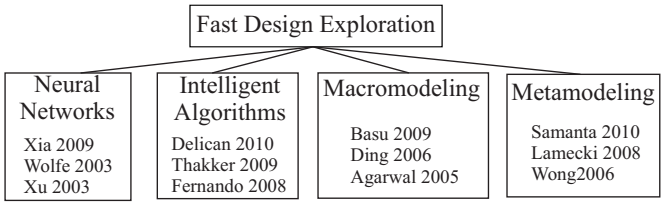


Fig. 1. Techniques for fast CMOS circuit design exploration.

Neural networks have been used to tackle the complexity of circuit optimization. A trained neural network preforms well for a large number of parameters based on a limited amount of simulation data points. In [7], the creation of neural networks for the estimation of the output of operational amplifiers from a high level perspective is given. However, this approach does not account for parasitics which has serious impact on circuit performance and hence can dramatically affect the estimation. In [8], the use of neural networks in the automatic synthesis of op-amps is explored. In [9], a feed-forward dynamic neural network model is introduced for amplifier and mixer circuits directly from input-output large-signal measurements.

Intelligent algorithms have also been explored for optimization over actual circuits. In [10], the artificial bee colony optimization algorithm is investigated considering the transient performance of a CMOS circuit. In [11], a hierarchical particle swarm optimization algorithm is proposed that performs automatic sizing of analog circuits in order to obtain low-power designs. In [12], a novel genetic algorithm is proposed for floor planning for gigascale complexity that simultaneously minimizes the total wire length and silicon area.

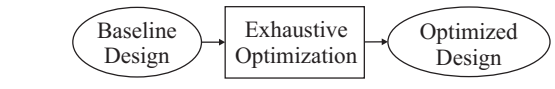
Macromodeling has been extensively investigated as a method to reduce circuit complexity in which a simpler circuit model is developed. The design process is still closely coupled to the circuit simulator and hence exhaustive Monte Carlo simulations can be still very time consuming. In [13], a variation-aware performance macromodeling technique is presented for analog building blocks for faster convergence during synthesis. In [14], performance macromodeling is presented using a sequential design space decomposition technique. In [15], macromodels for the feasible design regions (instead of the entire design space) are hierarchically generated, until the desired accuracy was achieved.

Metamodeling is recently becoming a popular alternative to macromodeling as an approach that represents the circuit using mathematical functions (contrary to circuit simulator specific simplified models as is the case of macromodels). In [16], a surrogate modeling approach for expensive circuit-level simulation is presented that uses support vector machine (SVM)-based machine learning. In [17], an automated creation technique for surrogate multivariate mathematical models is proposed for microwave components. In [18], a surrogate modeling approach is also used for statistical wire-length estimation.

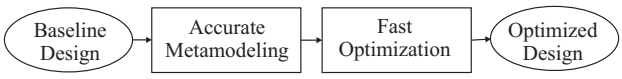
IV. The Proposed Metamodel Based Simulation and Optimization Flow

In order to obtain an optimal design, a designer can optimize the actual circuit model (a SPICE netlist). This optimization on the actual circuit (Fig. 2(a)) is very slow and may be even impossible for complex and nanoscale circuits with large numbers of transistors and interconnects. For fast, yet accurate design optimization of analog circuits this paper proposes the approach demonstrated in Fig. 2(b). In this approach, metamodels of the circuit model are first generated. The circuit optimization is then performed on the metamodels instead of the actual circuit. This makes the design exploration fast and accurate. It may be noted that *metamodeling is not macromodeling* [19], [8]. Macromodels are reduced complexity models but they rely on the same type of modeling and simulator as the original models (e.g., SPICE). In the *metamodeling approach, the underlying system is completely decoupled from the simulator and the resulting metamodel (i.e., mathematical model of the circuit) is more general, flexible and easier to simulate and optimize than macromodels*. In summary, a metamodel has the following distinct features over the macromodels:

1) It is a mathematical representation of the circuit output.
2) It is a prediction equation.
3) Metamodels can be used in a variety of tools, such as MATLAB, and are language independent.



(a) Traditional (slow) approach



(b) Proposed metamodeling-based (fast) approach

Fig. 2. Fast design space exploration of analog circuits through accurate metamodeling. *Comparing different statistical sampling techniques and metamodels is the scope of this paper.*

The proposed design flow is shown in Fig. 3. In this flow, first the logical design is performed and tuned to meet the required specifications. At this point the initial physical design is implemented (this is the 1st manual layout step). The physical design is then subjected to Design Rule Check (DRC), Layout vs. Schematic (LVS) comparison and parasitic (RCLK) extraction. If the specifications are not met, the parasitic netlist is then parameterized with design variables that can be considered in the circuit. This netlist is then used by our automated process to create a metamodel by applying sampling techniques as described in this paper. Once the metamodel is created, it can be further optimized to find the parameter set for the variables that were chosen before. The parameters that are generated in the optimization stage are then used to adjust the initial physical layout resulting in the final product (this is the 2nd manual layout step).

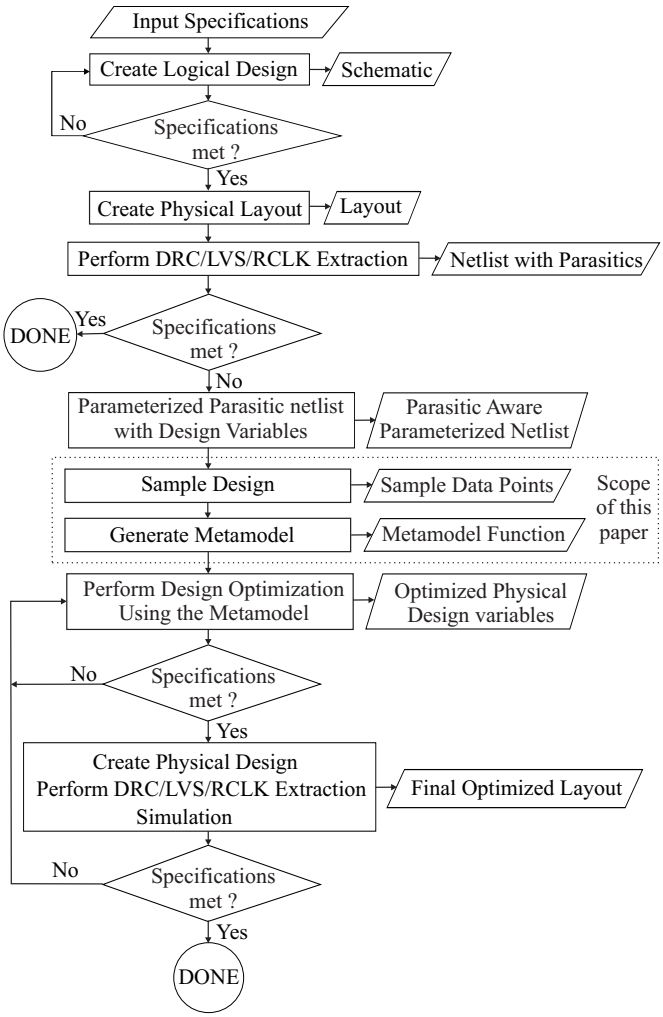


Fig. 3. The Proposed metamodel-based design (simulation and optimization) flow. It requires only two manual layouts and hence results in significantly faster design cycle.

Designers only need to create the physical design two times, the initial design to sample the data and the final design after the optimization of the metamodel. In this approach, for the algorithm to work properly, the key element is the generation of a very accurate metamodel. Hence this paper covers metamodel sampling techniques and their accuracy, as indicated in Fig. 3.

V. Design and Characterization of the Case Study Circuits

Two circuits are considered as case studies. They are designed for 45 nm and 180 nm CMOS technologies, depending on the library components available for their physical design.

A. 45 nm CMOS Ring Oscillator (RO)

A Ring Oscillator (RO) consists of an odd amount of inverters with a feedback loop. The feedback loop creates oscillations that are derived from the propagation delay of each inverter. ROs are useful in die and new technology testing and are commonly used to find the delay times of logic gates. They are also the main element in temperature sensors.

1) Logical Design of the 3 Inverter Ring Oscillator: Fig. 4 shows the schematic diagram of a three inverter RO. For a given technology node, the designer can adjust the widths of the NMOS and PMOS to obtain the desired frequency. The design space is spanned by the two widths in the identical inverters of the RO. Assuming that all inverters in RO have the appropriate size transistors, their fall and rise times are identical. The frequency of oscillation is calculated as follows [20]:

$$f = \left(\frac{1}{2Nt_p}\right), \tag{1}$$

where N is the number of inverters, which is odd, and t_p is the propagation delay of each inverter.

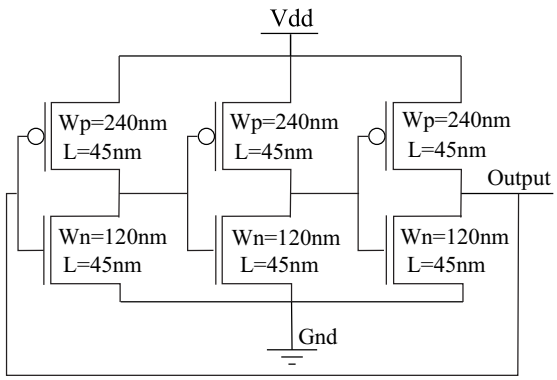


Fig. 4. Transistor-level schematic of the ring oscillator.

The design variables chosen for this design are: width of NMOS W_n = 120 nm and width of PMOS W_p = 240 nm at a nominal operating voltage $V_{dd} = 1$V and minimal technology length of L =45 nm. The ambient temperature of 27 °C is assumed to be constant for all simulations since temperature can affect the output dramatically. Temperature analysis for self-heating effects is not taken into account in this paper.

2) Physical Design of the 3 Inverter Ring Oscillator: As shown later in this section, the parasitics in analog nano-CMOS circuits have a very dramatic effect on performance. It is difficult to estimate these effects without actually performing the physical layout, which is shown in Fig. 5. The full

SPICE netlist is generated from RCLK parasitic extraction from this layout. The physical design which involves tedious labor-intensive work, particularly for complex circuits, can be shortened by using the proposed *metamodeling design flow will only needs two layout steps*: once for the initial design and one final time, after obtaining the optimized data from the metamodel. This is a *major outcome of the proposed metamodel-based design flow*. It may be noted that in a convectional flow, multiple layouts may be needed to meet design closure. Comparison for the number of components between the regular schematic and the parasitic netlist is shown in Table I.

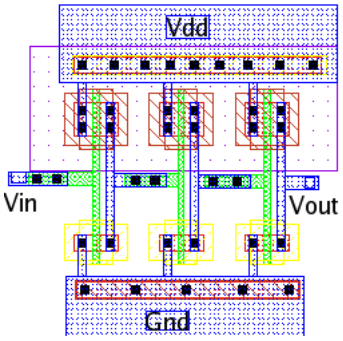


Fig. 5. Ring oscillator physical design for a 45 nm CMOS technology.

A dramatic decrease in frequency is observed in simulations using the parasitics from this layout versus the regular schematic simulations. For this simple circuit the simulation run time has increased by a factor of 3 due to the presence of parasitics. Contemporary complex circuit with thousands of transistors can have simulation times in days, if not weeks, depending on the complexity of the circuit. The change between the schematic and parasitic results is of the order of 40%. It is observed that the total power consumption has not been altered, and only changed by merely 1%. Table II shows a comparison between the simulation results with and without parasitics. From these results we can conclude that the extraction of parasitics is necessary to calculate the desired output such as the frequency for this circuit. On the other hand, when adjusting the widths of the CMOS components to $W_n = 360$nm and $W_p = 720$nm in the physical layout no drastic effect on the output frequency was observed.

TABLE II
RING OSCILLATOR CHARACTERIZATION FOR WIDTHS OF NMOS=120 NM AND PMOS=240 NM.

Design	Power	Frequency
Schematic (no parasitics)	27.17μW	16.21 GHz
Physical (with parasitics)	26.96μW	9.88 GHz

The eye diagram of the physical design of the ring oscillator is shown in Fig. 6. It is evident that the jitter effect of physical design for a 100 ns period is negligible, even when full parasitics are taken into account. Hence this paper will address frequency as it is the most important performance metric of the ring oscillator.

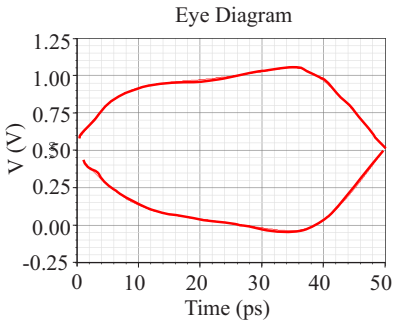


Fig. 6. Eye diagram of the physical design of the ring oscillator.

B. 180 nm CMOS LC-VCO

In this paper, a conventional complementary NMOS and PMOS cross-coupled VCO circuit is used as a case study.

1) Logical Design of LC-VCO: The physical design is shown in Fig. 7. For the LC-VCO the frequency is obtained using the following expression:

$$f_{osc} = \frac{1}{2\pi\sqrt{L_{tank}C_{tank}}} \quad , \tag{2}$$

where L_{tank} is the inductor and C_{tank} is the capacitor. C_{tank} is calculated using the following expression:

$$C_{tank} = C_1 + C_2 + C_{other} \quad , \tag{3}$$

where C_1 and C_2 are the capacitances of the varactors, and C_{other} is the summation of the NMOS and PMOS gate to drain/source and other parasitic capacitances of the circuit. The inductor tank is chosen to be as large as possible with a corresponding capacitor tank, which leaves transistor sizing to minimize the power dissipation. Since the LC-VCO has to be a symmetric circuit, all the components mirror each other to produce V_{outp} and V_{outn} with the same frequency. Therefore the couples of PMOS and NMOS transistors should have identical geometries and are denoted as parameters W_p and W_n, respectively.

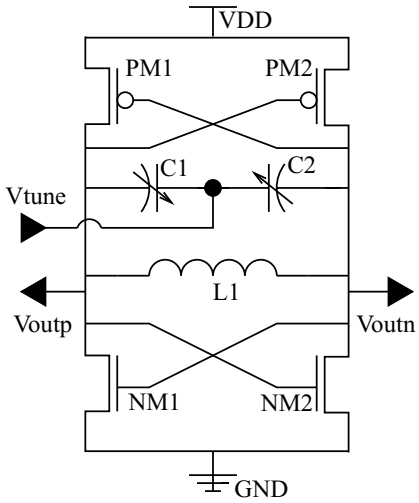


Fig. 7. LC-VCO schematic representation.

TABLE I
NUMBER OF COMPONENTS IN EXAMPLE CIRCUITS: RING OSCILLATOR AND LC-VCO.

	Simulation	Transistors	Capacitors	Resistors	Inductors	Total
Ring Oscillator	Without parasitics	6	0	0	0	6
	With parasitics	6	82	19	0	107
LC-VCO	Without parasitics	4	2	0	1	7
	With parasitics	4	108	600	14	726

2) Physical Design of the LC-VCO: The physical design of the LC-VCO is shown in Fig. 8. The symmetry of the layout provides even-order distortion in the differential output waveform and up-conversion [21]. The wire width is maximized to minimize wire resistance and it also provides space for future size change of the devices after the optimization physical design generation step, as discussed in section IV.

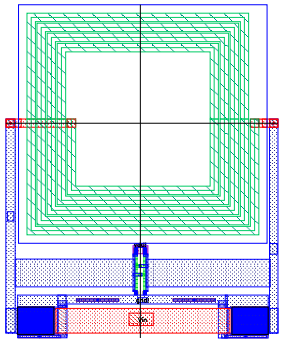


Fig. 8. LC-VCO physical layout for 180 nm CMOS technology node.

The simulation on the parasitic extracted netlist with the same sizing of the devices as in the schematic shows the impact of parasitics on the circuit. The netlist that is generated from the physical layout is parameterized for further simulations. For simplification of the analysis it is assumed that performing minor modifications on some devices will not have drastic effects on the parasitics of the future layout. In this way the optimization on the sizing of the devices for this circuit can be performed with extracted parasitics and only considering the parasitics in the final layout.

The LC-VCO was designed with schematic target in the middle tuning range of a frequency of 2.7 GHz, as shown in Fig. 9, but the frequency has decreased to approx. 2.15 GHz when parasitic effects are taken into account. The extra components that have to be taken into account for this circuit are presented in Table I. The simulation time has also increased by a factor of 3. The phase noise is shown in Fig. 10 for the center frequency of the parasitic extracted netlist. Phase noise at 1 MHz offset from the carrier is -117 dBc/Hz.

VI. METAMODEL GENERATION THROUGH STATISTICAL SAMPLING TECHNIQUES

Metamodeling generation has two distinct steps: generation of data through sampling, and accurate mathematical function fitting. An accurate metamodel can provide a good understanding of the circuit performance characteristics as the design space is traversed. The design development time and circuit generation is minimized given the constraint that

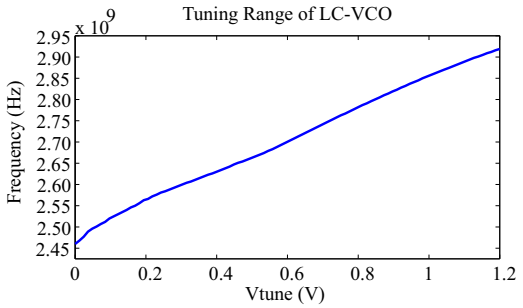


Fig. 9. Frequency tuning characteristic of the LC-VCO.

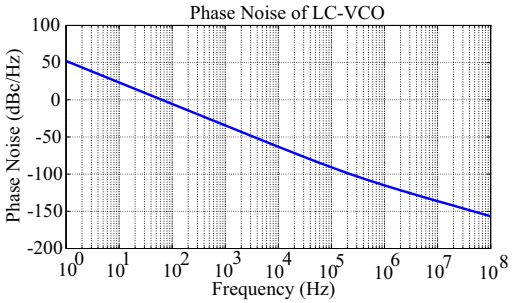


Fig. 10. Phase noise of LC-VCO output at 2.6 GHz.

metamodels should generate accurate results with a small number of samples. Hence the design can be optimized to the needed specifications with an accurate metamodel.

The sampling techniques investigated are divided into three different categories: random, uniform and Design of Experiments (DOE). Many different metamodels can be generated from the sample data. In addition, the choice of the fitting algorithm can have diverse effect on the accuracy of the metamodel. For comparison purposes, all sample data are fitted into polynomial linear regression models of order 4 except the DOE samples which are fitted to order 2 due to the small number of samples. Thus the metamodel for two parameters (W_n for NMOS and W_p for PMOS) has the following form [3], [22]:

$$y = \sum_{i,j=0}^{k} \left(\alpha_{ij} W_n^i W_p^j\right), \tag{4}$$

where y is the response being modeled (frequency in the RO case), W_n and W_p are variables and α_{ij} are the coefficients determined by the polynomial regression. $k =$ varies from 1 to 5 except in the case of DOE where it is fixed at k =2.

Of course, the *actual* response of the circuit is typically unknown as a limited number of samples is available at any point of time. However, the selected test circuits are intentionally simple to allow exhaustive sampling for accurate

capturing of the data for the purpose of research validation. An extremely accurate "golden" response surface with 10,000 sampling points is used for validation and evaluation of the various metamodels. The golden response will be taken as the true circuit response in the following discussion. The actual verification will probably use under 100 sample points in more complex circuits and substantially fewer points for very large circuits. The square Root of Mean Square Error (RMSE) shown in Eqn. 5 is used to compare the prediction values of the metamodel generated using sampling points, to the "true" response. The RMSE estimates the difference between the metamodel and the true model. The smaller the RMSE value, the more accurate the metamodel [3]. As overall accuracy of the metamodel is also of interest, the standard deviation (σ) is calculated for all 10,000 points of the "true" response. This is calculated using the expression shown in Eqn. 6. For a given RMSE a small σ value shows that the metamodel has fewer values deviating from the mean error which otherwise could result in a large error in the constraint area of the metamodel.

$$RMSE=\sqrt{\frac{1}{MN}\sum_{i=1}^{M}\sum_{j=1}^{N}(y(W_{n_i},W_{p_j})-\hat{y}(W_{n_i},W_{p_j}))^2}, \tag{5}$$

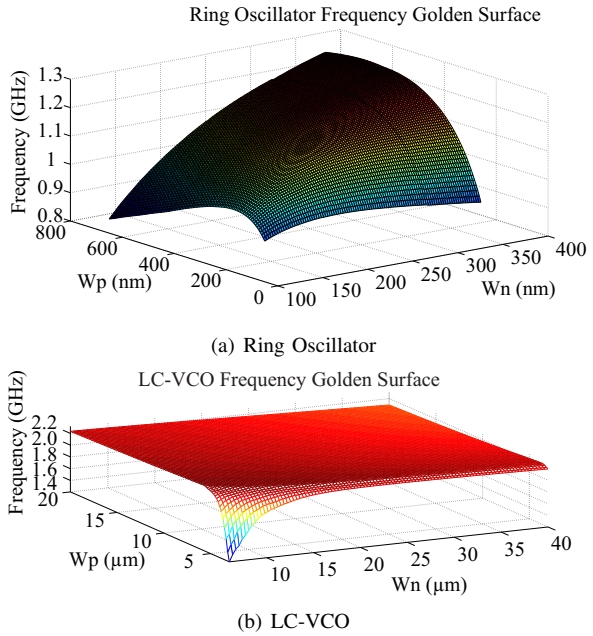
$$\sigma=\sqrt{\frac{1}{MN}\sum_{i=1}^{M}\sum_{j=1}^{N}(|y(W_{n_i},W_{p_j})-\hat{y}(W_{n_i},W_{p_j})|-RMSE)^2}. \tag{6}$$

(MN) =10,000 are randomly distributed points of the W_n and W_p parameters and are selected in the design domain T for metamodel evaluation. These points are checked to ensure that they are not the same points used in the generation of the golden model. This would generate artificially small values of the RMSE. y and $\hat{y}$ are the responses at point W_{n_i}, W_{p_j} of the golden model and the metamodel, respectively.

The generation of the sampling points, SPICE runs and post-processing calculations are done automatically using a combination of commercial and in-house tools.

A. Exhaustive Sampling

If the simulation time is not an issue, exhaustive sampling could be used. With m as the number of variables and n as the number of runs for each variable, the amount of samples required to create a metamodel will be m^n. The RMSE for a large m is very small. In this paper, taking in consideration the width of PMOS and NMOS as variables and running the simulation for these two variables 100 different times each, 10,000 simulation results are obtained for the case study circuits. The RMSE for a metamodel with that number of runs is minimal. Fig. 11(a) and 11(b) show the surfaces of the frequency output on the z-axis with W_n and W_p on the x- and y-axis, respectively. As the calculated RMSE is very small for this metamodel, it is concluded that the generated metamodel's data can be used as the golden model for a comparison for future simulations. Running this many simulations to receive an almost perfect metamodel is usually not practical in the design process. Hence other sampling techniques are explored to minimize the sampling amount for these two variables to generate the best metamodel that fits the design for the given circuit.



(a) Ring Oscillator

(b) LC-VCO

Fig. 11. Exhaustive surfaces for RO and LC-VCO.

B. Random Sampling: Monte Carlo

Monte Carlo or random sampling is a technique which samples the data for each variable by picking n random data points with a given probability distribution with mean at the center of each variable in the design constraint domain T. Fig. 12 shows the results for the creation of multiple metamodels with different numbers of samples and their RMSE results. Note that the RMSE and its standard deviation will both change each time if the simulation is performed with the same number of data points, since the data could have some areas of unsampled points or an over-abundant number of points in one area which is caused by the uneven distribution of sampling points in the domain T.

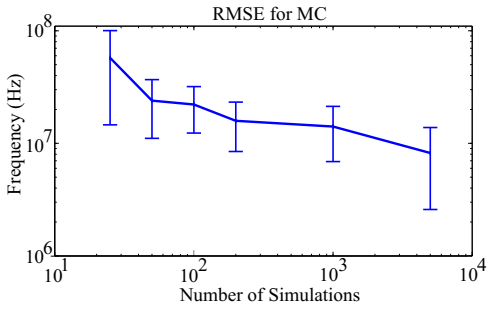


Fig. 12. RMSE data for Monte Carlo sampling of the Ring Oscillator. The error bars have unequal lengths due to the logarithmic scale.

C. Uniform Sampling

Latin Hypercube Sampling (LHS) and Middle Latin Hypercube Sampling (MLHS) techniques are common uniform sampling techniques. There are also many variations which are derived from these two, such as orthogonal array-based LHS, symmetric LHS, orthogonal column LHS, and optimal LHS. Uniform sampling results in more even distribution which usually has a large effect if the number of samples is small. Given that the points are more evenly spaced in the domain T this dispersal of points produces more efficient coverage than random sampling. Uniform sampling techniques can deal with a large number of runs and design parameters. They also are computationally cheap to generate. As shown in the comparative discussion section, on average both LHS and MLHS RMSE results are smaller than simply random sampling technique such as Monte Carlo.

Both LHS and MLHS sampling approaches divide the domain T into n amount of Latin squares, and a data point is then sampled from each square. The drawback for both designs is that the smallest possible variance for the sample mean can never be reached [3].

1) Latin Hypercube Sampling: Latin Hypercube Design produces a random point within the generated n amount of Latin squares on the domain T. This technique provides more evenly distributed sampling points than random sampling techniques, but the samples can still be clustered together as the samples are taken randomly from each Latin square and they can be adjacent to each other. Considering the same number of points as the Monte Carlo generated samples, Fig. 13 shows the RMSE results for LHS metamodels for the RO.

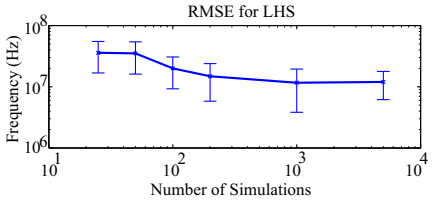


Fig. 13. RMSE data for LHS sampling of the ring oscillator circuit.

2) Middle Latin Hypercube Sampling: The Middle Latin Hypercube Sampling (MLHS) technique is very similar to regular LHS. It divides the domain T into n amount of Latin squares, but instead of randomly sampling from each of those squares, it picks the middle value from each one. This technique is more uniform than the LHS. The main drawback is that it is not able to sample the regions close to the edge of the design space. Considering the same number of points as the Monte Carlo generated samples, Fig. 14 shows the RMSE results for LHS metamodels for RO.

D. Design of Experiments Sampling

Design of Experiments (DOE) is a technique that is used with a large number of variables to profile and generate a predictive function of the model. A three level DOE metamodel was created from 9 points, 3 per axis and their intersection. The metamodel can only be fitted using a 2nd degree polynomial function, instead of the 4th as used in the other examples, due to the small amount of samples. Therefore the RMSE that was calculated for the DOE metamodel is considerably larger in comparison to the other techniques. The RMSE for the RO from the DOE sample was 750 MHz with a standard deviation of 410 MHz. The highest variance for the error was 2.11 GHz^2, while the RMSE for the LC-VCO was 193.4 MHz and the standard deviation was 219.4 MHz. The data from both circuits indicates that DOE is not a competitive sampling technique in terms of accuracy even for a small number of variables.

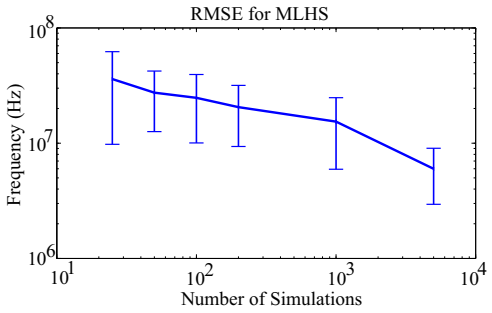


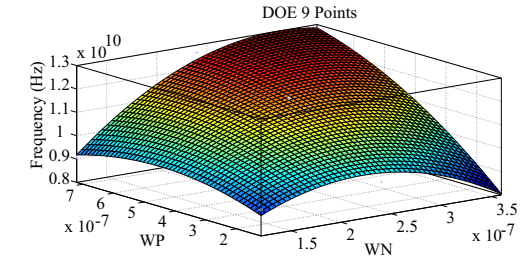
Fig. 14. RMSE data for MLHS sampling of the ring oscillator circuit.

E. Comparative Discussion of Sample Data

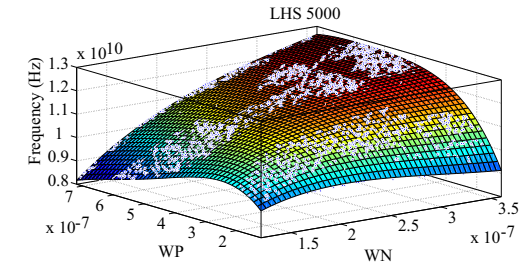
The resulting response surfaces for the four sampling techniques discussed previously are shown in Fig. 15 for the RO and in Fig. 16 for the LC-VCO.

Table III shows a quantitative comparison of the RMSE performance for each method. MC sampling produces higher RMSE than uniform sampling because it is random and might not cover the full spectrum of the design space. It is clear from the data provided in Table III that uniform sampling provides superior accuracy to random sampling. Designers should choose LHS or MLHS over MC but the trend in typical design environments is the opposite. This is probably due to the simplicity of running MC versus LHS or MLHS. Most commercial simulators can perform MC with a simple directive. Uniform sampling, on the other hand, requires extensive setup and if halted it takes extra effort to recover the design. However, the improved accuracy is well worth the extra effort.

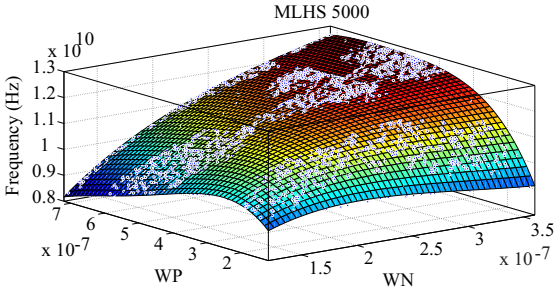
The RMSE (μ) value is slightly higher for few samples in LHS and MLHS vs. MC due to the uneven distribution of points, but as the number of samples increases, the distribution of samples does not have a large effect. Fig. 17 and 18 show the results from multiple simulation runs for MC and LHS techniques in comparison to MLHS. It is shown that the results are very close to each other, within 1% of the output frequency for RO. Based on the average RMSE and standard deviation of errors (σ) data from Table III, it is observed that LHS performed slightly better than MC and MLHS for both circuits. The additional random effect for these two techniques (LHS and MC) provides a slight advantage for a better fitted metamodel than MLHS.



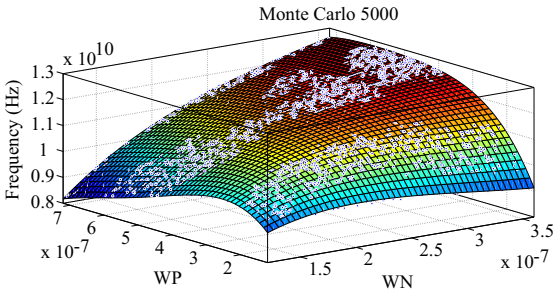
(a) DOE of 9 points



(b) LHS for 5000 points

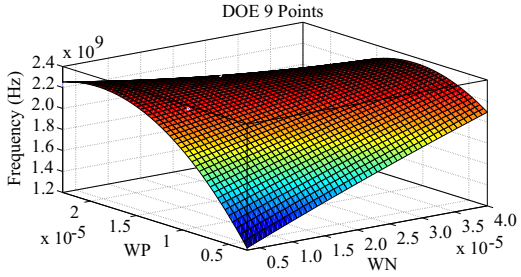


(c) MLHS for 5000 points

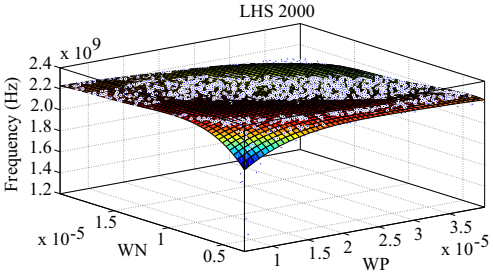


(d) MC for 5000 points

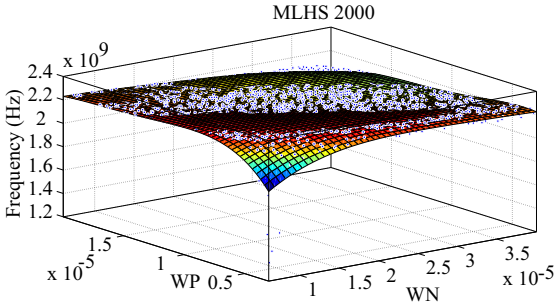
Fig. 15. Sampling of the Ring Oscillator Circuit.



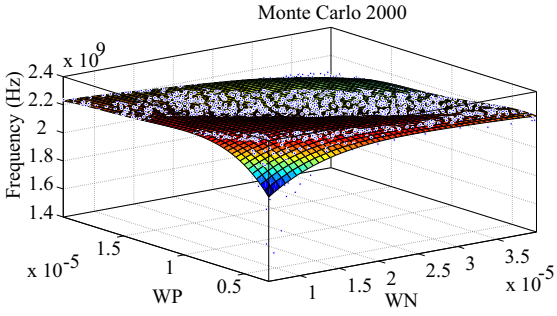
(a) DOE of 9 points



(b) LHS for 2000 points



(c) MLHS for 5000 points



(d) MC for 2000 points

Fig. 16. Sampling of the LC-VCO Circuit.

F. Comparative Discussion of Metamodels

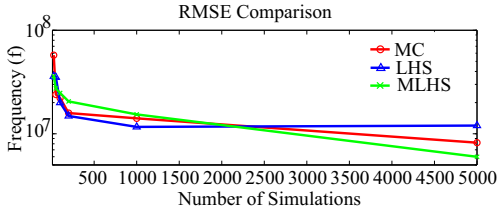
In this section the metamodels obtained as 1st to 5th polynomial order are compared. The sampling technique that was selected for metamodel creation was LHS. This was based on the observation from the previous section for the best performing sampling technique. During the design process it is necessary to allocate time for sampling and verification of the the data to assess how accurate the metamodel is. The exhaustive sampling points which were generated in the previous section were used to verify the accuracy of the metamodel. As an empirical rule of thumb, approx. 30% of the sampled data need to be allocated for verification. Table IV shows the metamodeling generation results for both circuits using an LHS sample of 100 points. The error distribution is also shown to compare the metamodels.

From the data observed in Table IV we can infer that for these two circuits, higher polynomial functions show best results. The generation of metamodels to perform linear regression only takes seconds so we did not provide the generation times.

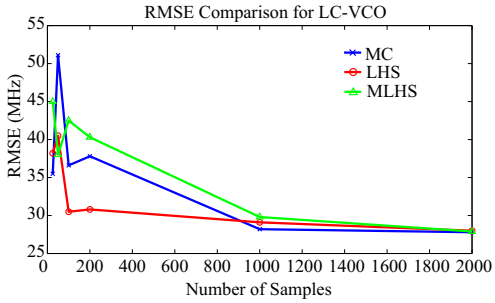
The polynomial metamodel functions are generated for power and frequency for both circuits. The polynomials investigated are from 1st order to 5th order. However, for brevity they are presented for 1st and 2nd order and for the oscillating frequency only in the following:

TABLE III
RMSE COMPARISON FOR DIFFERENT SAMPLING TECHNIQUES

Samples	MC		LHS		MLHS	
Ring Oscillator						
N	μ (MHz)	σ (MHz)	μ (MHz)	σ (MHz)	μ (MHz)	σ (MHz)
25	57.5	42.9	35.6	19.1	36.0	26.2
50	24.0	12.9	35.2	19.1	27.4	14.8
100	22.1	9.7	20.0	10.7	24.8	14.7
200	15.9	7.3	14.9	9.0	20.5	11.2
1000	14.1	7.2	11.7	7.8	15.4	9.4
5000	8.2	5.6	12.0	5.8	5.9	3.0
Average	23.6	14.3	21.6	11.9	21.7	13.2
LC-VCO						
N	μ (MHz)	σ (MHz)	μ (MHz)	σ (MHz)	μ (MHz)	σ (MHz)
25	35.5	33.4	38.2	36.7	45.0	39.7
50	51.1	41.9	40.5	39.9	38.0	31.9
100	36.6	28.9	30.5	29.3	42.5	38.8
200	37.8	32.7	30.8	36.8	40.3	36.2
1000	28.2	25.9	29.1	26.3	29.8	24.8
2000	27.8	25.3	28.0	24.9	27.9	24.6
Average	36.2	31.4	32.9	32.3	37.3	32.7



(a) RMSE comparison for ring oscillator

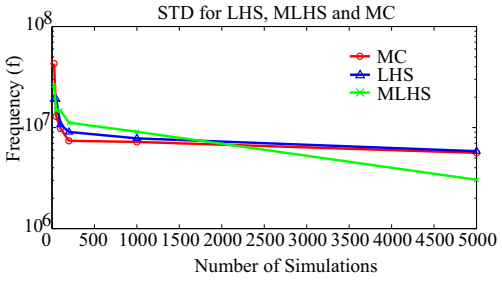


(b) RMSE comparison for LC-VCO

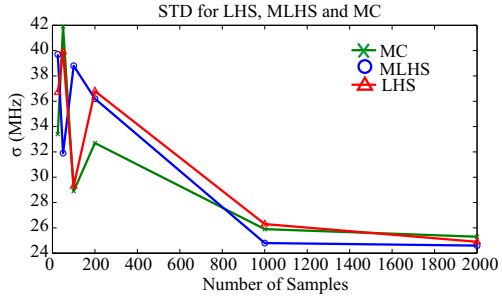
Fig. 17. RMSE comparison of the sampling techniques.

TABLE IV
METAMODEL POLYNOMIAL ORDER COMPARISON

Case Study Circuits	Polynomial Order	μ error (in MHz)	σ error (in MHz)
Ring Oscillator	1	571.0	286.7
	2	195.4	78.1
	3	37.2	18.0
	4	20.0	10.7
	5	17.1	9.6
LC-VCO	1	42.3	40.1
	2	39.4	37.8
	3	35.4	33.9
	4	30.5	29.3
	5	26.5	25.2



(a) STD comparison for ring oscillator



(b) STD comparison for LC-VCO

Fig. 18. STD Comparison of the sampling techniques.

Ring oscillator – Order 1:

$$f(W_n, W_p) = 7.94 \times 10^9 + 1.1 \times 10^{16} W_n + 1.28 \times 10^{15} W_p. \quad (7)$$

Ring oscillator – Order 2:

$$f(W_n, W_p) = 6.38 \times 10^9 + 2.2 \times 10^{16} W_n + 6.1 \times 10^{15} W_p - 5.03 \times 10^{22} W_n^2 + 3.28 \times 10^{22} W_n W_p - 1.52 \times 10^{22} W_p^2. \quad (8)$$

LC-VCO – Order 1:

$$f(W_n, W_p) = 2.38 \times 10^9 - 3.49 \times 10^{12} W_n - 6.66 \times 10^{12} W_p. \quad (9)$$

LC-VCO – Order 2:

$$f(W_n, W_p) = 2.3 \times 10^9 + 6.25 \times 10^{11} W_n + 1.45 \times 10^{11} W_p - 4.16 \times 10^{16} W_n^2 - 2.01 \times 10^{17} W_n W_p - 1.02 \times 10^{17} W_p^2. \quad (10)$$

This paper only considers polynomial functions for the metamodel. Once the sample data are generated, there can be many other forms of functions that can be used for fitting, such as exponential functions, logarithmic functions, trigonometric functions, power functions, Gaussian function, and Lorentzian curves. Since the target of this paper is sampling, they are not covered here. The metamodels will be used for fast design optimization and verification of complex circuits. It is observed that the optimization over metamodels can have significant speed-up over the actual circuit netlists [23].

VII. CONCLUSIONS AND FUTURE RESEARCH

In this paper, a novel design flow using metamodels is introduced. The most important aspect of the flow, the creation of a metamodel using statistical sampling is thoroughly

presented. A comparison is presented for commonly used sampling techniques using a nano-CMOS ring oscillator in 45 nm technology and an LC-VCO in 180 nm technologies as case studies. The presented design flow can be used to speed up the design process of nanoscale circuits in general. The frequencies of the RO and LC-VCO were used as objective functions for target specifications. It was shown that the parasitic effects play a major role in the circuit's response. A thorough analysis for various sampling data rates and methods demonstrates that uniform sampling techniques have better overall performance (in terms of accuracy) than the randomized and DOE sampling techniques. Whether LHS or MLHS is more appropriate for a particular design depends on whether edge effects are important or not. It is observed that LHS is typically preferable over MLHS because it covers the design space uniformly, while, at the same time, providing for a small amount of randomness in the samples. Also LHS has a chance to cover the edges of the design space while MLHS does not. It is worthy to note that during this study it is shown that both sampling techniques and metamodeling generation are technology independent. The second part of the study concentrated on how to select a more accurate metamodel using already sampled data. For two different circuits, it was determined that higher order polynomials provide better overall fit and smaller mean error and error distribution.

Our future research will include specific optimization techniques as part of the proposed design flow. Future research will also involve analysis of other functional forms for metamodeling. Extensive study of metamodeling-based optimization for a large number of design variables for more complex nano-CMOS circuits will be performed. Process-Voltage-Temperature (PVT) variation analysis and mitigation during the design process using metamodels will be also investigated.

ACKNOWLEDGMENTS

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