

# DOE-ILP Based Simultaneous Power and Read Stability Optimization in Nano-CMOS SRAM

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## Abstract

This paper presents a novel design flow and algorithms for simultaneous power-stability optimization of nano-CMOS static random access memory (SRAM) circuits. A  $45nm$  single-ended seven transistor SRAM has been used as case study. The SRAM cell is subjected to a dual- $V_{Th}$  assignment based on a novel combined Design of Experiments and Integer Linear Programming (DOE-ILP) approach, resulting in 50.6% power reduction (including leakage) and 43.9% increase in the read static noise margin over the baseline design. The process variation analysis of the optimized cell is performed considering the variability effect in twelve device parameters. An  $8 \times 8$  array is constructed to show the feasibility of the proposed SRAM cell. To the best of the authors' knowledge, this is the first research reporting the use of DOE and ILP for optimization of conflicting targets of power and stability in SRAM.

## Index Terms

Nanoscale CMOS, Low-Power Design, Power Optimization, Static Random Access Memory (SRAM), Static Noise Margin (SNM)

## I. INTRODUCTION AND CONTRIBUTIONS

A major part of systems-on-chip (SoC) is the memory subsystem. A typical state-of-the-art microprocessor die has a large portion devoted to on-chip memory [1]. High-performance, large-capacity SRAM is a crucial component in the memory hierarchy of modern digital systems. SRAM design requires balancing delay, area, and power dissipation. Memory accesses consume a substantial portion of the total power budget for many applications. Reducing power dissipation in SRAMs significantly improves power efficiency, reliability, and cost.

SRAM stability has also become a major concern for nano-CMOS. It has become increasingly challenging to maintain an acceptable Static Noise Margin (SNM) in embedded SRAMs while scaling minimum feature sizes and supply voltages. SNM becomes worse during the read operation (read SNM) compared to the hold operation [2]. Thus, there is a pressing requirement to design SRAM where the read operation does not disturb the cell stability. The read SNM can serve as a figure of merit in stability evaluation of SRAM cells [3]. Process variation is a major concern at nanoscale CMOS technologies. Variations in device parameters translate into variations in SRAM circuit parameters, such as power and stability, which eventually lead to loss in parametric yield. Any asymmetry in the cells due to process variations makes them less stable. Under adverse operating conditions such cells may inadvertently flip and corrupt the data.

The *novel contributions* of this paper are:

- 1) A novel design flow for power and stability optimization in nanoscale CMOS SRAM is proposed.
- 2) A  $45nm$  SRAM cell is subjected to the proposed methodology.
- 3) For simultaneous power and stability optimization of the SRAM, a novel combined Design of Experiments (DOE) - Integer Linear Programming (ILP) based algorithm is proposed that selects transistors for dual- $V_{Th}$  assignment.
- 4) Process variation analysis of the SRAM cell is presented to study the effect of twelve process parameters on its power and stability.
- 5) An  $8 \times 8$  SRAM array is constructed and characterized using the power and stability optimized SRAM cell, to demonstrate its feasibility.

The paper is organized as follows: Current related research is presented in section II. Section III discusses the proposed optimized design flow. The baseline design is discussed in section IV. Section V highlights the combined DOE-ILP simultaneous power and read stability optimization. Section VI studies the effect of variability in device parameters on the proposed SRAM cell stability and power, followed by conclusions and future research in section VII.

## II. PRIOR RESEARCH IN SRAM DESIGN

A nine transistor SRAM cell with enhanced stability and reduced power is proposed in [2], [4]. A Schmitt-trigger based SRAM proposed in [5], providing better read stability and better write ability. A ten transistor, low-voltage SRAM cell with faster readout operation is proposed in [6]. A subthreshold approach has been used in [7]. The methodology in [8] analyzes the stability of an SRAM cell in the presence of random fluctuations in device parameters. [9], [10], [11], gives a method based on dual- $V_{Th}$  and dual- $T_{ox}$  assignment for low power while maintaining performance. A comparison of our research with existing literature is presented in Table I. It can be observed that we attain high stability and low power.

The current archival journal paper is based on our shorter conference paper [14] and is expanding that work as follows:

- 1) A tabular comparison with existing literature is given in Table I to highlight the significance of our research.
- 2) The optimization methodologies are discussed in more detail in section III.
- 3) The Design of Experiments (DOE) part of the optimization is described in detail in section V, showing how the coefficients (half-effects) for the ILP models are obtained.

TABLE I  
COMPARATIVE PERSPECTIVE WITH RELATED PRIOR RESEARCH

| Research          | Power            | SNM     | Optimization Approach                              |
|-------------------|------------------|---------|--|
| Liu [2]           | 31.9nW (leakage) | 0.3V    | Separate data access mechanism.                    |
| Kulkarni [5]      | 0.11 $\mu$ W     | 300mV   | Schmitt Trigger.                                   |
| Okumura [6]       | –                | 0.36V   | Column line assist scheme.                         |
| Agrawal [8]       | –                | 150mV   | Modeling based approach.                           |
| Singh [12]        | 11.53 $\mu$ W    | 305mV   | Transmission gates are used as access transistors. |
| Liu [13]          | 12.5nW           | 222mV   | Dynamic threshold voltage tuning.                  |
| <b>This Paper</b> | 113.6nW          | 303.3mV | Combined DOE-ILP optimization.                     |

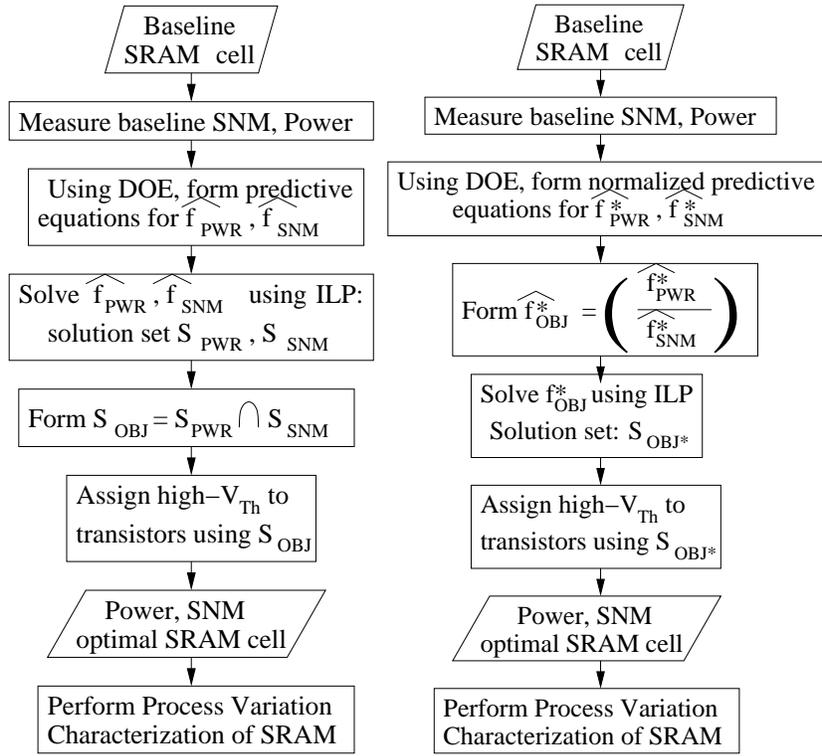
- 4) Pareto plots for the half-effects of transistors are presented.
- 5) Monte Carlo simulation results of power and SNM, and butterfly curves under process variation for approaches involving power minimization only ( $S_{PWR}$ ) and SNM maximization only ( $S_{SNM}$ ) are presented.

### III. PROPOSED DESIGN METHODOLOGY FOR POWER AND STABILITY OPTIMAL NANO-CMOS SRAM DESIGN

Fig. 1 shows the two approaches investigated in this paper. The input to each flow is a baseline cell, with minimum sized transistors.

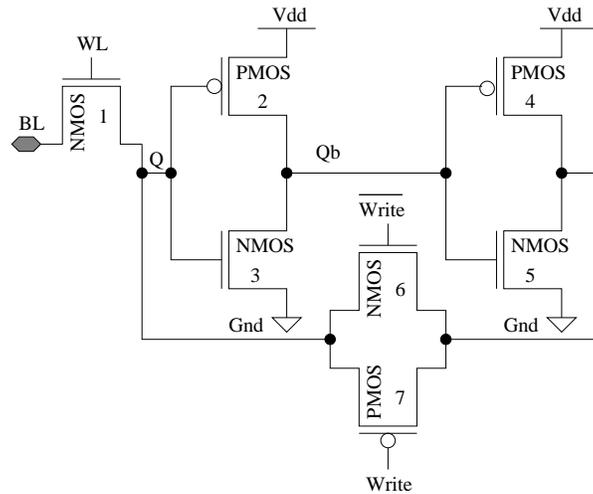
The figures of merit under consideration (power and SNM) are measured for the baseline design. The average power consumption and read SNM are considered in this paper. To reduce dissipation we propose a well-established process-level technique, dual threshold voltage. For the 45nm node, leakage is the major component of total power dissipation [16]. Its reduction through dual- $V_{Th}$  reduces total power.

In approach 1 (Fig. 1(a)), predictive equations are formulated for power ( $\widehat{f_{PWR}}$ ), and SNM ( $\widehat{f_{SNM}}$ ). These equations, and the constraints are linear and each of the solution variables is restricted to be either 0 or 1. The linear objective function is optimized subjected to linear equality and linear inequality constraints. Thus, ILP is an optimal way to solve these predictive equations. The solution set for power minimization is called  $S_{PWR}$ , and the solution set for SNM maximization is called  $S_{SNM}$ . The overall objective set  $S_{OBJ}$  is formulated as  $S_{PWR} \cap S_{SNM}$  ( $\cap$  refers to the intersection of sets), where the transistors suitable for high and nominal  $V_{Th}$  assignment are identified. Using the optimal configuration



(a) Optimization Flow - 1

(b) Optimization Flow - 2



(c) Topology of a 7-transistor SRAM cell

Fig. 1. Proposed design flow for simultaneous power and stability optimization of Nano-CMOS SRAM. A single-ended seven transistor cell [15]; load transistors - (2, 4), driver transistors - (3, 5), and access transistors - (1, 6 and 7).

the design is re-simulated. For nanoCMOS SRAM it is important to perform well under process variations, thus the statical variability is studied for twelve important parameters.

In approach 2 (Fig. 1(b)), the normalized predictive equations for power ( $\widehat{f_{PWR^*}}$ ), and SNM ( $\widehat{f_{SNM^*}}$ ) are used. The objective function:  $\widehat{f_{OBJ^*}}$  is formed as the ratio of  $\widehat{f_{PWR^*}}$  and  $\widehat{f_{SNM^*}}$ .  $\widehat{f_{OBJ^*}}$  is to be minimized using ILP, and leads to simultaneous power minimization (numerator) and SNM maximization (denominator). The solution set is called  $S_{OBJ}$ , where the transistors suitable for high and nominal  $V_{Th}$  assignment for achieving the objective are identified. The design is then re-simulated with this configuration. The statical variability is studied subjected to twelve parameters.

A seven transistor (7T) cell topology which is suitable for ultra-low voltage regimes and is tolerant to read failure is selected [15] as a case study. However, the proposed methodologies are also to other variants present in literature.

#### IV. DESIGN AND SIMULATION OF A 45nm CMOS 7T SRAM

##### A. Cell Design

Single-ended SRAMs are known for their low-power potential. The baseline cell is shown in Fig. 1(c) with initial ( $W/L$ ) sizes. The cell is composed of a read and write access transistor (1), two cross-coupled inverters (transistors 2, 3, 4 and 5) and a transmission gate (transistors 6 and 7) which opens the feedback connection during the write operation. The cell operates on a single bit-line, instead of having two bit-lines as in standard six transistor cell. Both read and write are performed over the single bit-line. However, the word-line (WL) must be asserted high prior to write and read, as in the standard six transistor cell. When the cell is in hold mode, the WL is low and a strong feedback is provided to the cross-coupled inverters by the transmission gate. The power consumption ( $\tau_{PWR}$ ) and SNM ( $\tau_{SNM}$ ) of the baseline design are presented in Table II.  $\tau_{PWR}$  and  $\tau_{SNM}$  represent these values, because they are used as constraints in the optimization methodology.

##### B. Power and Leakage Simulation and Measurement

The total power of the circuit is defined as the summation of dynamic power, subthreshold leakage, and gate-oxide leakage. SRAM cells have a tendency to retain data for some duration of time as they cannot be shut off. So, minimizing leakage becomes a critical issue [7]. The total power is quantified as follows:

$$P_{total} = P_{dyn} + P_{sub} + P_{gate}, \quad (1)$$

where  $P_{dyn}$  is the dynamic power,  $P_{sub}$  is the subthreshold leakage, and  $P_{gate}$  is the gate-oxide leakage.

The current flow, which is manifested in leakage and power dissipation, in each device depends of the location the device and the operation. For accurate measurement of current (power) it is important that the currents are identified. Fig. 2 shows the paths for read and write operations. The dashed arrows are gate-oxide leakage, and subthreshold leakage is represented by dotted arrows. Solid arrows identify the dynamic current which flows when the transistor is ON. When the transistor is ON, it dissipates dynamic power along with the gate-oxide leakage [17]. When the transistor is OFF, it has gate-oxide leakage and subthreshold leakage.

Current paths for write “1”, read “1”, write “0” and read “0” are shown in figures 2(a), 2(b), 2(c) and 2(d), respectively.

### C. Read Static Noise Margin (SNM) Simulation and Measurement

SNM is defined as the maximum amount of noise that can be tolerated at the cell nodes just before flipping the states.

A simulation based approach is used to measure SNM (Fig. 3(a)). Two DC voltage noise sources  $V_N$  are placed in adverse direction to the input of each inverter of the cell to obtain the worst-case SNM. The sources are swept from 0 to  $V_{dd}$  until the cell voltages flip. A common graphical representation of SNM called butterfly curve is used during read access [10]. The SNM is defined as the length of the side of the largest square that can be embedded inside the lobes of the butterfly curve [3].

The power and SNM results are presented in Table II.

TABLE II  
POWER AND SNM RESULTS FOR THE BASELINE SRAM

| Parameters   | Estimated Values |
|--------------|------------------|
| $\tau_{PWR}$ | 203.6 nW         |
| $\tau_{SNM}$ | 170 mV           |

## V. COMBINED DOE-ILP OPTIMIZATION ALGORITHMS

This section discusses the combined Design of Experiments (DOE)-Integer Linear Programming (ILP) algorithms. According to Algorithm 1, the baseline cell is taken as input along with the nominal and high  $V_{Th}$  model files. Experimental analysis is then performed for the transistors of the cell using a 2-Level

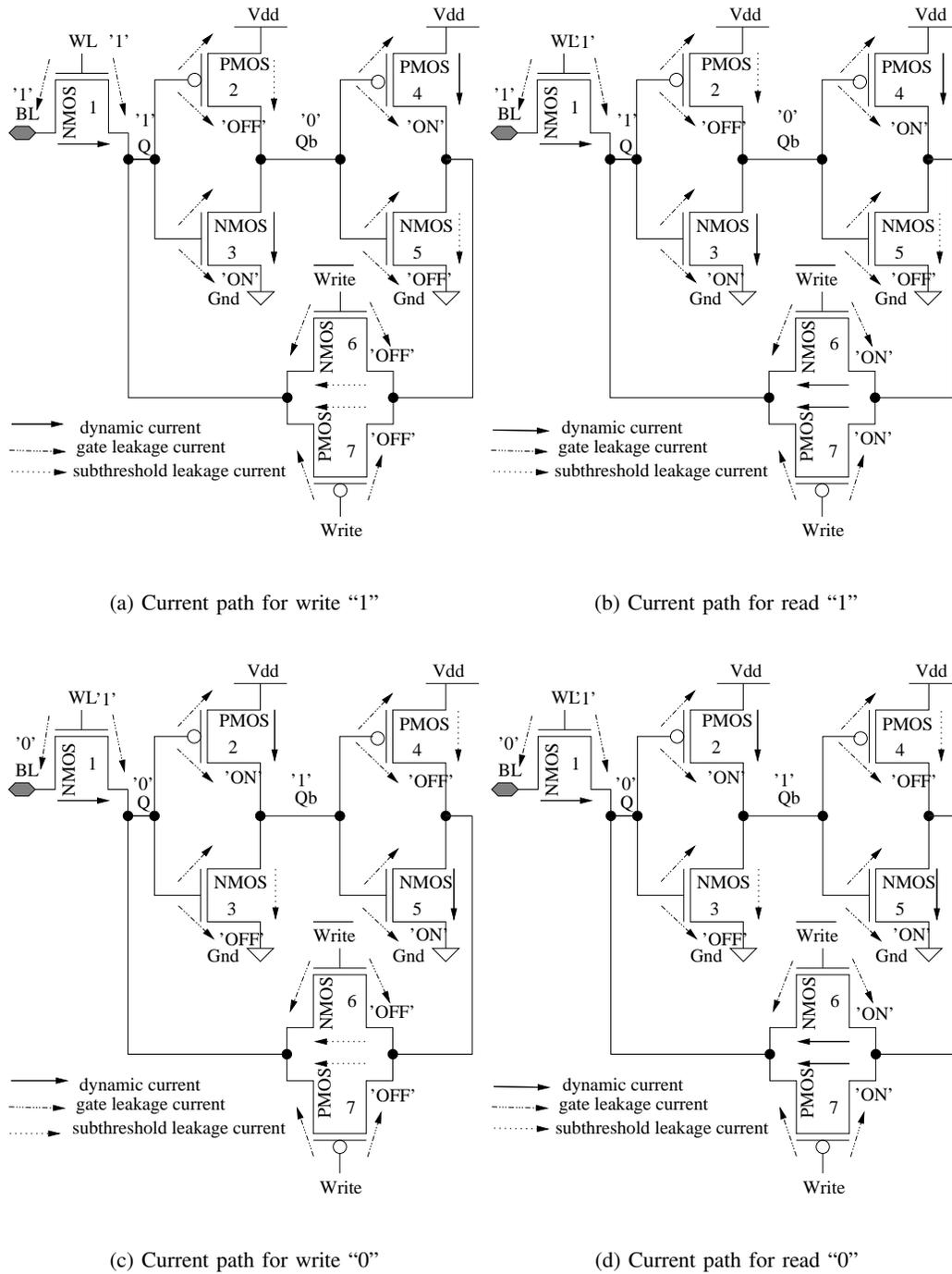


Fig. 2. Current paths for the 7T SRAM cell during different read and write operations.

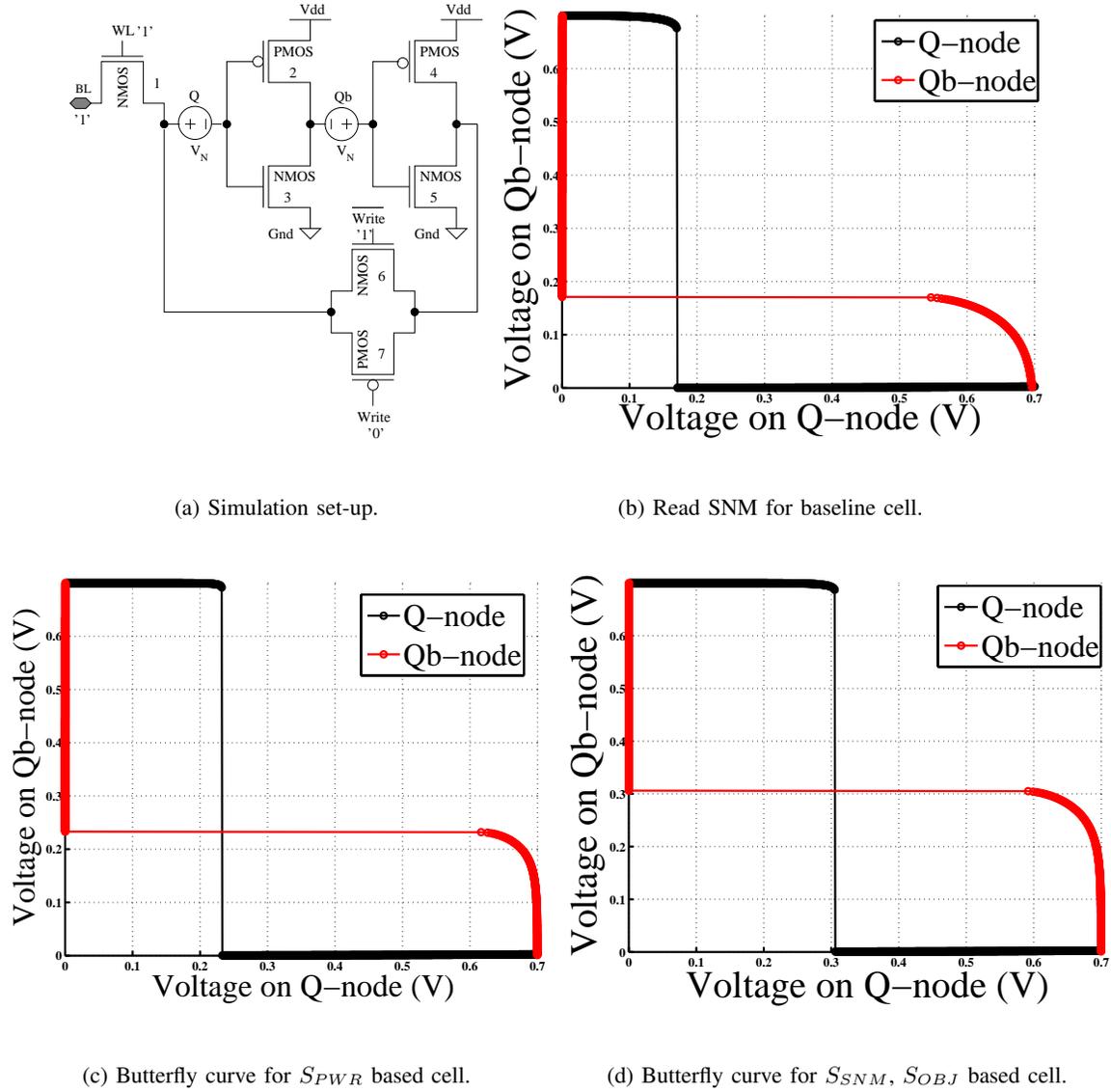


Fig. 3. Read SNM measurement in different configurations of SRAM cells.

Taguchi L8 array. The input factors are the 7 transistor  $V_{Th}$  states, and the responses are the average power consumption ( $\widehat{f_{PWR}}$ ) and SNM ( $\widehat{f_{SNM}}$ ) of the cell. Each factor can take a high  $V_{Th}$  (1) or a nominal  $V_{Th}$  (0) state. Simulations are run for each experiment of the array and the values for both PWR and SNM are recorded. Then, the linear predictive equations are formulated.

In Algorithm 2, the steps are the same as in algorithm 1. Here, however, the normalized (unitless) equations are formed for power ( $\widehat{f_{PWR}^*}$ ) and SNM ( $\widehat{f_{SNM}^*}$ ).

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**Algorithm 1** Approach 1 for simultaneous power and read stability optimization
 

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- 1: **Input:** Baseline PWR and SNM of the cell, Nominal and High  $V_{Th}$  model files.
  - 2: **Output:** Optimized objective set  $S_{OBJ} = [f_{PWR}, f_{SNM}]$  cell with transistors identified for high  $V_{Th}$  assignment.
  - 3: Setup experiment using L8 array, where the factors are  $V_{Th}$  states, and the responses are average power consumption ( $f_{PWR}$ ) and read SNM ( $f_{SNM}$ ).
  - 4: **for** Each 1:8 experiments of L8 array **do**
  - 5:     Run simulations.
  - 6:     Record PWR and SNM.
  - 7: **end for**
  - 8: Form linear predictive equations:  $\widehat{f_{PWR}}$  for power,  $\widehat{f_{SNM}}$  for SNM.
  - 9: Solve  $\widehat{f_{PWR}}$  using ILP. Solution set:  $S_{PWR}$ .
  - 10: Solve  $\widehat{f_{SNM}}$  using ILP. Solution set:  $S_{SNM}$ .
  - 11: Form  $S_{OBJ} = S_{PWR} \cap S_{SNM}$  (intersection of  $S_{PWR}$  and  $S_{SNM}$ ).
  - 12: Assign high  $V_{Th}$  based on  $S_{OBJ}$ .
  - 13: Re-simulate SRAM cell to obtain power and SNM.
- 

The half-effects are given by:

$$\frac{\Delta(n)}{2} = \left( \frac{avg(1) - avg(0)}{2} \right), \quad (2)$$

where  $\left[ \frac{\Delta(n)}{2} \right]$  is the half-effect of  $n$ th transistor,  $avg(1)$  is the average value of power when transistor  $n$  is in high- $V_{Th}$  state, and  $avg(0)$  is the average value of power when transistor  $n$  is in nominal  $V_{Th}$  state. Figs. 4(a) and 4(b) show the pareto plots of the half-effects of the transistors for  $\widehat{f_{PWR}}$  and  $\widehat{f_{SNM}}$ , respectively. Predictive equations are then obtained as follows:

$$\hat{f} = \bar{f} + \sum_{n=1}^7 \left( \frac{\Delta(n)}{2} \times x_n \right), \quad (3)$$

where  $\hat{f}$  is the response,  $\bar{f}$  is the average,  $\left[ \frac{\Delta(n)}{2} \right]$  is the half effect of the  $n$ th transistor, and  $x_n$  is the  $V_{Th}$  state of the  $n$ th transistor.

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**Algorithm 2** Approach 2 for simultaneous power and read stability optimization
 

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- 1: **Input:** Baseline PWR and SNM of the cell, Nominal and High  $V_{Th}$  model files.
  - 2: **Output:** Optimized objective set  $S_{OBJ} = [f_{PWR}, f_{SNM}]$  cell with transistors identified for high  $V_{Th}$  assignment.
  - 3: Setup experiment using L8 array, where the factors are  $V_{Th}$  states, and the responses are average power consumption ( $f_{PWR}$ ) and read SNM ( $f_{SNM}$ ).
  - 4: **for** Each 1:8 experiments of L8 array **do**
  - 5:     Run simulations.
  - 6:     Record PWR and SNM.
  - 7: **end for**
  - 8: Form normalized predictive equations:  $\widehat{f_{PWR}^*}$  for power,  $\widehat{f_{SNM}^*}$  for SNM.
  - 9: Form  $\widehat{f_{OBJ}^*} = \frac{\widehat{f_{PWR}^*}}{\widehat{f_{SNM}^*}}$ .
  - 10: Solve  $\widehat{f_{OBJ}^*}$  using ILP. Solution set:  $S_{OBJ}$ .
  - 11: Assign high  $V_{Th}$  to transistors based on  $S_{OBJ}$ .
  - 12: Re-simulate SRAM cell to obtain power and SNM.
- 

**A. Solution for power minimization:  $S_{PWR}$** 

The predictive equation for average power consumption is:

$$\begin{aligned}
 \widehat{f_{PWR}}(nW) &= 118.2075 - 5.975 \times x_1 - 28.955 \times x_2 \\
 &\quad - 23.1625 \times x_3 - 10.995 \times x_4 - 10.6375 \times x_5 \\
 &\quad - 12.1425 \times x_6 + 6.475 \times x_7.
 \end{aligned} \tag{4}$$

Where,  $x_i$  represents the  $V_{Th}$  of transistor  $i$  (Fig. 1(c)). The ILP formulation is:

$$\begin{aligned}
 \min \quad & \widehat{f_{PWR}} \\
 \text{s.t.} \quad & 0 \leq x_1 \leq 1, 0 \leq x_2 \leq 1, 0 \leq x_3 \leq 1, 0 \leq x_4 \leq 1, \\
 & 0 \leq x_5 \leq 1, 0 \leq x_6 \leq 1, 0 \leq x_7 \leq 1, f_{SNM} > \tau_{SNM}.
 \end{aligned}$$

where the constraints ‘1’ and ‘0’ represent coded values for high  $V_{Th}$  and nominal  $V_{Th}$  states and  $\tau_{SNM}$  is the SNM of the baseline design. The optimal solution is:  $S_{PWR} = [x_1 = 1, x_2 = 1, x_3 = 1, x_4 = 1, x_5 = 1, x_6 = 1, x_7 = 0]$ . Fig. 5(a) shows the configuration for minimum power consumption, with the high  $V_{Th}$  transistors circled. The power consumption is 26.34 nW with an SNM of 231.9 mV (Table III). Fig. 3(c) shows the butterfly curve obtained.

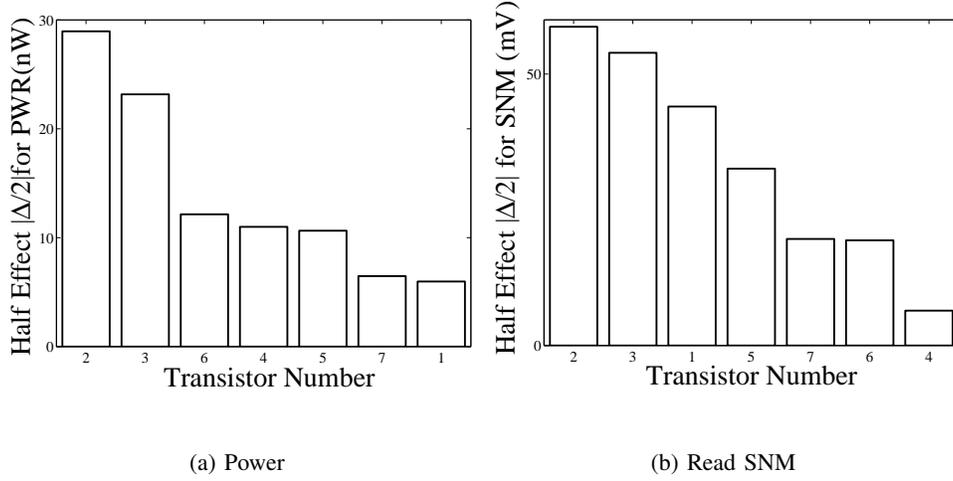


Fig. 4. Pareto plot for power and SNM of the SRAM cell.

### B. Solution for SNM maximization: $S_{SNM}$

The predictive equation for the read SNM is:

$$\begin{aligned}
 \widehat{f_{SNM}}(mV) &= 156.675 - 44.025 \times x_1 + 58.725 \times x_2 \\
 &- 53.925 \times x_3 - 6.425 \times x_4 + 32.575 \times x_5 \\
 &+ 19.375 \times x_6 - 19.625 \times x_7,
 \end{aligned} \tag{5}$$

The ILP formulation is:

$$\begin{aligned}
 \max \quad & \widehat{f_{SNM}} \\
 \text{s.t.} \quad & 0 \leq x_1 \leq 1, 0 \leq x_2 \leq 1, 0 \leq x_3 \leq 1, 0 \leq x_4 \leq 1, \\
 & 0 \leq x_5 \leq 1, 0 \leq x_6 \leq 1, 0 \leq x_7 \leq 1, f_{PWR} < \tau_{PWR}.
 \end{aligned}$$

where  $\tau_{PWR}$  is the power consumption of the baseline design. The optimal solution is obtained as follows:  $S_{SNM} = [x_1 = 0, x_2 = 1, x_3 = 0, x_4 = 0, x_5 = 1, x_6 = 1, x_7 = 0]$ . Fig. 5(b) shows the SRAM configuration for  $S_{SNM}$ , with the high  $V_{Th}$  transistors circled. The power consumption is 113.6 nW with an SNM of 303.3 mV (Table III). Fig. 3(d) shows the butterfly curve.

### C. Solution for power minimization and SNM maximization: $S_{OBJ}$

1) *Approach 1:* The overall objective set  $S_{OBJ}$  for simultaneous optimization of power and SNM is to achieve low power and high stability. Hence a solution between  $S_{PWR}$  and  $S_{SNM}$  is explored. In

approach 1, the following solution set is formed:

$$S_{OBJ} = S_{PWR} \cap S_{SNM}, \quad (6)$$

where  $\cap$  is the intersection of two solution sets  $S_{PWR}$  and  $S_{SNM}$ . Equation 6 is derived for the set domain where the AND operation in the logic domain translates to intersection in the set domain. The constraints are same as the individual ILP formulations. The ILP solver results in the following solution:  $S_{OBJ} = [x_1 = 0, x_2 = 1, x_3 = 0, x_4 = 0, x_5 = 1, x_6 = 1, x_7 = 0]$ . Fig. 5(c) shows the configuration for approach 1, with the high  $V_{Th}$  transistors circled. The power consumption is 113.6 nW with an SNM of 303.3 mV (Table III). Fig. 3(d) shows the butterfly curve.

2) *Approach 2*: The normalized forms of  $\widehat{f_{PWR}}$  and  $\widehat{f_{SNM}}$  are used, denoting them as  $\widehat{f_{PWR}^*}$  and  $\widehat{f_{SNM}^*}$ . These equations have been normalized by division of each value of the data by the maximum value of data. The following normalized predictive equations are obtained:

$$\begin{aligned} \widehat{f_{PWR}^*} &= 0.58 - 0.03 \times x_1 - 0.14 \times x_2 \\ &- 0.11 \times x_3 - 0.05 \times x_4 - 0.05 \times x_5 \\ &- 0.06 \times x_6 + 0.03 \times x_7, \end{aligned} \quad (7)$$

and

$$\begin{aligned} \widehat{f_{SNM}^*} &= 0.52 - 0.15 \times x_1 + 0.19 \times x_2 \\ &- 0.18 \times x_3 - 0.02 \times x_4 + 0.11 \times x_5 \\ &+ 0.06 \times x_6 - 0.06 \times x_7, \end{aligned} \quad (8)$$

The objective function is:

$$\begin{aligned} \widehat{f_{OBJ}^*} &= \frac{\widehat{f_{PWR}^*}}{\widehat{f_{SNM}^*}}, \\ &= 0.18 \times x_3 - 0.02 \times x_4 + 0.11 \times x_5 \\ &+ 0.06 \times x_6 - 0.06 \times x_7, \end{aligned} \quad (9)$$

The aim is to minimize  $\widehat{f_{OBJ}^*}$ , where the numerator ( $\widehat{f_{PWR}^*}$ ) would be minimized, and the denominator ( $\widehat{f_{SNM}^*}$ ) would be maximized. The ILP formulation is:

$$\begin{aligned} \min \quad & \widehat{f_{OBJ}^*} \\ \text{s.t.} \quad & 0 \leq x_1 \leq 1, 0 \leq x_2 \leq 1, 0 \leq x_3 \leq 1, 0 \leq x_4 \leq 1, \\ & 0 \leq x_5 \leq 1, 0 \leq x_6 \leq 1, 0 \leq x_7 \leq 1, \\ & f_{PWR} < \tau_{PWR}, f_{SNM} > \tau_{SNM}. \end{aligned}$$

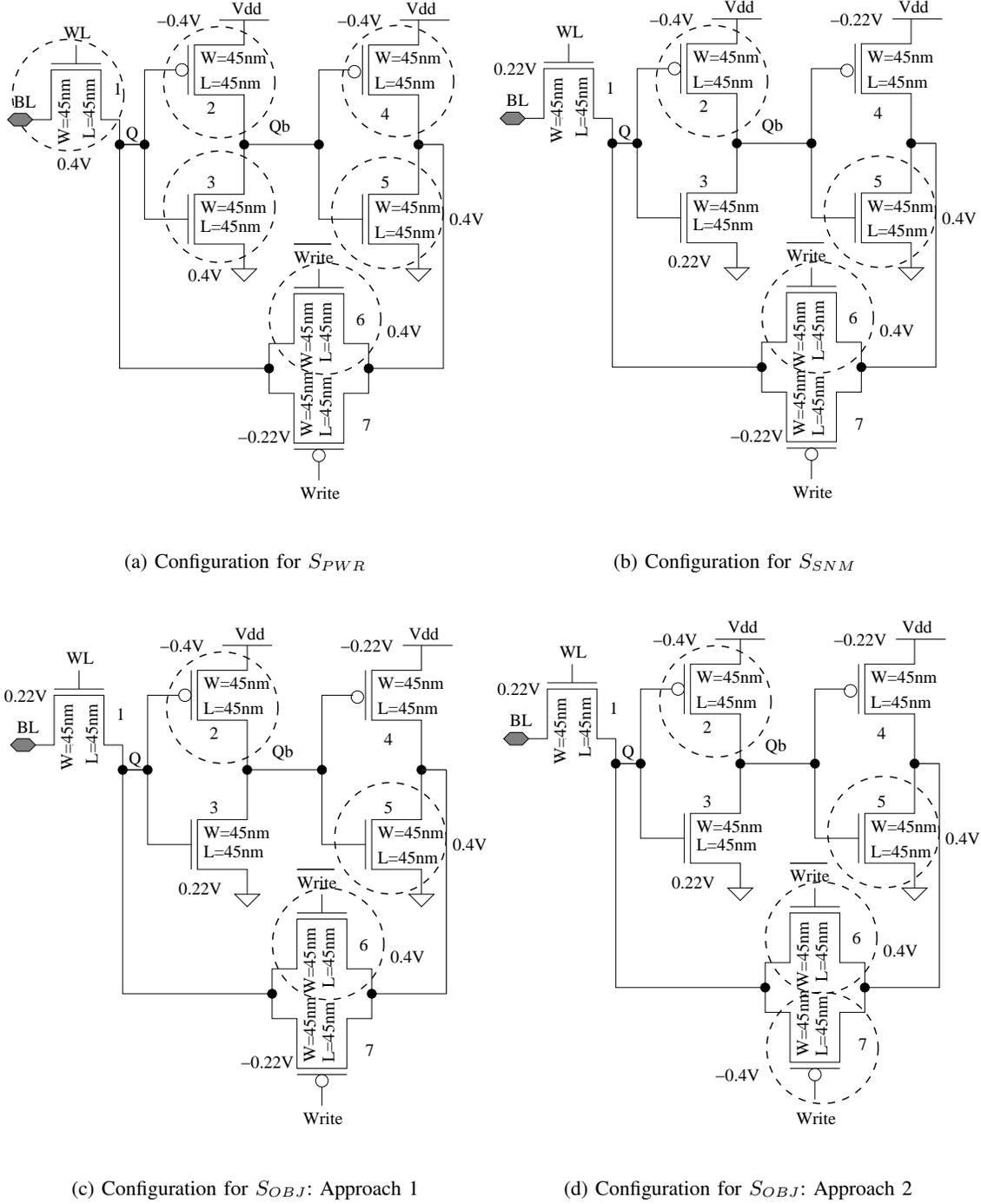


Fig. 5. Dual  $V_{Th}$  configurations of 7T SRAM cell according to  $S_{PWR}$ ,  $S_{SNM}$  and  $S_{OBJ}$  with their threshold voltages marked on the side. The high  $V_{Th}$  ( $V_{Thn} = 0.4V$ ,  $V_{Thp} = -0.4V$ ) transistors are circled and the remaining transistors are nominal  $V_{Th}$  ( $V_{Thn} = 0.22V$ ,  $V_{Thp} = -0.22V$ ).

Solving the ILP problem, the optimal solution is:  $S_{OBJ} = [x_1 = 0, x_2 = 1, x_3 = 0, x_4 = 0, x_5 = 1, x_6 = 1, x_7 = 1]$ . Figure 5(d) shows the configuration for approach 2, with the high  $V_{Th}$  transistors circled. The power consumption is  $100.5 \text{ nW}$  with an SNM of  $303.3 \text{ mV}$  (Table III). Fig. 3(d) shows the butterfly curve.

TABLE III  
OPTIMIZATION RESULTS FOR DIFFERENT OBJECTIVES

| Optimization            | Parameter  | Value              | Change         |
|-------------------------|------------|--------------------|----------------|
| $S_{PWR}$               | $P_{SRAM}$ | $26.34 \text{ nW}$ | 87.1% decrease |
|                         | SNM        | $231.9 \text{ mV}$ | 26.7% increase |
| $S_{SNM}$               | $P_{SRAM}$ | $113.6 \text{ nW}$ | 44.2% decrease |
|                         | SNM        | $303.3 \text{ mV}$ | 43.9% increase |
| $S_{OBJ}$<br>Approach 1 | $P_{SRAM}$ | $113.6 \text{ nW}$ | 44.2% decrease |
|                         | SNM        | $303.3 \text{ mV}$ | 43.9% increase |
| $S_{OBJ}$<br>Approach 2 | $P_{SRAM}$ | $100.5 \text{ nW}$ | 50.6% decrease |
|                         | SNM        | $303.3 \text{ mV}$ | 43.9% increase |

Fig. 6 shows the comparison of baseline and optimized cell power and read SNM for various values of  $V_{dd}$ . Both power and SNM increase with supply voltage. For  $V_{dd} = 0.7V$  the power dissipation is reduced by 44.2% and SNM has increased by 43.9% using approach 1, and the power dissipation is reduced by 50.6% and SNM is increased by 43.9% using approach 2.

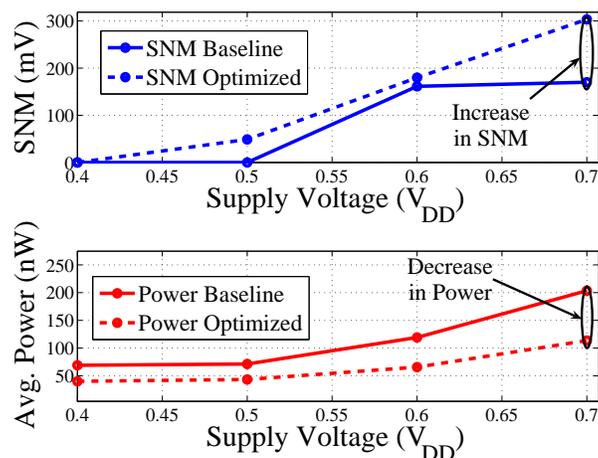


Fig. 6. Power and SNM comparison of optimal and baseline SRAM.

For an  $8 \times 8$  array using the optimized cells (Fig. 7), the average power consumption is  $4.5 \mu W$ .

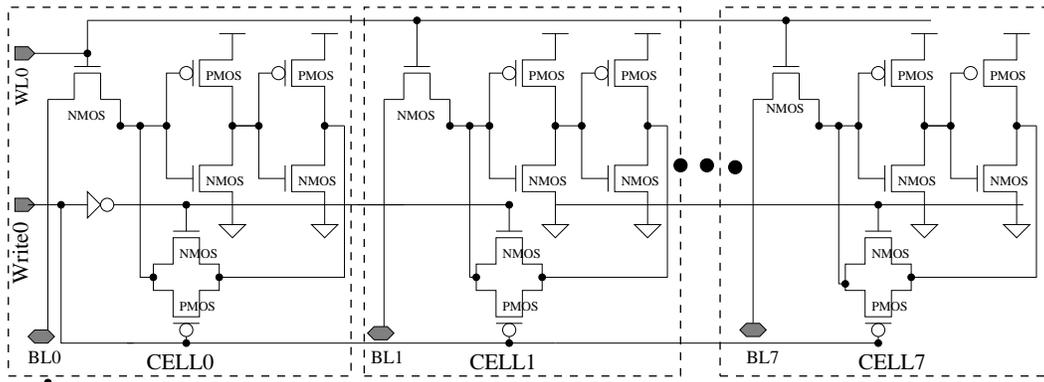


Fig. 7. Schematic representation of one row of the  $8 \times 8$  array constructed using optimized 7T cells.

## VI. STATISTICAL VARIABILITY ANALYSIS OF THE SRAM

Threshold voltage variation is strongly related to device geometry and doping profile. We selected twelve process parameters for process variation: (1,2)  $T_{oxn,oxp}$ : NMOS, PMOS gate oxide thickness ( $nm$ ), (3,4)  $L_{na,pa}$ : NMOS, PMOS access transistor channel length ( $nm$ ), (5,6)  $W_{na,pa}$ : NMOS, PMOS access transistor channel width ( $nm$ ), (7,8)  $L_{nd}, W_{nd}$ : NMOS driver transistor channel length, width ( $nm$ ), (9,10)  $L_{pl}, W_{pl}$ : PMOS load transistor channel length, width ( $nm$ ), (11,12)  $N_{chn,chn}$ : NMOS, PMOS channel doping concentration ( $cm^{-3}$ ). Some of the parameters are correlated; this is taken into consideration during simulation for realistic study.

The SNM is exhaustively evaluated through 1000 Monte Carlo simulations. Figs. 8(a), 8(d), 8(g), 8(j) show the effect of process variations on the butterfly curve with  $S_{PWR}$ ,  $S_{SNM}$  and  $S_{OBJ}$  based configurations, respectively. Figs. 8(b), 8(e), 8(h), 8(k) show the distributions for “SNM High” and “SNM Low” extracted from the Monte Carlo simulations with  $S_{PWR}$ ,  $S_{SNM}$  and  $S_{OBJ}$  based configurations. “SNM Low” is treated as the actual SNM. Table IV shows the corresponding statistical data. Figs. 8(c), 8(f), 8(i), 8(l) show the distribution of average power. It follows a lognormal nature.

## VII. SUMMARY, CONCLUSIONS AND FUTURE RESEARCH

A methodology is presented for simultaneous optimization of SRAM cell power and read stability. A  $45nm$  single-ended 7T cell is used as case study, leading to 50.6% power reduction (including leakage) and 43.9% increase in read stability (read SNM). A novel DOE-ILP approach has been used for power

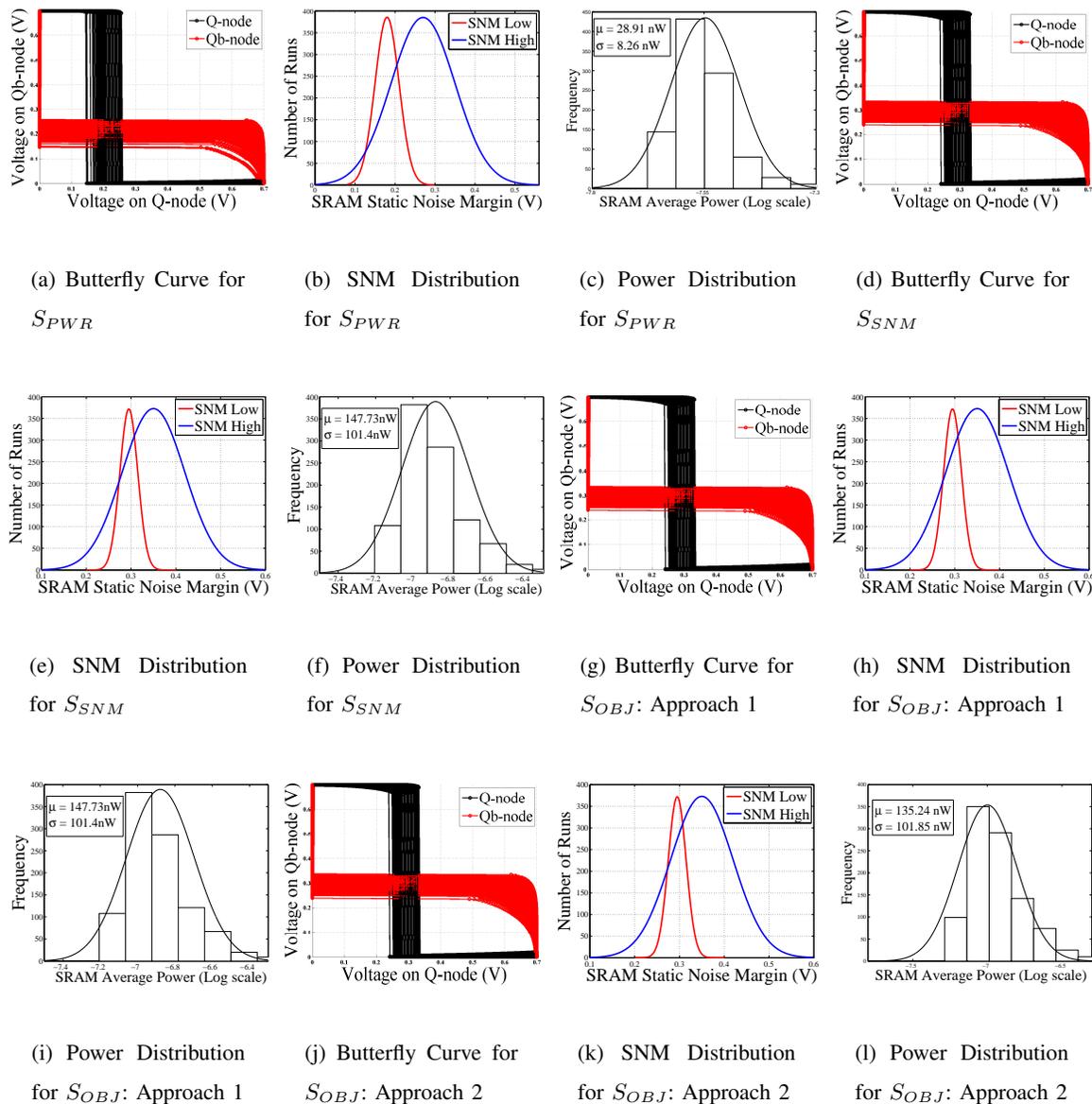


Fig. 8. Process variation study for  $S_{PWR}$ ,  $S_{SNM}$  and  $S_{OBJ}$  based configurations using Monte Carlo simulations.

minimization and read SNM maximization. The effect of process variation of twelve process parameters on the proposed cell is evaluated, and it is found to be process variation tolerant. An  $8 \times 8$  array has been constructed using the optimized cell and data for power consumption is presented.

A fair comparison of the proposed methodology with prior research is difficult. The proposed and existing research differ in terms of technology node, topology, and array size. However, a broad compar-

TABLE IV  
 STATISTICAL PROCESS VARIATION EFFECTS ON SRAM POWER AND SNM

| Optimization           | Parameter  | $\mu$    | $\sigma$ |
|------------------------|------------|----------|----------|
| $S_{PWR}$              | $P_{SRAM}$ | 28.91nW  | 8.26nW   |
|                        | SNM        | 180mV    | 30mV     |
| $S_{SNM}$              | $P_{SRAM}$ | 147.73nW | 101.4nW  |
|                        | SNM        | 295mV    | 28mV     |
| $S_{OBJ}$ : Approach 1 | $P_{SRAM}$ | 147.73nW | 101.4nW  |
|                        | SNM        | 295mV    | 28mV     |
| $S_{OBJ}$ : Approach 2 | $P_{SRAM}$ | 135.24nW | 101.85nW |
|                        | SNM        | 295mV    | 28mV     |

ative perspective is presented with some closely related research [9], [11], [10] which does not account for dynamic current in optimization and only leakage minimization is measured whereas the current paper taken into account all components like dynamic, subthreshold, gate-oxide leakages. In [9], [11], a combined dual- $V_{Th}$  and dual- $T_{ox}$  assignment is used where the leakage power reduction is 53.5% and SNM increase is 43.8%. However, the current methodology which considers only dual- $V_{Th}$  (this is significant in terms of manufacturing cost) has resulted in power reduction (accounting all components) of 50.6% and increase in read SNM as 43.9%.

Future research will involve array-level optimization of SRAM where mismatch and process variation will be considered as part of the design flow. Also, thermal effects will be incorporated. Simultaneous PVT optimal SRAM design for sub-45nm technology will be performed. Also, to make the optimization methodology more practical, transistor size will be included along with  $V_{Th}$  state for each transistor in the search space.

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