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RESEARCH ARTICLE

A Comparative Study on Gate Leakage and Performance of High-κ Nano-CMOS Logic Gates

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This paper provides a novel attempt to evaluate the gate leakage and delay characteristics of CMOS transistors and logic gates with various alternative high-κ gate dielectrics which are replacing SiO_2 in traditional nanoscale MOSFETs. Results have been obtained for both fixed as well as variable loads. The assumption that all gates drive the same load is considered in order to provide a fair comparison of the effect of the variation of design and process parameters, especially that of different high-κ dielectrics on the gate direct tunneling current and propagation delay. On the other hand, the variable loading effect considers a set of practical loading conditions for the logic gates. An exhaustive comparison of all cases finally presents a concluding evidence that the tunneling current is independent of loading conditions. On the other hand, there is an increase in the delay as the dielectric constant of gate material, and consequently the load on the device, increases. Ultimately, this paper presents fast and accurate models for on-the-fly calculation of tunneling current and delay with the aim of integrating them into design automation tools.

Keywords: Low-power design, gate leakage, leakage current, tunneling current, high-κ, nanoscale CMOS

1. Introduction and motivation

The demand for ever smaller and portable electronic devices has ultimately driven the scaling of CMOS towards its physical limits. Transistor feature sizes have dramatically shrunk with technology scaling and the value of gate oxide thickness (T_{ox}) has reached the range of $12 - 16\mathring{A}$ which is just a few mono-layers of SiO_2. This trend is unavoidable in order to provide the required current drive in the presence of low supply voltages. It has led to a drastic change in the leakage components of the device both in the active and inactive modes of operation. Consequently, the gate direct tunneling current I_{gate} has emerged as the most prominent form of leakage.

Use of alternatives for SiO_2 as the gate dielectric has led to the construction of non-classical transistors demonstrated in Fig. 1 [Misra et al. (2005), Manchanda et al. (2001)]. The use of high$-\kappa$ serves the dual purpose of scaling the device as well as reducing gate leakage [Bohr et al. (2007)]. Intel has recently revealed a processor in the Nehalem family, called *Westmere* using such transistors of $32nm$ technology [Intel (2009)].

A proper analysis of the dielectric is necessary in order to give the designer a complete idea of the efficacy of the material as a gate dielectric and to evaluate its potential in replacing SiO_2. It further necessitates the development of analytical models for on-the-fly calculation of electrical characteristics of logic level representations of circuits to facilitate design automation and exploration decisions.

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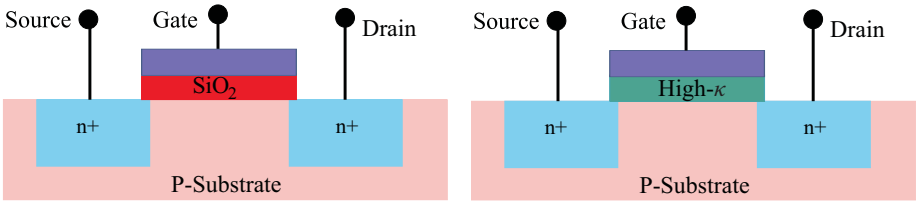


(a) with SiO_2 gate dielectric (b) with high-κ gate dielectric

Figure 1. Nanoscale planar CMOS transistors: Classical versus non-classical

The rest of the paper is organized as follows. Section 2 summarizes contributions of this paper and reviews important literature results relating to this work. In Section 3 we give an overview of the major high-κ dielectric materials and their process technologies. In section 4 we present a complete transient study of logic gates. We present the characterization of logic gates with respect to design and process parameters in Section 5. Analytical modeling of high-κ devices is presented in Section 6. The effect of load variation for high-κ logic gates is examined in 7. Applications of our analysis in terms of functional unit library characterization and high level synthesis using high-κ cells are given in Section 8. Our findings and directions for future work are summarized in Section 9.

2. Contributions of this paper and related research

The replacement of SiO_2 with a number of alternative dielectrics necessitates the development of an analytical method for on-the-fly calculation of electrical characteristics of logic circuits. These analytical expressions will help in extending the benefits of design automation involving traditional CMOS processes to design using alternative, non-traditional processes. This paper presents a novel characterization of high-κ nano-CMOS logic gates and provides a complete analysis of the various associated design and process parameters in order to enhance the design process. The various *contributions* of this paper are as follows:

- A new approach is introduced for the characterization of high-κ dielectric CMOS transistors and corresponding logic gates.
- A complete view of the design and process parameter variations of the devices is given, when high-κ gate dielectric materials are used.
- An exhaustive overview of the performance and characteristics of high-κ gates is presented for both fixed and variable load.
- Novel analytical functions are given to provide on-the-fly calculations of the device characteristics which would be a great tool for the design engineer for design space and technology exploration.

There has been extensive effort from academic as well as industrial research communities to overcome the barriers to scaling of devices. This has extended from the domain of design and fabrication to the study of device physics and material science [Yang et al. (2003), Yu et al. (2002)]. Few research works exist for analysis and estimation of gate leakage in nano-CMOS circuits. In [Rao et al. (2003)], the authors presented mechanisms for estimation of leakage. In [Lee et al. (2003)], a method is presented for analysis of I_{gate}. The authors in [Guindi and Najm (2003)] have formulated "state-dependent" gate leakage. The authors in [Agarwala et al. (2005)] have developed several methods of analysis of total leakage. In [Mukhopadhyay et al. (2003)], the authors have studied the effect of gate tunneling current in ultra-thin gate oxide MOS devices. An analysis of the loading effect on leakage and a method of estimation of the total leakage in a logic circuit is proposed in [Mukhopadhyay et al. (2005)]. In [Maitra and Bhat (2003)], the authors propose

analytical schemes to combine the channel and edge components of the gate oxide direct tunneling current.

3. High$-\kappa$ dielectrics in CMOS technology

3.1 *Need for high-κ gate dielectrics*

SiO_2 has reached the fundamental limits in its role as the gate dielectric of choice [Karamcheti et al. (2000)]. This is primarily due to the fact that decrease in the gate-oxide thickness is associated with a concomitant and significant increase in tunneling current. This inevitable drawback and the impending increase in leakage has called for alternatives candidates to replace SiO_2. Such candidates need to have a higher dielectric constant than SiO_2 [Manchanda et al. (2001)].

3.2 *Fabrication technology for high$-\kappa$*

Several materials have been investigated for use in nano-CMOS technology, such as ZrO_2, TiO_2, BST, HfO_2, Al_2O_3, SiON, and Si_3N_4 [Yang et al. (2003), Manchanda et al. (2001)]. It is a challenging task in itself to integrate these materials into conventional CMOS processes [X. Guo and T. P. Ma (1998)]. Progress has been made in the development of various technologies for high-$-\kappa$ gate dielectric deposition, but is still not in the mainstream of fabrication [Huff et al. (2001), Kingon et al. (2000), Qi and et al. (2000)].

3.3 *Compact modeling for high$-\kappa$*

While the materials research is in progress, there is no research to address automatic design and synthesis of systems using high-κ transistors. For compact modeling based study of high-κ, non-classical transistors using the BSIM4/5 model, *two possible options* can be considered: (i) varying the model parameter in the model card that denotes relative permittivity (EPSROX) and/or (ii) finding the equivalent oxide thickness (EOT) for a dielectric under consideration. Approach (i) may not be sufficient to model the behavior of non-classic nano-CMOS with non-SiO_2 dielectrics as it does not correctly account for the barrier height of non-SiO_2 dielectrics. Using method (ii) the EOT will be calculated so as to keep the ratio of relative permittivity over dielectric thickness constant.

Both of these approaches ignore several aspects of the physics behind non-SiO_2 dielectrics, particularly in the Si/dielectric interface. However, in the absence of published device data, the methodology presented will provide meaningful information of the various materials under consideration for EDA applications.

We believe that along with the efforts in introducing high-κ gate dielectrics, future physical-aware low power synthesis methodologies should be developed in order to incorporate them into existing automatic design or synthesis flows. This leads us to perform extensive modeling, analysis and characterization of a number of high-κ dielectric CMOS logic gates to facilitate design space exploration.

4. Analysis of logic gates

For direct tunneling, the tunneling probability of an electron is affected by the barrier height, and the structure and thickness of the gate dielectric material. The tunneling current density of a MOS J_{DT} (in A/m^2) is expressed by [Mohanty and Kougianos (2006),

Roy et al. (2003), Choi et al. (1999)]:

$$J_{DT} = \left(\frac{q^3 V_{ox}^2}{16\pi^2 \hbar \phi_B T_{ox}^2}\right) \times \exp\left[-\left\{\frac{4\sqrt{2m_{eff}}\phi_B{}^{1.5} T_{ox}}{3\hbar q V_{ox}}\right\} \times \left\{1 - \left(1 - \frac{V_{ox}}{\phi_B}\right)^{1.5}\right\}\right], \tag{1}$$

where q is the electronic charge (in Cb), V_{ox} is the voltage drop across the gate oxide (in V), $\hbar$ is Planck's constant (in m^2kg/s), T_{ox} is the electrical equivalent oxide thickness (in m), ϕ_B is the barrier height for the gate dielectric (in V), and m_{eff} is the effective carrier mass (in kg). Some of these parameters are implicitly or explicitly affected by the use of high-κ dielectric materials.

The corresponding gate leakage current can be divided into five components, such as I_{gs} and I_{gd} (components due to the overlap of gate and diffusions), I_{gcs} and I_{gcd} (components due to tunneling from the gate to the diffusions via the channel) and I_{gb}, the component due to tunneling from the gate to the bulk via the channel [Mukherjee et al. (2005), Cao et al. (2000)]. The gate leakage for a device can then be calculated as follows:

$$I_{gate_{MOS}} = I_{gs} + I_{gd} + I_{gcs} + I_{gcd} + I_{gb}, \tag{2}$$

where all the currents are in A.

The above equations can be used in several ways to estimate gate leakage of CMOS circuits. Numerical equation solvers using a high-level language like MATLAB or C can be written to solve the simultaneous equations for different input conditions. Commercial tools like Sentaurus Process and Device, can also be used to perform the simulations and calculations. Another option is to use the above models for each transistor in a circuit level netlist and use SPICE as a nonlinear equation solver to calculate the currents. The SPICE option is followed in this paper, as it is simple to use and easily available and produces accurate results. We chose to use the Predictive Technology Model (PTM) since it is well established and is able to predict general technological trends [Cao et al. (2000)].

We performed a complete transistor level characterization of a number of logic gates (NOT, NAND, NOR, AND and OR) with respect to gate tunneling leakage and input-output delay using an analog circuit simulator [SPECTRE (2005)], but present only the results for NAND/NOR for brevity.

4.1 *Average current and delay analysis*

The gate direct tunneling current of a logic gate is calculated from all components for each PMOS and NMOS device in the logic gate. Likewise, the total gate tunneling current for each device was calculated by summing all components:

$$I_{gate}[i] = I_{gs}[i] + I_{gd}[i] + I_{gcs}[i] + I_{gcd}[i] + I_{gb}[i], \tag{3}$$

where the index i identifies the device within a gate. A total gate tunneling current for the logic gate (I_{gate} is then calculated by summing the gate currents over all the devices in the gate:

$$I_{gate} = \sum_i I_{gate}[i]. \tag{4}$$

During its various states of operation, a logic gate presents different dominant leakage paths, depending on the combination of inputs. For example, for 2-input gates, for each of the four possible states (00, 01, 10 and 11), the overall gate tunneling current (I_{00}, I_{01}, I_{10}, and I_{11}, respectively) is calculated from Eqns. 3 and 4. Assuming that all

states are to occur with equal probability, an "average direct tunneling current" ($\overline{I_{gate}}$) is calculated as :

$$\overline{I_{gate}} = \left(\frac{I_{00} + I_{01} + I_{10} + I_{11}}{4} \right). \tag{5}$$

On the other hand, the "peak tunneling current" can be defined as $I_{peak} = \max(I_{00}, I_{01}, I_{10}, I_{11})$.

While characterizing the gate leakage current we present its average value over various switching states of the logic gate. This ensures that we eliminate the effect of stacking. However, a state dependent look-up-table based gate leakage current approach can always be used to facilitate its estimation in larger CMOS circuits.

Following standard approaches, we define the delay as the time difference between the 50% level of the input and output waveforms Baker et al. (1998). For worst-case scenario, we chose the maximum delay time regardless of whether this was due to a low-to-high or a high-to-low transition.

A load value of 10 times the total gate capacitance C_{gg} of the PMOS device has been chosen Mukherjee et al. (2005). In order to obtain a fair comparison of the performance of the various dielectrics, without reference to a specific load, this value was calculated for a SiO_2 device and kept fixed throughout the simulations.

4.2 *Process and Design Parameters Variation*

The BSIM 4.4 models generated represent a hypothetical $45nm$ CMOS process with oxide thickness $T_{ox} = 1.4nm$, threshold voltage $V_{Th} = 0.22V$ for the NMOS and $V_{Th} = -0.22V$ for the PMOS. The nominal power supply is $V_{DD} = 0.7V$. These models are also scalable with respect to T_{ox} and channel length. The effect of varying oxide thickness (T_{ox}) was incorporated by varying $TOXE$ in the spice model deck directly. The effect of varying dielectric material was modeled by calculating an equivalent oxide thickness (T^*_{ox}) according to the formula:

$$T^*_{ox} = \left(\frac{\kappa_{SiO_2}}{\kappa_{gate}} \right) \times T_{gate}. \tag{6}$$

In the above, κ_{gate} is the relative permittivity (dimensionless) and T_{gate} is the thickness of the gate dielectric material (in m or $\mathring{A}$) other than SiO_2, while κ_{SiO_2} is the relative permittivity of SiO_2 (=3.9). In this section we perform a parametric study for κ; however all real values of κ may not translate to a specific physical dielectric in nano-CMOS technology. The length of the device is proportionately changed to minimize the impact of higher dielectric thickness on device performance and to maintain the per width gate capacitance constant as per CMOS fabrication requirements [Taur (2002), Weste and Harris (2005)]. Thus, the scaling ratio of channel length to gate thickness is maintained constant. Moreover, the length and width of the transistors are chosen to maintain a $\left(\frac{W}{L}\right)$ ratio of $4:1$ for NMOS and $8:1$ for PMOS to ensure equal flow of current through the devices and symmetric switching points. The variation of V_{DD} is achieved by running a parameter sweep in the simulator. Different simulation results for these variations are presented in figures 2 and 3.

4.2.1 Effect of variation on tunneling current

It can be seen from Fig. 2(a) that with an increase in the value of κ there is a steady decrease in the value of tunneling leakage, I_{gate}. This trend continues up to a knee region of $\kappa = 12$, after which all the components eventually become almost constant and there is not much of a decrease in the value of I_{gate} with an increase in κ. This indicates the

presence of a saturation zone in the gate leakage versus κ characteristics which implies that there is *not much benefit in deploying gate dielectrics of very high-κ* (i. e. $\kappa > 12$) *for gate tunneling leakage reduction* in the $45nm$ node. The physical mechanism for the presence of the knee can be seen by combining equations 1 and 6:

$$\ln J_{DT} \sim -\alpha \ln \kappa - \beta\kappa, \tag{7}$$

where α and β (both in $\ln(A/m^2)$) are positive, technology-dependent constants. The knee occurs when the linear (second) term in equation 7 overtakes the logarithmic (first) component. Since the constants α and β depend on material parameters, it is expected that the knee region will vary for different technology nodes.

As can be seen from figure 2(b) there is a uniform decrease among all the components of the gate tunneling current with an increase in the gate thickness. However, this effect can be utilized in some design styles as in dual-thickness approaches as an effective means of minimizing the impact of gate tunneling leakage [Mohanty et al. (2006)].

Finally, ss can be seen from Fig. 2(c) an increase in the supply voltage leads to a corresponding increase in the level of the gate tunneling leakage. This trend supports the scaling down of the supply voltage along with scaling of the device. Thus, supply voltage scaling can, to a certain extend, reduce gate leakage as well as dynamic power.

4.2.2 Effect of variation on propagation delay

The variation of T_{pd} is shown in Fig. 3(a), and demonstrates that there is a sharp increase in the value of T_{pd} with an increase in the gate dielectric constant. This increase continues until a value of around $\kappa = 6$ after which the slope is much lower. The increase in propagation delay can be attributed to the increase in capacitance per unit area (C'_{gate}, in F/m^2) of gate oxide with dielectric constant, i.e.,

$$C'_{gate} = \left(\frac{\kappa_{gate}}{T_{gate}}\right), \tag{8}$$

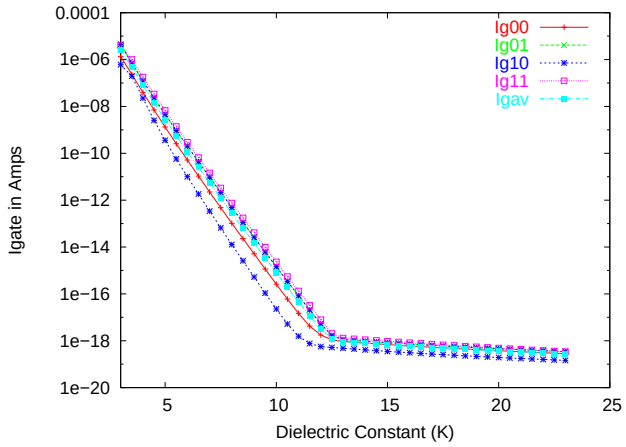
while the presence of a "knee" region around $\kappa \simeq 6$ is due to similar behavior of T_{pd} as in equation 7.

The effect of variation of propagation delay with respect to the process parameter gate thickness shown in figure 3(b) indicates that there is an increase in the propagation delay of the gate as the gate thickness increases. This happens due to the increase in gate capacitance (C_{gate}, in F) with oxide thickness T_{ox} (in m or nm) for a particular dielectric, say SiO_2 with κ, as evident from the following discussion. The gate capacitance (C_{gate}) is given by [Weste and Harris (2005)]:

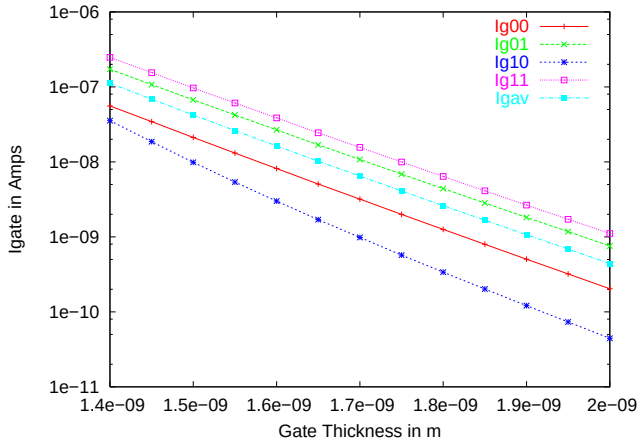
$$C_{gate} = \epsilon_{ox}\left(\frac{L}{T_{ox}}\right)W = \epsilon_{ox}\left(\frac{W}{L}\right)\left(\frac{L}{T_{ox}}\right)L, \tag{9}$$

where ϵ_{ox} is the permittivity of the gate material (in F/m) and L and W are the length and width of the transistor (both in m or nm). Thus, as per the suggestion in [Taur (2002), Sultania et al. (2004), Weste and Harris (2005)], with increase in T_{ox} when we maintain $\left(\frac{L}{T_{ox}}\right)$ and $\left(\frac{W}{L}\right)$ constant by increasing L, C_{gate} increases, and hence the propagation delay. This result is consistent with the experimental results presented in [Sultania et al. (2004)], in the context of gate leakage reduction.

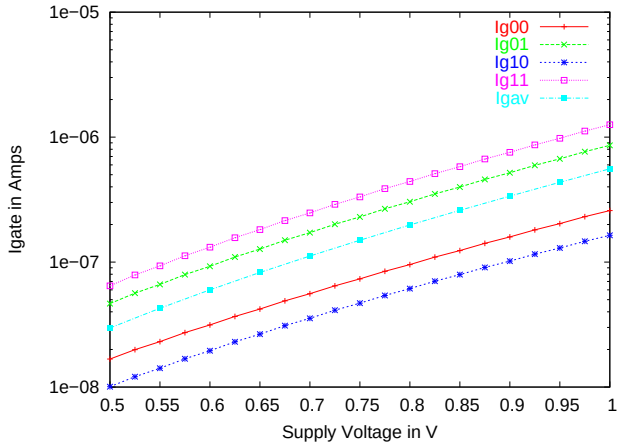
It can be observed from Fig. 3(c) that the propagation delay shows a decreasing trend with an increase in the value of the supply voltage when κ_{gate} and T_{gate} are kept fixed. This is due to the increase in the drive current resulting from the increase in supply voltage. However, a better insight of the situation can be obtained from the following discus-



(a) I_{gate} Vs κ



(b) I_{gate} Vs T_{gate}



(c) I_{gate} Vs V_{DD}

Figure 2. Gate tunneling current for a 2-input NAND logic gate for different input switching states (00, 01, 10, 11) when the dielectric constant (κ), gate dielectric thickness (T_{gate}), and supply voltage (V_{DD}) are varied.

sion. For a technology parameter α (in s/F), propagation delay is given by [Rabaey et al. (2003)]:

$$T_{pd} = \alpha C_{load} \left(\frac{1}{1 - V_{Th}^*/V_{DD}} \right), \tag{10}$$

where $V_{Th}^{*} = V_{Th} + 0.5V_{DSAT}$ and V_{DSAT} is the drain saturation voltage. All voltages are in V. Since, $-1 < \frac{V_{Th}^{*}}{V_{DD}} < 1$, using a McLaurin series expansion, we get:

$$T_{pd} = \alpha C_{load}\left(1 + \frac{V_{Th}^{*}}{V_{DD}} + \left(\frac{V_{Th}^{*}}{V_{DD}}\right)^{2} + ...\right) \tag{11}$$

$$\approx \alpha C_{load}\left(1 + \frac{V_{Th}^{*}}{V_{DD}}\right) \tag{12}$$

This clearly suggests that for fixed load and threshold voltage, as V_{DD} increases, T_{pd} decreases. However, as scaling continues, the trend is to scale down the supply along with other device features and that is also compatible with the objective of decreasing the gate leakage current in the nanometer regime.

5. Logic gates with specific high$-\kappa$ nano-CMOS

The NAND gate study in section 4 suggests that the two significant parameters that influence the gate tunneling current are the gate thickness T_{gate} and the supply voltage (V_{DD}). The characterization of the effect of these two parameters will give a complete picture of the gate tunneling leakage characteristics of the various high-κ materials in their role as CMOS transistor gate dielectrics.

5.1 *Varying κ for different T_{gate}*

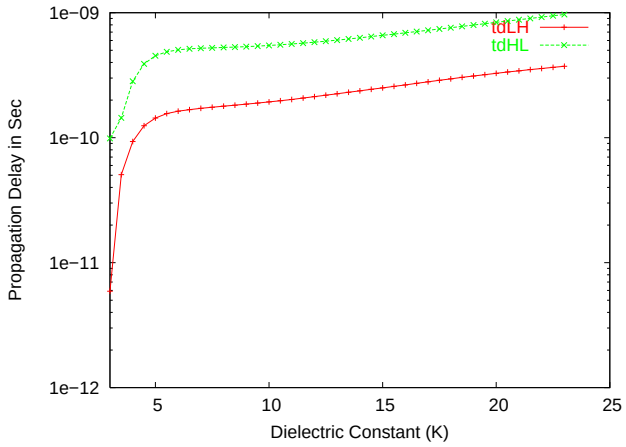
In order to evaluate the effect of the thickness of the gate dielectric on the leakage current, the thickness (T_{gate}) was varied over a range of $1.4nm$ to $2.0nm$ for a particular dielectric and the gate leakage current was studied. As can be seen from figure 4(a), the gate tunneling current decreases with an increase in the dielectric constant and for a particular dielectric the gate tunneling current decreases with an increase in the gate thickness. The decrease in the gate tunneling current with the increase in the gate thickness is more prominent in the range of medium dielectric constant which is observed to be about a κ value of 7 to 9. After a value of $\kappa = 12$ the value of I_{gate} becomes almost constant.

Figure 4(b) shows the variation in the propagation delay of a 2-input NAND gate when the process parameter T_{gate} is changed along with a change in the gate dielectric. It can be seen that for a given dielectric, the propagation delay increases as the gate dielectric thickness increases. This poses a serious limitation to the approach of using a gate of higher thickness to circumvent the problem of gate tunneling current leakage. Also, for a given thickness it can be seen that, as the dielectric constant increases, there is a corresponding increase in the propagation delay. Also, it can be observed from the plot in Fig. 4(b) that there is an almost exponential increase in the delay of the gate with an increase in dielectric constant.

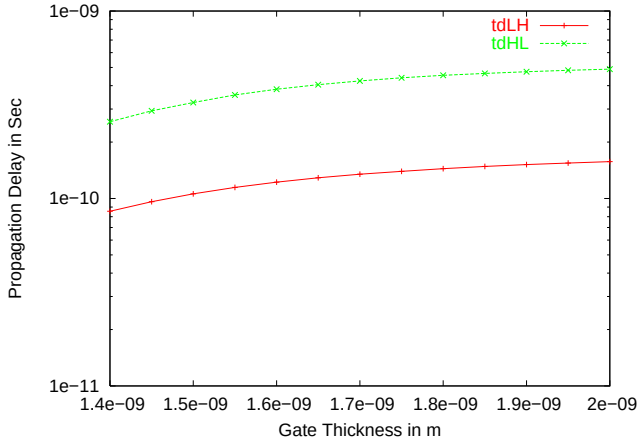
5.2 *Varying κ for different V_{DD}*

From figure 5(a) it can be seen that for any given supply voltage the gate tunneling current decreases with an increase in the value of gate dielectric constant. Also for a given dielectric constant (κ) the gate tunneling current increases with an increase in the value of the supply voltage.

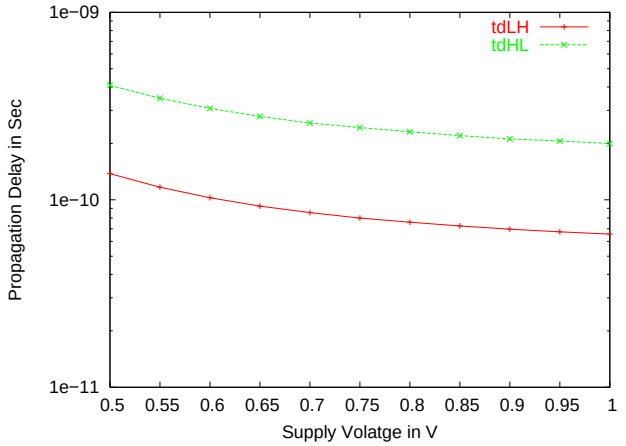
It can be seen from figure 5(b) that for a given supply voltage (V_{DD}), the propagation delay increases with an increase in the value of κ which is a common trend for all values of



(a) T_{pd} Vs κ



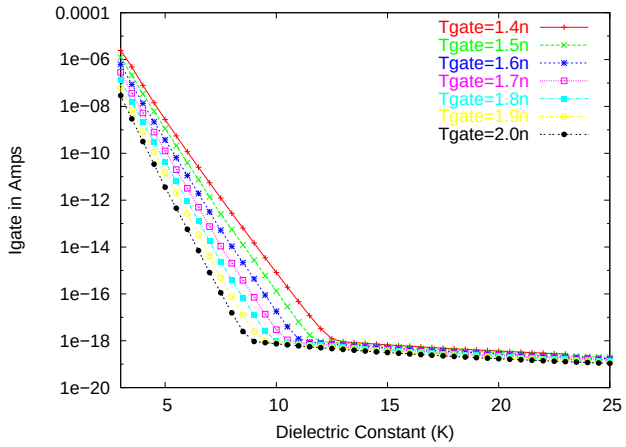
(b) T_{pd} Vs T_{gate}



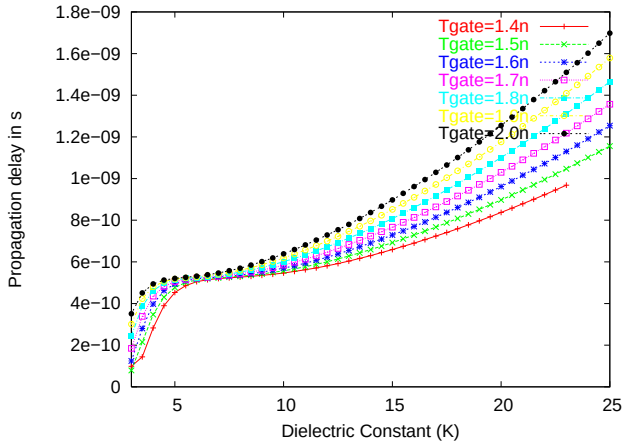
(c) T_{pd} Vs V_{DD}

Figure 3. Low-to-high and high-to-low propagation delay (T_{pd}) for a 2-input NAND logic gate for different input switching states (00, 01, 10, 11) when the dielectric constant (κ), gate dielectric thickness (T_{gate}), and supply voltage (V_{DD}) are varied.

V_{DD}. Also, from the same plots it can be observed that for a particular value of dielectric constant the propagation delay tends to increase with a decrease in the value of (V_{DD}).



(a) $\overline{I_{gate}}$ Vs κ for different T_{gate}



(b) T_{pd} Vs κ for different T_{gate}

Figure 4. Effect of variation of the dielectric constant on tunneling current ($\overline{I_{gate}}$) and propagation delay (T_{pd}) of a 2-input NAND gate for different gate dielectric thicknesses (T_{gate}).

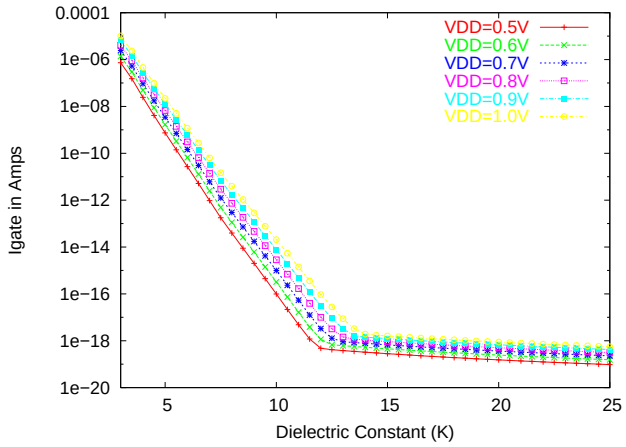
5.3 *Specific dielectrics (κ)*

A number of dielectric materials are being investigated as potential alternatives to silicon. Among some of the more prominent ones are SiON, Si_3N_4, Al_2O_3, $ZrSiO_4$, $HfSiO_4$ and HfO_2 [Yang et al. (2003), Manchanda et al. (2001)]. Figures 6(a) and 6(b) show how these alternative dielectrics perform with respect to variations in the design and process parameters.

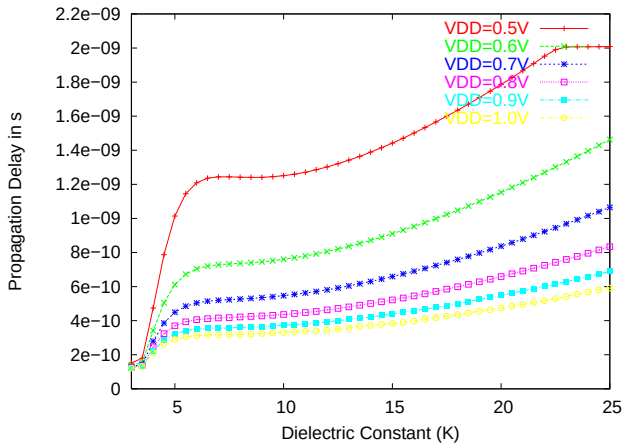
5.3.1 Variation of process parameter T_{gate}

The combined effect of a change in the gate dielectric thickness (process parameter) with different dielectrics can be seen in figure 6(a). Among the dielectrics considered, HfO_2 has the highest dielectric constant while SiO_2 has the lowest. It can be clearly seen that in all cases, the gate tunneling current for SiO_2, having the least κ, is the highest across all thicknesses. As the value of κ increases the gate tunneling current reaches a constant level for all values of thickness. In other words, the tunneling current can be obviated to a great extent with the use of high-κ dielectrics.

Figure 6(b) shows the behavior of different dielectrics for a change in the process parameter T_{gate} with respect to the propagation delay. In this case the dielectric with the least value of κ, i.e., SiO_2 has the least propagation delay across all thicknesses. However, as the thickness increases the propagation delay increases too. In the case of dielectrics with a medium value of κ the propagation delay stays constant over the range of dielectric



(a) $\overline{I_{gate}}$ Vs κ for different V_{DD}



(b) T_{pd} Vs κ for different V_{DD}

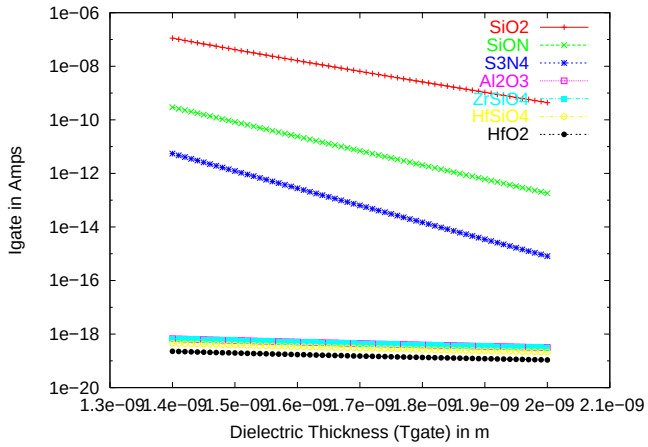
Figure 5. Effect of variation of the dielectric constant (κ) on tunneling current ($\overline{I_{gate}}$) and propagation delay (T_{pd}) of a 2-input NAND gate for varying supply voltage V_{DD}.

thicknesses.

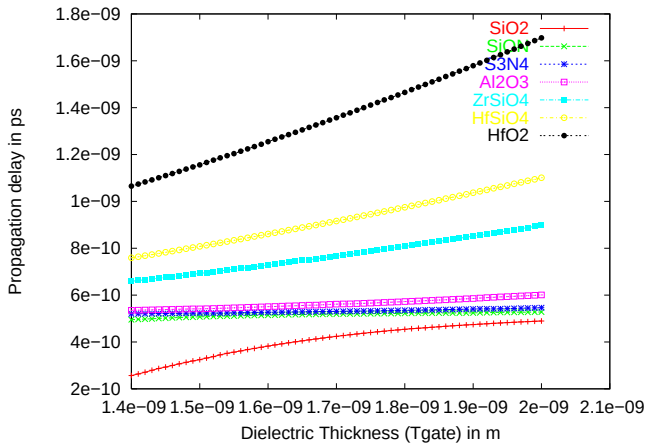
5.3.2 Variation of design parameter V_{DD}

As can be seen from figure 7(a), the gate tunneling current increases with an increase in the value of the supply voltage for all dielectrics. In the case of the default gate dielectric, i.e., SiO_2, the gate tunneling current is maximum among all the other dielectrics across the range of supply voltages from $0.5V$ to $1.0V$. On the other hand, HfO_2, having the highest value of κ, exhibits the smallest gate tunneling current throughout the range of supply voltages. For any given supply voltage, it can be seen that the gate tunneling current is lower for dielectrics with higher κ.

The plot in figure 7(b) shows the behavior of propagation delay for various dielectrics when the the design parameter supply voltage is changed. When the supply voltage is kept fixed at $0.5V$, the propagation delay is larger for gate dielectrics with higher values of κ. As the supply voltage increases it can be seen from the same figure that there is a corresponding decrease in the propagation delay. Also it is noted that the dielectric with highest value of κ, i.e., HfO_2, has the highest value of propagation delay while SiO_2 with the lowest value of κ has the lowest values of propagation delay across the range of supply voltages.



(a) $\overline{I_{gate}}$ Vs T_{gate}



(b) T_{pd} Vs T_{gate}

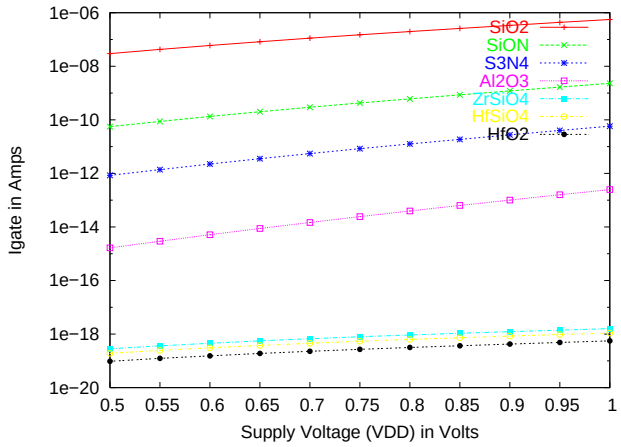
Figure 6. Evaluation of selected gate dielectrics for effect of variation of the process parameter T_{gate} on gate tunneling current and propagation delay.

6. Analytical modeling of high-κ nano-CMOS logic gates

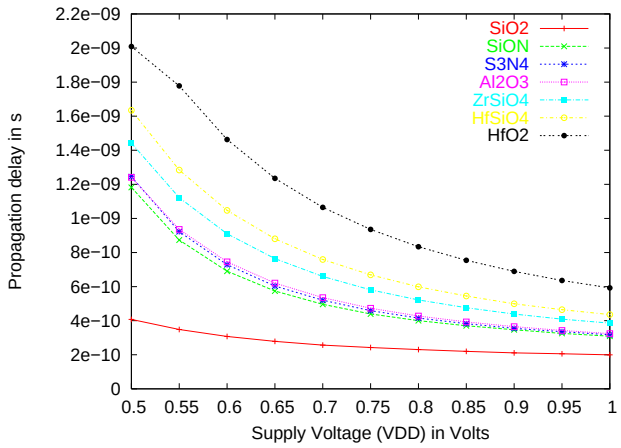
In this section we perform a least squares fit of the data presented in section 5 to a set of functional equations. For brevity NAND/NOR data is presented, however following the methodology shown here, similar results can be obtained for other logic gates.

6.1 *Modeling for κ variation*

We present a set of functions in table 1 which show the best-fit for the effect of variation of gate dielectric constant κ on the gate tunneling current and propagation delay. As can be seen from the table, the effect on various gates and on various parameters is distinct. However the effect of a change in κ can be represented through an exponential function which has almost the same nature for all gates under consideration. For the 2-input NAND gate the gate tunneling current decreases exponentially with an increase in the dielectric strength. The propagation delay varies in a more complex fashion; it is represented as a combination of two functions over the range of dielectric strength considered. The same is the case for the other gate in consideration, i.e., the NOR2.



(a) $\overline{I_{gate}}$Vs V_{DD}



(b) T_{pd} Vs V_{DD}

Figure 7. Evaluation of selected gate dielectrics for effect of variation of the design parameter V_{DD} on gate tunneling current and propagation delay.

6.2 *Modeling for T_{gate} variation*

The effect of variation of dielectric thickness on the gate tunneling current and propagation delay of various logic gates has been modeled and presented in table 2. This table shows that the gate tunneling current has a uniform characteristic for all gates when the gate thickness is varied. Across the range of variation of T_{gate} the tunneling current shows a trend of exponential decrease with increase in the value of gate thickness. This is verified with the nature of data and curve presented in section 5. The fitting for both NAND2 and NOR2 correspond to a Langmuire function and shows an excellent fit over the range in consideration.

6.3 *Modeling for V_{DD} variation*

For the variation of V_{DD}, both I_{gate} and T_{pd} behave in the same fashion for all gates. While the gate tunneling current shows a uniform exponential increase with an increase in the value of the supply, the propagation delay shows an exponential decrease and the nature remains the same across all gates under consideration.

The curve fitting in all the cases shows a perfect fit and gives us a very useful means of analysis and design of the various design and process parameters of the logic gates. This can be extended to other gates or compound gates and thus result in a faster design process with the analytical functions replacing the look-up tables at the back end of design

Table 1. Curve fitting for effect of variation in gate dielectric constant in logic gates. Parameters with no units indicated are dimensionless.

Gates	Attributes	Fitting Functions	Function Parameters	Corr. Coeff
NAND2	$\overline{I_{gate}}$ Vs κ	$\overline{I_{gate}} = A * e^{\frac{-K}{\alpha}} + \overline{I_{gate_0}}$	$\overline{I_{gate_0}} = -4.6 * 10^{-9}\ A$ $A = 0.00966\ A$ $\alpha = 0.36115$	0.99655
	T_{pd} Vs κ	$T_{pd} = \begin{cases} B + \frac{A-B}{1+e^{\frac{K-K_0}{dK}}},\ 2.5 \leq K < 6 \\ C * e^{\frac{-K}{\alpha}} + T_{pd_0},\ 6 \leq K < 30 \end{cases}$	$A = 4.12 * 10^{-11}\ s$ $B = 5.14 * 10^{-10}\ s$ $K_0 = 4.02176$ $dK = 0.47847$	0.99725
			$T_{pd_0} = 3.75 * 10^{-10}\ s$ $C = 6.94 * 10^{-11}\ s$ $\alpha = 10.62653$	0.99797
NOR2	$\overline{I_{gate}}$ Vs κ	$\overline{I_{gate}} = A * e^{\frac{-K}{\alpha}} + \overline{I_{gate_0}}$	$\overline{I_{gate_0}} = -1.42 * 10^{-8}\ A$ $A = 0.00302\ A$ $\alpha = 0.43885$	0.97657
	T_{pd} Vs κ	$T_{pd} = T_{pd_0} + A * (1 - e^{\frac{-K}{\alpha}}) + B * (1 - e^{\frac{-K}{\beta}})$	$T_{pd_0} = -1.21 * 10^{-8}\ s$ $A = 1.23 * 10^{-8}\ s$ $\alpha = 6.66 * 10^{-1}$ $B = 1.13 * 10^{-1}\ s$ $\beta = 10548034228$	0.96941

Table 2. Curve fitting for effect of variation gate dielectric thickness in logic gates. Parameters with no units indicated are dimensionless.

Gates	Attributes	Fitting Functions	Function Parameters	Corr. Coeff
NAND2	$\overline{I_{gate}}$ Vs T_{gate}	$\overline{I_{gate}} = A * e^{\frac{-T_{gate}}{\alpha}} + \overline{I_{gate_0}}$	$\overline{I_{gate_0}} = 3.13 * 10^{-10}\ A$ $A = 0.09475\ A$ $\alpha = 1.03E - 10$	0.99564
	T_{pd} Vs T_{gate}	$T_{pd} = \frac{a*b*(T_{gate})^{(1-c)}}{1+b*(T_{gate})^{(1-c)}}$	$a = 5.10110^{10}$ $b = 1.50110^{75}$ $c = -7.49133$	0.99913
NOR2	$\overline{I_{gate}}$ Vs T_{gate}	$\overline{I_{gate}} = A * e^{\frac{-T_{gate}}{\alpha}} + \overline{I_{gate_0}}$	$\overline{I_{gate_0}} = 3.53 * 10^{-10}$ $A = 0.08227\ s$ $\alpha = 1.05 * 10^{-10}$	0.99998
	T_{pd} Vs T_{gate}	$T_{pd} = \frac{a*b*(T_{gate})^{(1-c)}}{1+b*(T_{gate})^{(1-c)}}$	$a = 6.99 * 10^{-10}\ s$ $b = 1.22 * 10^{+71}$ $c = -7.02216$	0.99847

software.

7. Effect of load variation on gate leakage and delay

With an increase in the gate dielectric constant there is a concomitant increase in the intrinsic load of the gate itself. The gate has to drive this load along with the external load that it is subjected to. In this section we study the effect of load variation on the gate. We considered three values of dielectric constant, SiO_2 ($\kappa = 3.9$) which forms the base case for comparison, Al_2O_3 ($\kappa = 9$) which is a gate dielectric of intermediate strength and HfO_2 ($\kappa = 25$) which is a very high-κ gate dielectric. This gives us a scope to examine the impact of variation of κ over a wide range and the load that the high-κ gate can sustain.

In the experiment the loading condition is changed keeping the other design and process parameters constant. This was done for each of the three dielectrics under consideration. The loading condition is incorporated in the form of a "Load Factor" multiplied to the

Table 3. Curve fitting for effect of variation in value of supply voltage of logic gates. Parameters with no units indicated are dimensionless.

Gates	Attributes	Fitting Functions	Function Parameters	Corr. Coeff
NAND2	$\overline{I_{gate}}$ Vs V_{DD}	$\overline{I_{gate}} = A * e^{\frac{V_{DD}}{\alpha}} + \overline{I_{gate_0}}$	$\overline{I_{gate_0}} = -2.47 * 10^{-08}\ A$ $A = 4.76 * 10^{-9}\ A$ $\alpha = 0.20795\ V^{-1}$	0.99996
	T_{pd} Vs V_{DD}	$T_{pd} = A * e^{\frac{-V_{DD}}{\alpha}} + T_{pd_0}$	$T_{pd_0} = 1.92 * 10^{-10}\ s$ $A = 4.21 * 10^{-9}\ s$ $\alpha = 0.16781\ V^{-1}$	0.99903
NOR2	$\overline{I_{gate}}$ Vs V_{DD}	$\overline{I_{gate}} = A * e^{\frac{V_{DD}}{\alpha}} + \overline{I_{gate_0}}$	$\overline{I_{gate_0}} = -2.98 * 10^{-8}\ A$ $A = 5.56 * 10^{-9}\ A$ $\alpha = 0.20583\ V^{-1}$	0.99996
	T_{pd} Vs V_{DD}	$T_{pd} = A * e^{\frac{-V_{DD}}{\alpha}} + T_{pd_0}$	$T_{pd_0} = 2.66 * 10^{-10}\ s$ $A = 7.11 * 10^{-09}\ s$ $\alpha = 0.16822\ V^{-1}$	0.99925

intrinsic load of the gate (C_{gg}) and is varied over a range of 1-100. This enabled us to investigate the characteristics of high-κ gates (which themselves have a higher intrinsic load) over a wide range of load conditions.

From the results, it is observed that the loading in the scenario of a high-κ gate has no, or limited effect on the gate current. It can be seen from figure 8(a) that for a given dielectric constant the gate tunneling current remains almost constant for large loads of the order of a hundred times the intrinsic capacitance of the gate. When the load is too high the tunneling current gradually decreases.

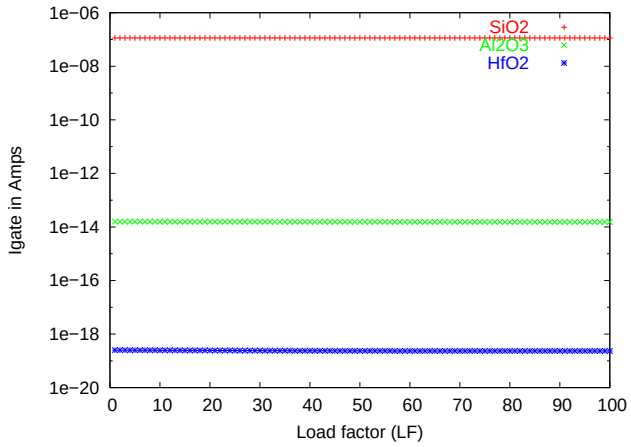
However there is a significant change in the delay of the logic gates as the load on the logic gates is increased, keeping all other parameters constant. This is shown in figure 8(b). For our base case, with SiO_2 as the gate dielectric, the propagation delay increases very gradually throughout the range of load from 1 to 100 times C_{gg}. In the case of gate dielectrics with still higher values of κ, like Al_2O_3 and HfO_2 the logic gate becomes *increasingly slower*. So at a higher load the response of the gate becomes very slow and the gate needed more time to change states. The results become more and more obvious in the case of HfO_2 where we can see a sharp increase in the propagation delay. It has also been observed from our experiments that, at a very high value of dielectric constant and a very high load of the order of 500-600 times the intrinsic load of the gate, *the logic gate simply stops working*.

This shows that there is a variation of intrinsic load itself when we change the gate dielectric. With an increase in the permittivity of gate dielectric there is an increase in the intrinsic load of the logic gate. There is hardly any effect on the gate tunneling current with load variations irrespective of a gate dielectric. However there is a significant increase in the delay of the logic gate at a higher dielectric constant and a high value of load.

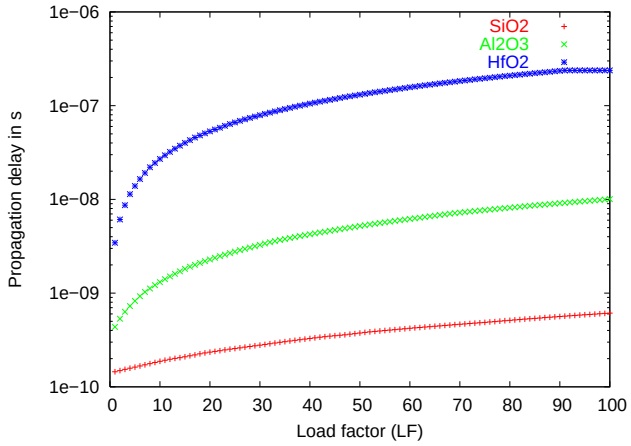
8. Applications to library characterization and high level synthesis

In the previous sections we presented extensive modeling and characterization of NAND2 and NOR2 gates in terms of their performance as a function of dielectric material (κ), gate material thickness (T_{gate}) and power supply (V_{DD}). In this section we will present a comparison of the standard logic gates (INV, NAND2, NOR2, AND2 and OR2) in terms of gate leakage current and propagation delay. This allows the quantification of the effect of new dielectric materials on cell library characterization, and the investigation of novel algorithms in high level synthesis using these libraries.

Table 4 compares the gate leakage current (hence leakage power) and propagation delay for the standard logic gates constructed using two different dielectric materials: SiO_2 ($\kappa =$



(a) I_{gate} Vs Load Factor



(b) T_{pd} vs load factor

Figure 8. Effect of load variation for various dielectrics on a 2-input NAND gate.

3.9) vs. SiON ($\kappa = 5.7$). The values given are dependent on the input state, shown as "00", "01", "10" and "11" in the table. Details of the characterization methodology are given in Mukherjee et al. (2005). The tradeoff between leakage power consumption and delay is clear. Judicious use of both types of gates (dual-κ technology) can result in digital systems that have substantial reduction in leakage power, with minimal impact on timing. In Mohanty (2008) we have demonstrated leakage reduction of the order of 68% when using a SiO_2-SiON dual-κ library.

Table 4. Characterization of Gate Leakage Current and Delay for Various Logic Gates. Parameters with no units indicated are dimensionless.

	$\kappa = 3.9$ (SiO_2)					$\kappa = 5.7$ (SiON)				
	I_{gate} in $nA/\mu m$				T_{pd} in ps	I_{gate} in $nA/\mu m$				T_{pd} in ps
	00	01	10	11		00	01	10	11	
INV	100.4	252.0	-	-	129.6	0.262	0.770	-	-	241.3
NAND2	55.8	172.0	35.8	247.6	256.9	0.134	0.506	0.029	0.754	495.3
NOR2	102.1	128.5	121.3n	246.6	378.2	0.260	0.382	0.375	0.755	680.3
AND2	179.6	295.7	160.0	298.5	350.0	0.513	0.885	0.409	0.887	741.3
OR2	225.4	179.6	171.8	297.7n	340.3	0.640	0.513	0.501	0.885	697.0

Such characterized libraries can be used to obtain analytical expression for quality met-

rics of functional units (such as adders, subtractors, multipliers etc.) for a given high-κ technology. In Mohanty et al. (2006) we investigated the performance of such functional units as a function of κ. The results are shown in Table 5.

Table 5. Gate Leakage and Delay as Analytical Functions of κ. Parameters with no units indicated are dimensionless.

Functional Unit	$I_{gate}(\mu A) = A * e^{\left(\frac{-K}{\alpha}\right)} + I_{gate_0}$			$T_{pd}(ns) = \begin{cases} A_2 + \frac{A_1 - A_2}{\left(1+e^{\left(\frac{K-K_0}{dK}\right)}\right)}, & 2.5 \leq K < 6 \\ C * e^{\left(\frac{-K}{\alpha}\right)} + T_{pd_0}, & 6 \leq K < 30 \end{cases}$					
	$I_{gate_0}\,(\mu A)$	$A\,(\mu A)$	α	$A_1\,(ns)$	$A_2\,(ns)$	K_0	β	α	$T_{pd_0}\,(ns)$
Adder	-1.20	2.53	0.36	5.06	63.22	4.02	0.47	-10.63	0.37
Subtractor	-1.34	2.83	0.36	5.06	63.22	4.02	0.47	-10.63	0.37
Multiplier	-16.10	33.81	0.36	8.07	100.74	4.02	0.47	-10.63	0.37
Divider	-24.80	52.08	0.36	27.43	342.32	4.02	0.47	-10.63	0.37
Register	-0.95	2.00	0.36	5.93	74.01	4.02	0.47	-10.63	0.37
Multiplexer	-0.81	1.70	0.36	0.28	3.59	4.02	0.47	-10.63	0.37
Comparator	-2.85	5.99	0.36	6.50	81.21	4.02	0.47	-10.63	0.37

Applications of these results are given in Mohanty and Pradhan (2009) where high-κ functional units have been used in a tabu search high level synthesis algorithm and in Ghai et al. (2009) where a complete logic library is statistically characterized using the techniques presented here.

9. Conclusions and future work

We presented the characterization of two crucial process (κ_{gate}, T_{gate}) parameters and one design (V_{DD}) parameter of the tunneling effect and propagation delay of logic gates having various high-κ gate dielectrics. It was observed that the NAND gate had minimal gate leakage and propagation delay among all the logic gates under consideration for the same experimental conditions.

We performed a further analysis of the inter-dependence of these parameters and used the data to derive curve-fitting parameters. The resulting fitting equations provide an excellent approach towards modeling the various process and design parameters of advanced nanoscale CMOS devices with high-κ gate dielectrics. We propose that the data from the characterization and modeling equations provides an excellent means for the design of novel and complex low-leakage CMOS devices involving high-κ dielectrics and provides valuable information to estimate the effect of gate leakage and propagation delay which can then be used to characterize entire cells and libraries.

Our research in this field is ongoing. As a first phase, we experimented based on compact models (BSIM4) and SPICE simulations. However, we are in the process of adopting two different approaches to thoroughly validate the data. Initially, a first principle physics based approach will be used, followed by TCAD based simulations.

10. Acknowledgments

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