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RESEARCH ARTICLE

A Variability Tolerant System-on-Chip Ready Nano-CMOS Analog-to-Digital Converter

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As integrated circuit technologies progress to nanoscale, process variations become relatively large and significantly impact circuit performance. The proactive management of process variation during the design process is critical to ensure effective device yield and to keep manufacturing costs down. In the present scenario, designers are searching for analog-to-digital converter (ADC) architectures which are nanoscale CMOS processes tolerant. Expectations on the performance of ADCs are continuously increasing along with the progress of digital systems. A process and supply variation tolerant, System-on-Chip (SoC) ready, $1GS/s$, 6 bit flash ADC suitable for integration into nanoscale digital CMOS technologies is presented. The physical design of the ADC has been done using a generic $90nm$ Salicide $1.2V$/$2.5V$ 1 Poly 9 Metal process design kit. Baseline post layout simulation results at nominal supply and threshold voltages are presented. The parasitic-extracted physical design of the ADC is then subjected to a corner based methodology of process variation. The results show that process variation causes a maximum variation of 10.5% in the INL and 5.7% in the DNL, with both INL and DNL being less than $0.5LSB$. The $90nm$ ADC consumes a peak power of $5.794mW$ and an average power of $3.875mW$. The comparators for the ADC have been designed using the threshold inverting technique. To show technology scalability of the design, the ADC has also been presented using $45nm$ Predictive Technology Models (PTM). At $45nm$, $INL = 0.46LSB$, $DNL = 0.7LSB$ and a sampling rate of $100MS/s$ **were obtained**. The $45nm$ ADC consumes a peak power of $45.42\mu W$, and average power of $8.8\mu W$.

Keywords: Flash ADC, TI Comparator, Low Voltage, High Speed, Process Variation, Nano-CMOS, SoC

1. Introduction and Motivation

The analog-to-digital converter (ADC) is an essential circuit in System-on-a-Chip (SoC) designs which bridges the gap between the analog and digital world as an interfacing element. Mixed-signal applications such as image sensors [Fossum (1997)], wireless applications and medical monitoring devices need high-speed ADCs which are commonly implemented using the flash architecture. High speed ADCs are also applied for the integration of low data rate radio frequency (RF) analog circuit components for complete SoC technology based applications. Typically, Megasample (MS/s) ADCs are required in digital cameras, video capture cards, and TV tuner cards to convert full-speed analog images to digital image files [Li et al. (2005)], which are available as SoCs [Okada et al. (1999)]. A high-level block diagram of such a digital camera is shown in figure 1 [RIM (2006)].

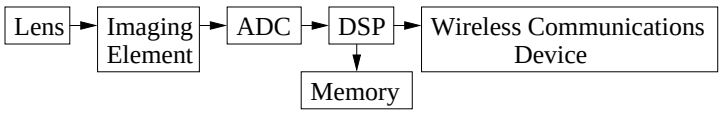

Figure 1. Block diagram of a typical digital camera.

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Semiconductor designers are facing numerous challenges as they migrate their existing designs or start new designs in $90nm$, $65nm$ and finer process geometries. One of the biggest challenges is the potential yield loss caused by increasing process variations. Designing for yield is an afterthought in today's design flows, whether they are digital, analog, radio frequency (RF), or mixed-signal. The lack of design for yield tools has forced the digital world to accept overly pessimistic guardbands as the norm. Just as in digital design where interconnect delays make or break a design, the move to $90nm$ and lower process technologies means that the variations in process parameters have a resounding effect on the performance metrics of analog, mixed-signal, memory, and RF circuits. IP core providers are faced with the challenge of meeting analog performance in a technology that has been targeted for digital logic. New circuit design techniques that accommodate lower supply voltages necessary for portable systems also need to be integrated into the IP core. Systems that once worked at $3.3V$ or $2.5V$ now need to work at $1.8V$ or lower, without any performance degradation. The need for greater processing speed has designers taking advantage of smaller device geometries. Smaller devices provide higher packing density and lower overall power consumption, due to lower parasitics and lower supply voltages. This shortening of the minimum channel length has resulted in the reduction of power supply voltage to the $1V - 0.7V$ range.

The SoC trend also forces analog circuits to be integrated with digital circuits. To keep up with the scaling of the minimum channel length and SoC trend, ADCs need to be operated at low voltages, especially in portable devices. However, the minimum supply voltage for analog circuits predicted in the semiconductor road map [ITRS (2006)] does not follow the digital supply voltage reduction. Analog supply voltages between $1.8V$ and $2.5V$ are still being used with channel lengths of $0.18\mu m$ and $0.13\mu m$ [Sandner et al. (2005)]. Hence, it is a great challenge to design a low supply voltage operating ADC while considering the relatively high threshold voltage of short channel length transistors. Another important consideration for an SoC is that the analog, mixed-signal circuits should be designed using a standard CMOS digital process, without necessarily having process options such as deep N-WELL or on-chip inductors or varactors.

Analog circuits contain matched transistors [Pelgrom et al. (1989)]. The threshold voltage (V_t) of a MOSFET is the gate voltage required to induce a channel for current flow through the transistor. Matched CMOS transistors are designed to be identical. During fabrication, the threshold voltage of a CMOS transistor is engineered to a desired voltage using processing, where ion-implanted charges are employed to shift the threshold voltage. This processing step is called threshold voltage adjustment implant. The fluctuations of this process results in fluctuations in threshold voltage as a function of transistor area. Additionally, variations in lithography result in small geometric inaccuracies. The variation of V_t increases as the transistor area decreases. It is the relative variation of the threshold voltages between two transistors rather than their absolute voltage values that is of interest for the majority of applications. Also, power supply voltage variations in analog circuits need to be accounted for, to verify their SoC readiness.

In summary, the demand for emerging application-specific, nanoscale mixed-signal SoCs which need process (threshold voltage mismatch) and power supply voltage variation tolerant ADC interfacing circuitry, and the development of mature nano-CMOS processing technology is the motivation behind this research.

The organization of the paper is as follows: Contributions of this paper are presented in section 2. Section 3 discusses related research. The logical transistor level as well as physical design of the $90nm$ ADC is presented in section 4. Simulation and characterization of the ADC is presented in section 5. Section 6 discusses the corner based methodology applied for variability analysis and the effects on the circuit attributes. Section 7 discusses the design of the ADC at the $45nm$ node. Section 8 presents the simulation results and characterization. Conclusions and future research are presented in Section 9.

2. Contributions of This Paper

The *novel contributions* of this paper are follows:

(1) The logical design of a $90nm$ low-voltage and low-power consuming ADC is presented.
(2) The physical design of the ADC is presented using a digital nano-CMOS process, thus showing its suitability for SoC integration.
(3) The ADC has been subjected to a corner-based methodology for process variation and the results are presented. These results are obtained from a parasitic extracted physical design making them comparable to silicon results.
(4) The ADC is subjected to supply (V_{dd}) variation and the results are presented.
(5) To show the scalability of the design with technology, **the ADC is also presented** at $45nm$ technology.

A low supply voltage ($V_{dd} = 1.2V$) has been used for the ADC design. Power dissipation (including gate-oxide leakage, subthreshold leakage and dynamic power) of the ADC circuit with a nominal $100fF$ load reveals that the proposed ADC consumes minimal power.

The *circuit design issues* that **were** faced during the design of the ADC can be summarized as follows:

(1) Reduction in power supply voltage (V_{dd}) leads to reduction in dynamic power dissipation as it is proportional to V_{dd}^2 [Baker (2005)]. Hence, low V_{dd} results in a low-power design. The first issue is that lower V_{dd} puts a constraint on the size of 63 voltage quantization levels for the 6 bit ADC that **are presented** in this paper. An LSB value of $1mV$ has been chosen to meet this requirement. More details are given in Section 4.
(2) The second concern is that the initial physical design exhibited an $INL > 1LSB$, which is unacceptable. Such INL degradation is due to IR drop in the power supply and ground lines. To counter the IR drop, power and ground buses have been populated with a large number of contacts (figure 5). This reduced the INL to $0.344LSB$. IR drop is also reduced by generous use of substrate contacts and N-WELL ties.
(3) The third concern is electromigration risk, which has been countered by widening the power and ground buses (figure 5).

3. Existing Prior Research

The ADC is a bottleneck in SoC design. As the technology scales to nanometer, there is need for more improvement in terms of speed, area, noise immunity and adaptability to digital processes. Recent ADC literature deals with issues of comparator offset cancelation [Donovan and Flynn (2002)], using capacitive interpolation to eliminate power-hungry resistive ladders [Rong et al. (2007), Sandner et al. (2005)] or simplifying the comparator design [Tseng and Ou (2004)]. In [Chang et al. (2008)], the authors propose the active interpolation technique to reduce the input capacitance of the ADC and the amount of calibration circuit. In [Scholtens and Vertregt (2002)], an average termination circuit has been proposed to reduce power consumption. The metastability problem at high sampling speeds has been addressed in [Uyttenhove and Steyaert (2000)]. The SoC integration problem faced by ADCs has not been given sufficient attention. In [Yoo et al. (2003)], the authors propose a solution using the threshold inverting technique. **In [Song et al. (2000)], a low voltage ($1V$) operating ADC is proposed**, but the technology is not nano-CMOS. Low voltage ADC designs generally need to use either voltage-boosting techniques [Abo and Gray (1999)] or low-threshold processes [Mutoh et al. (1996)].

Table 1 provides a broad overview of the ADCs in the current literature. The overview

has been narrowed down to flash type architecture based ADCs. It can be seen that the proposed ADC is suitable for nanoscale CMOS SoCs with superior INL and DNL performance and is a low-voltage, low-power, high-speed design. The simulation results of the $90nm$ ADC presented in this paper have been obtained using a parasitic extracted physical design and hence are of *comparable accuracy* to silicon data.

Table 1. Broad overview of 6-bit flash ADCs

Research Works	Tech. (nm)	DNL (LSB)	INL (LSB)	V_{dd} (V)	Power (mW)	Rate GS/s	Type of Data
Geelen [Geelen (2001)]	350	< 0.7	< 0.7	3.3	300	1.1	Experimental
Uyttenhove [Uyttenhove and Steyaert (2000)]	350	–	–	3.3	–	1	Experimental
Tseng [Tseng and Ou (2004)]	250	< 0.1	< 0.4	2.5	35	0.3	Simulation
Yoo [Yoo et al. (2001)]	250	–	–	2.5	66.87	1	Simulation
Donovan [Donovan and Flynn (2002)]	250	–	–	2.2	150	0.4	Experimental
Scholtens [Scholtens and Vertregt (2002)]	180	–	0.42	1.95	328	1.6	Experimental
Chang [Chang et al. (2008)]	180	< 1.1	< 1	1.8	550	1	Experimental
Sandner [Sandner et al. (2005)]	130	< 0.4	< 0.6	1.5	160	0.6	Experimental
This Work	90	0.459	0.344	1.2	3.875	1	Simulation
	45	0.70	0.46	0.7	8.8μ	0.1	Simulation

4. Design of the ADC for 90nm CMOS Technology

A high level representation of the 6-bit ADC [Yoo et al. (2003)] is shown in figure 2. To achieve a high sampling rate, a flash architecture is chosen. The input to the ADC is an analog voltage and the output is in the form of digital codes. An n-bit ADC requires $2^n - 1$ comparators which collectively form the comparator bank. The output of the comparator bank is a thermometer code. The position of the meniscus (the 1-0 transition) represents the analog input and is determined by the thermometer decode circuit, which consists of "1 of n" code generators. The "1 of n" code generators generate a "1 of n" code which is converted to binary code using the NOR ROM. Hence, the output of the ADC is in the form of a 6-bit binary code.

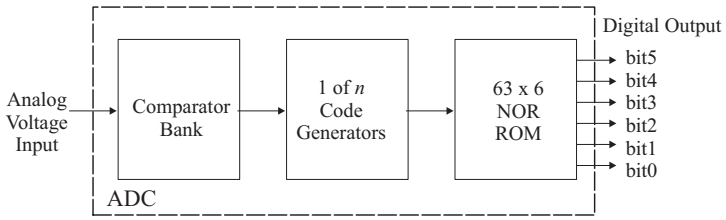

Figure 2. Block diagram of the flash ADC.

4.1 *Comparator Design*

The comparators in the proposed flash ADC have been designed using the threshold inverting (TI) technique [Yoo et al. (2001), Lee et al. (2002)]. The TI comparator has the advantage of high speed and simplicity [Lee et al. (2002)]. There is no need for inherently complex high-gain differential input voltage comparators and additional resistor ladder circuit [Stanoeva and Popov (2005)].

The TI comparator sets its switching threshold voltage $V_{\text{switching}}$ internally as the built-in reference voltage, based on its transistor sizes. In the TI based ADC, all comparators have transistors of unique sizes. For an n-bit ADC, $2^n - 1$ different comparators **are required**, each having a different $V_{\text{switching}}$ value. Hence, a total of 63 comparators for

a 6-bit ADC, each having different size of transistors is required. A suitable expression to determine the $V_{\text{switching}}$ **(in** V**)** is given by [Baker (2005)]:

$$V_{\text{switching}} = V_{dd} \times \left(\frac{R_{nmos}}{R_{nmos} + R_{pmos}} \right), \tag{1}$$

where R_{nmos} and R_{pmos} are the effective switching resistances **(in** Ω**)** for short-channel NMOS and PMOS transistors **and** V_{dd} **is the power supply voltage (in** V**).** R_{nmos} is calculated using the following expression:

$$R_{nmos} = \left(\frac{V_{dd}}{W_{nmos} \times v_{sat} \times C^*_{ox} \times (V_{\mathbf{gs}} - V_{tnmos} - V_{DS,sat})} \right), \tag{2}$$

where W_{nmos} = NMOS width **(in** nm**)**, v_{sat} = carrier saturation velocity **(in** nm/sec**)**, C^*_{ox} = gate oxide capacitance per unit area **(in** F/nm^2**)**, and V_{tnmos} = NMOS threshold voltage **(in** V**)**. R_{pmos} is defined in a similar fashion. For brevity the equation for R_{nmos} (equation 2) **is presented**. It can be observed that the switching resistance of a transistor is dependent on the width (W) of the transistor. The width of the PMOS (W_{pmos}) transistor in the TI comparator **was varied** in order to achieve the 63 different switching voltages. The channel length L is kept constant throughout the design and only W is varied. A good input voltage is determined using the following equation:

$$\text{Input Voltage Range} = V_{dd} - (V_{tnmos} + |V_{tpmos}|). \tag{3}$$

The input voltage **was chosen** to vary from $493mV$ (V_{start}) to $557mV$ (V_{end}). The LSB value V_{LSB} **(in V)** is calculated as follows:

$$V_{LSB} = \left(\frac{\text{Input Voltage Range}}{2^n} \right) = \left(\frac{V_{end} - V_{start}}{2^n} \right). \tag{4}$$

In the above expressions, the V_{LSB} value is calculated to be $1mV$ for this design. V_{LSB} signifies the minimum step the ADC can distinguish. The sizes of NMOS transistors in the comparator are kept constant at $240nm/120nm$ (W_{nmos}/L_{nmos}). For determining the sizes of PMOS transistors, a DC parametric sweep **was performed** using an analog simulator, where the input DC voltage is varied from $493mV$ to $557mV$ in steps of $1mV$. During this simulation, L_{pmos} has been kept at $120nm$ while W_{pmos} is varied from $240nm$ ($W_{pmos} = W_{nmos}$) to $448nm$ (in steps of $1nm$) in order to obtain 63 linear quantization voltage levels. The TI comparator consists of four cascaded inverters, as shown in figure 3. Inverters 1 and 2 form the baseline comparator, while inverters 3 and 4 provide increased gain and sharper switching.

4.2 *"1 of n" Code Generator Design*

The output of the comparator bank is a thermometer code. This thermometer code is converted to a "1 of n" code using "1 of n" code generators. A single slice of "1 of n" code generator consists of AND gates as combinations of an inverter followed by a NAND gate. The output from each of the AND gates is fed to the input of the NOR ROM. One of the two inputs to the AND gate is fed from the TI comparator output [Choudhury and Massiha (2004)]. The other input to the AND gate is the inverted output from the next level comparator as shown in figure 4.

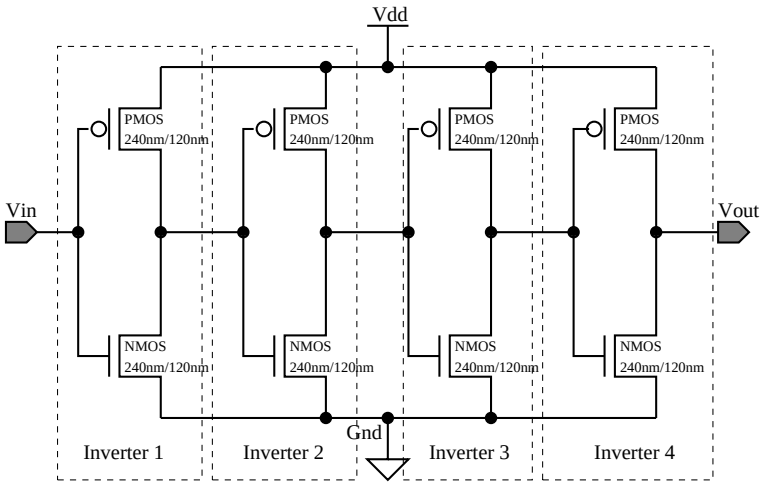

Figure 3. **TI comparator architecture used in this paper.**

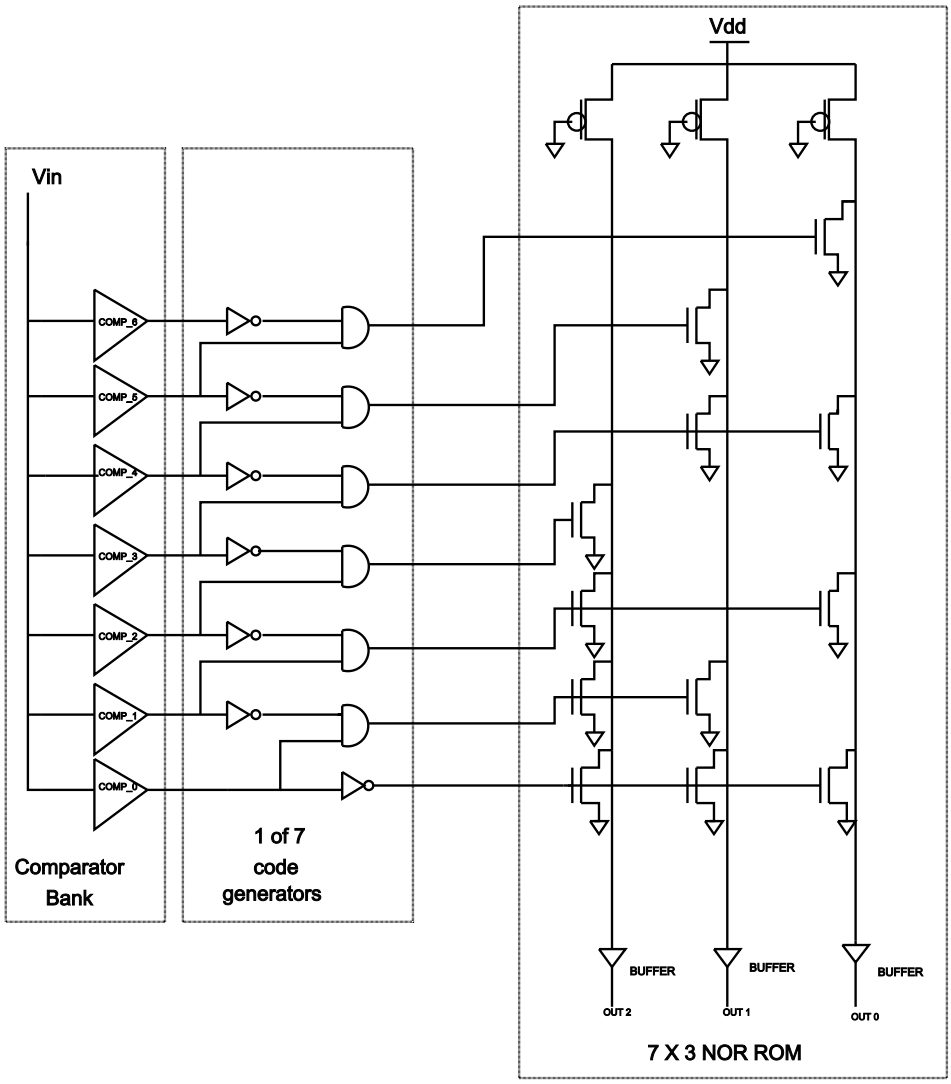

Figure 4. **Complete circuit diagram of a 3-bit flash ADC.**

4.3 *NOR ROM Design*

The input to the NOR ROM is a "1 of n" code. The NOR ROM converts this "1 of n" code to a binary code. Basically, the NOR ROM maps the n-bit address input onto arbitrary values of m-bit data output. It consists of a grid of word lines (the address input) and bit lines (the data output), selectively joined together with transistor switches. It can represent an arbitrary look-up table with a regular physical layout. As **there are** 63 word lines and 6 bit lines, a 63×6 NOR ROM **was designed**. The NOR ROM consists of PMOS pull-up and NMOS pull-down devices. The PMOS and NMOS sizes have been taken as $135nm/180nm$ and $180nm/180nm$, respectively. A design decision of $W_{pmos} < W_{nmos}$ has been taken to obtain a good voltage swing at the output so that the pull-up device (PMOS) is narrow enough for the pull-down devices (NMOS) to pull the output down safely [Rabaey et al. (2003)]. Finally, buffers are applied at the outputs to obtain symmetrical waveforms, with equalized rise and fall times. The buffer consists of two cascaded inverters having NMOS size of $240nm/120nm$ and PMOS size of $480nm/120nm$.

4.4 *Physical Design*

The physical design of the ADC has been carried out using a generic $90nm$ Salicide "1.2V/2.5V 1 Poly 9 Metal" process design kit. A digital CMOS process **was used** for the physical design of the ADC to demonstrate SoC readiness. The three major blocks of the flash ADC, namely the comparator bank, the "1 of n " code generator and the NOR ROM have been laid out column-wise. The overall layout is shown in figure 5. The post layout simulation results are presented in subsequent sections. Power and ground routing is comprised of wide vertical bars, as can be seen from the layout, giving minimal electromigration risk and IR drop. Generous use of contacts to the power and ground buses also ensures small IR drop and improved INL and DNL.

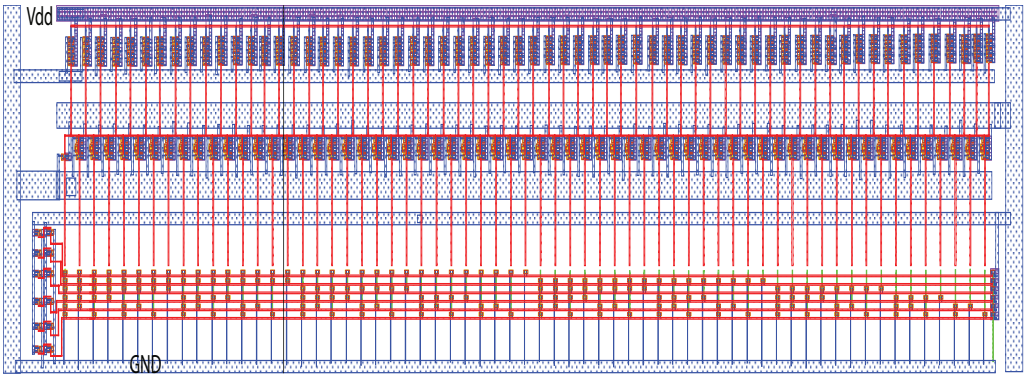

Figure 5. Complete layout of the $90nm$ ADC.

5. Simulation and Characterization of the Proposed 90nm ADC

5.1 *Post-Layout Functional Simulation*

Figure 6 shows the functional simulation of the ADC, obtained from the parasitic extracted layout. A transient analysis is carried out, where a linearly varying ramp covering the full scale range of the ADC is given as input. Output digital codes from 0 to 63 are obtained correctly, with no missing codes. A maximum sampling speed of $1GS/s$ **is observed**. All 64 codes of the ADC are covered as the input voltage ramp traverses the full-scale range.

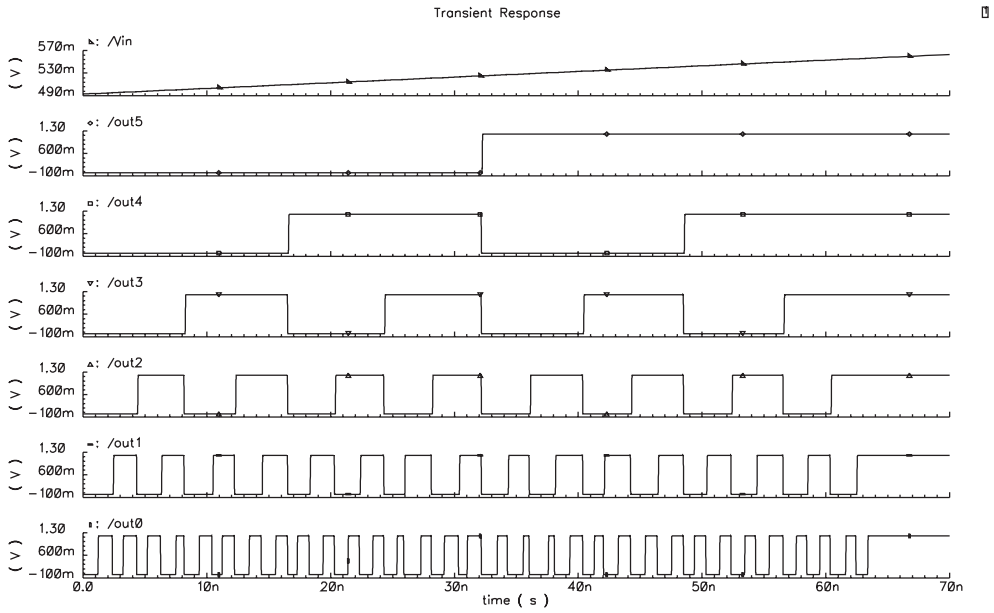

Figure 6. Functional simulation of the 6 bit ADC operating at $1GS/s$.

5.2 *Baseline Characterization*

The ADC has been characterized for Integral Non-Linearity (INL) and Differential Non-Linearity (DNL). The INL and DNL tests have been performed with nominal supply and threshold voltages to confirm satisfactory results before the ADC is subjected to variability analysis. Also, a power consumption analysis of the designed ADC circuit has been performed.

The proposed 6-bit ADC's INL and DNL have been measured using the histogram method [Max (2008)]. **In the methodology followed in this design**, the INL and DNL calculating blocks are Verilog-A modules. The Verilog-A block generates a voltage 'vout', which is sequentially set to 4096 equally spaced voltages between V_{start} and V_{end}, which is the input voltage range for ADC conversion (Section 4). At each different value of 'vout' a clock pulse is generated causing the ADC to convert this 'vout' value. The resultant code of each conversion is stored. When all the conversions have been performed, the INL and DNL **(in multiples of** V_{LSB}**)** are calculated from the recorded data as follows:

$$INL[i] = width[i] + INL[i-1] - 1, \tag{5}$$

$$DNL[i] = width[i] - 1, \tag{6}$$

$$width[i] = \frac{1.0 * bucket[i]}{hits * (NUM_{CODES} - 2)}, \tag{7}$$

where $bucket$ holds the number of code hits for each code and $width$ holds the code width calculations. The total hits between codes 1 and 62 is denoted as $hits$. NUM_{CODES} is the number of codes, 64 for a 6-bit ADC. **The quantities** $bucket$**,** $width$**,** $hits$ **and** NUM_{CODES} **are dimensionless.** For the designed ADC, the maximum INL obtained is $0.344LSB$ and the maximum DNL is $0.459LSB$. Any information of variation of the gain of ADC with V_{dd} is contained in the variable $hits$ (equation 7). Figure 7 and figure 8 show the INL and DNL plots, respectively, for the ADC. Low distortion requires an

ADC with low INL. Also a $DNL < 1LSB$ ensures a monotonic transfer function for the ADC.

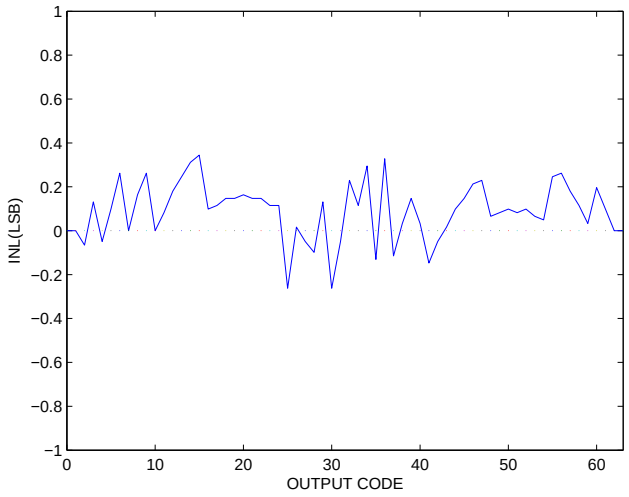

Figure 7. Integral Non-Linearity (INL) plot of the ADC.

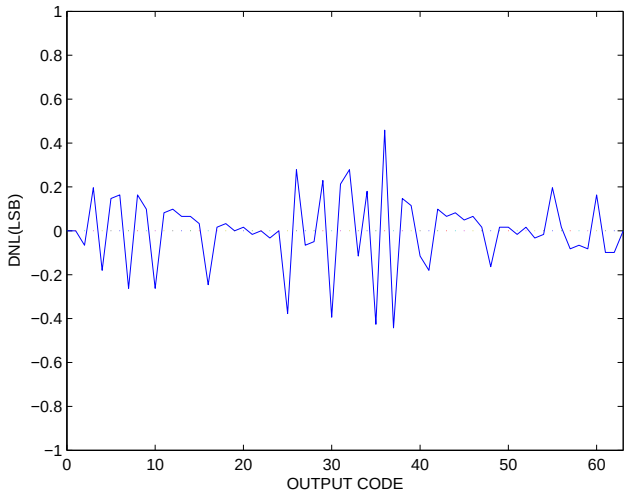

Figure 8. Differential Non-Linearity (DNL) plot of the ADC.

5.2.1 Power Analysis

Power analysis of the ADC was performed with a capacitive load of $100fF$ [Mohanty et al. (2007)]. The ADC consumes a peak power of $5.794mW$ and an average power of $3.875mW$, which satisfies the lower bound on power consumption [Svensson et al. (2006)]. The power dissipation of different components of the ADC as well as overall power dissipation of the ADC is presented in Table 2. It can be seen that the comparator bank consumes almost all the power. A power-saving scheme could be introduced to turn off the unused TI comparators, which is currently on-going research. The instantaneous power plot of the ADC is shown in figure 9. The plot has a parabolic nature with peak power at the middle of the conversion process. This is because most of the comparators are turned on at the middle voltage, (Input Voltage Range)/2. The summary of the measured performance of the ADC is shown in Table 3. As the ADC design is taking place at

nanometer scale, the total power of the ADC can be expressed as the sum of significant components as follows:

$$P_{ADC} = P_{dyn} + P_{sub} + P_{gate}, \tag{8}$$

where P_{dyn} is the dynamic power, P_{sub} is the subthreshold leakage, P_{gate} is the gate-oxide leakage consumed by all transistors in the ADC, **and P_{ADC} is the total power consumed by the ADC, all in W.**

Table 2. Componentwise power consumption of ADC.

Component	Average Power (mW)
Comparator Bank	3.68125 (95%)
1 of n code generators	0.03875 (1%)
NOR ROM	0.155 (4%)
Total	3.875

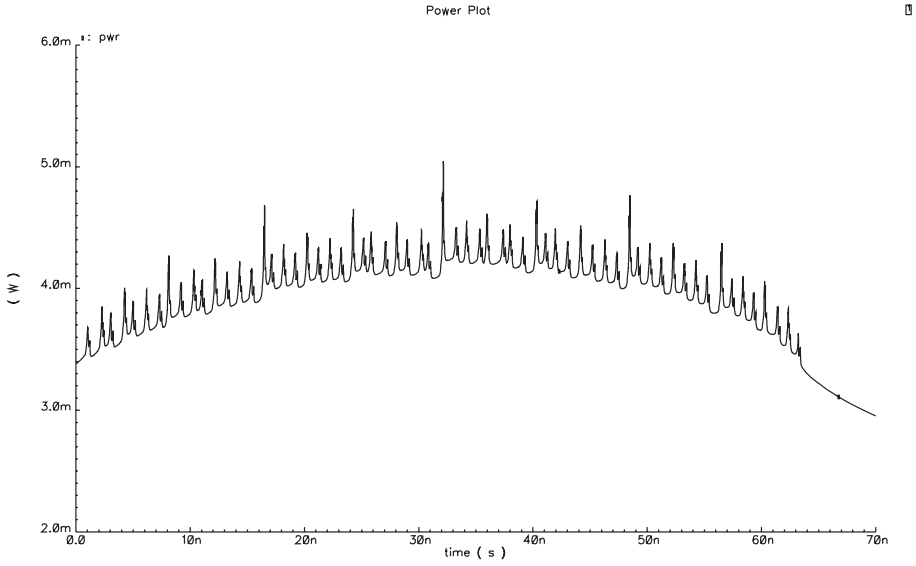

Figure 9. Instantaneous power plot (accounting for dynamic power, subthreshold leakage, and gate-oxide leakage) of ADC with a load capacitance of $100fF$.

Table 3. ADC performance with nominal supply and threshold voltages

Parameter	Value
Technology	$90nm$ CMOS $1P\ 9M$
Resolution	6 bit
Supply Voltage (V_{dd})	$1.2V$
Sampling Rate	$1GS/s$
INL	$0.344LSB$
DNL	$0.459LSB$
Peak Power	$5.794mW$@$1.2V$
Average Power	$3.875mW$@$1.2V$
Input Voltage Range	$493mV$ to $557mV$
V_{LSB}	$1mV$

The dynamic power can be represented as follows:

$$P_{dyn} = \eta \times C_L \times V_{dd}^2 \times f, \tag{9}$$

where P_{dyn} is the dynamic power (in W), η is the activity factor (dimensionless), C_L is the load capacitance (in F), V_{dd} is the power supply (in V) and f is the frequency of operation (in Hz). Due to the quadratic relationship between P_{dyn} and V_{dd}, a lower V_{dd} leads to lower dynamic power dissipation.

The subthreshold leakage current in a transistor is represented as follows [Fotty (1997), Sill et al. (2007)]:

$$I_{sub} = \alpha \times \exp\left(\frac{V_{gs} - V_t}{S v_{therm}}\right) \times \left(1 - \exp\left(\frac{-V_{ds}}{v_{therm}}\right)\right), \tag{10}$$

where $\alpha = \left(\mu_0 \times \left(\frac{\epsilon_{ox} W}{T_{ox} L_{eff}}\right) \times v_{therm}^2 \times e^{1.8}\right)$. **$I_{sub}$ is given in A, V_{gs} and V_{ds} are the gate-to-source and drain-to-source voltages, respectively (in V), V_t is the threshold voltage of the device (in V), v_{therm} is the thermal voltage (in V) and S is the subthreshold shape factor/subthreshold swing coefficient (dimensionless). The pre-factor α has units of A, μ_0 is the carrier mobility (in $m^2/(V \times sec)$), W, L_{eff} and T_{ox} are the width, effective length and oxide thickness, respectively, of the device (all in m) and ϵ_{ox} is the oxide permittivity (in F/m).** The subthreshold leakage current is exponentially dependent on the threshold voltage (V_t).

The gate-oxide leakage current density J_{ox} **(in A/m^2)** of a device can be represented as follows [Mohanty and Kougianos (2006)]:

$$J_{ox} = A\left(\frac{V_{ox}}{T_{ox}}\right)^2 \times exp\left(\frac{-B\left(1 - \left(1 - \frac{V_{ox}}{\phi_{ox}}\right)^{\frac{3}{2}}\right)}{\left(\frac{V_{ox}}{T_{ox}}\right)}\right), \tag{11}$$

where A **(in A/V^2)** and B **(dimensionless)** are technology dependent factors. **V_{ox} is the voltage drop across the device's oxide (in V), T_{ox} is the oxide thickness (in m) and ϕ_{ox} is the oxide barrier height (in V).**

6. Corner Based Methodology for Variability Characterization

The impact of the variations in the process parameters and operating conditions on the performance factors of a design is much higher for today's nanometer than the sub-micron technologies of the past. Hence, the nominal operating point, which is the center of the distribution of the parameters for a given process, may not be the best operating point for design yield. A corner based method **is proposed** that covers the process spread with a minimum number of simulation runs. Process and supply variation in an ADC is a critical issue. Process variation is a static problem and supply variation is a dynamic problem. The ADC has been tested for the effects of threshold voltage mismatch and supply voltage variation on the INL and DNL. It is assumed that $V_{\text{switching}}$ is not sensitive to variation in the length of the transistors (L_{pmos}, L_{nmos}), because the effective switching resistances of transistors are not dependent on their lengths (equation 2). Hence the effect due to device mismatch can be modeled to some degree by the effect of threshold voltage mismatch. The methodology is shown in figure 10. The NMOS threshold voltage (V_{tnmos}) and the PMOS threshold voltage (V_{tpmos}) were varied by $\pm 5\%$ from their nominal values specified in the process design kit (PDK), and the INL, DNL and input voltage range

values were recorded. The results have been summarized in Table 4. The INL shows a variation from $+0.2\%$ to $+10.5\%$ and the DNL shows a variation from $+2.2\%$ to $+5.7\%$. The corners are defined as:

- Corner 1: V_{tnmos} -5%, V_{tpmos} -5%
- Corner 2: V_{tnmos} -5%, V_{tpmos} $+5\%$
- Corner 3: V_{tnmos} $+5\%$, V_{tpmos} -5%
- Corner 4: V_{tnmos} $+5\%$, V_{tpmos} $+5\%$

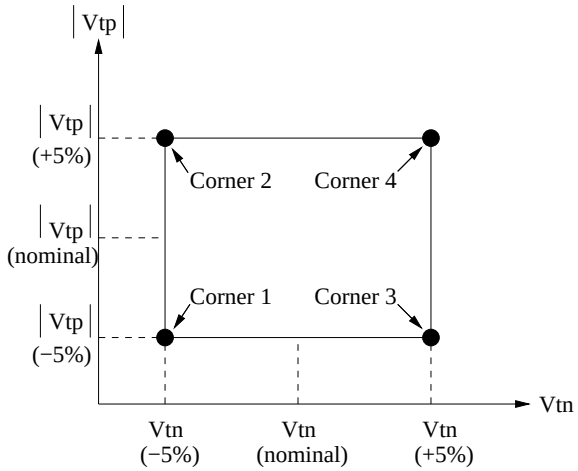

Figure 10. Corner based methodology used for process variation study.

Table 4. Process variation results

PMOS threshold voltage, NMOS threshold voltage	Input Voltage Range (mV)	V_{LSB} (mV)	INL (LSB)	DNL (LSB)
V_{tp}(nominal),V_{tn}(nominal)	493-557	1	0.344	0.459
Corner 1	491-556	1.015625	0.345	0.477
Corner 2	501-566	1.015625	0.38	0.479
Corner 3	500-564	1	0.36	0.485
Corner 4	495-557	0.96875	0.333	0.46

The results reveal that while the INL and DNL values are within control, there is a shift observed in the input voltage range. Consequently, the V_{LSB} value also changes. To overcome this shift, one may add a programmable pre-amplifier to the input signal of the ADC, thereby adjusting the signal offset and amplitude [Tseng and Ou (2004)], or digital signal processing may be performed on the ADC which is suitable for SoC applications as an on-chip processor may be present. The corner based method may not be as accurate as traditional Monte Carlo simulations which are very time consuming, but it is very useful in getting a quick estimate of the impact of process variation on circuit's behavior.

For the supply voltage variation, the nominal supply voltage ($1.2V$) has been varied by $\pm 10\%$, and the INL and DNL and input voltage range values have been recorded, as shown in Table 5. Any information of variation of the gain of ADC with V_{dd} is contained in the variable $hits$ 7. The INL shows a variation of -1% to $+4\%$ and the DNL shows a variation of $+1.8\%$ to $+4.8\%$. It can be observed that the INL and DNL values are satisfactory (INL, $DNL < 0.5LSB$). Hence **it is concluded** that the ADC is process and supply variation tolerant [Ghai et al. (2008)]. These variation studies have been carried out on the physical design of the ADC considering the effect of parasitics, hence they are *highly accurate* and comparable to silicon results.

Table 5. Supply voltage variation results

V_{dd} (V)	Input Voltage Range (mV)	V_{LSB} (mV)	INL (LSB)	DNL (LSB)
$1.08V(-10\%)$	448-500	0.8125	0.359	0.467
$1.2V$(nominal)	493-557	1	0.344	0.459
$1.32V(+10\%)$	537-614	1.203	0.339	0.481

7. Transistor Level Design and Characterization of the ADC at $45nm$ Technology

To demonstrate the scalability of the proposed ADC with technology, it **was built and characterized** at $45nm$ technology [Ghai et al. (2007)]. The block diagram of the ADC remains the same as described earlier in Section 4 but the device sizes and the supply voltage change according to the technology used. The simulation and characterization details of ADC at $45nm$ technology are discussed in this Section. Simulated with the $45nm$ Predictive Technology Model, the results demonstrate $INL < 0.5LSB$ and $DNL < 0.8LSB$. The threshold inverting (TI) technique is used with W_{pmos}/ $W_{nmos} < 1$ for many transistors in order to keep the power consumption as low as possible. The ADC shows a peak power consumption of $45.42\mu W$ and an average power consumption of $8.8\mu W$ while operating on a power supply voltage of $0.7V$. Due to unavailability of a process design kit for $45nm$ technology, the physical design is not presented.

The methodology followed for choosing the comparator sizes was the same as for $90nm$ technology. However, a suitable power supply of $0.7V$ for $45nm$ design [ITRS (2006)] has been chosen. Also the channel length of the transistors has been reduced accordingly. Using equation 3, the input voltage range was chosen to vary from $296.3mV$ (V_{start}) to $328.3mV$ (V_{end}). The V_{LSB} value is calculated to be $500\mu V$ (equation 4). In this case, W_{nmos}/L_{nmos} =$90nm$/$90nm$ and L_{pmos}=$90nm$ was kept constant throughout the design, while W_{pmos} was varied from $51nm$ to $163nm$, to get 64 quantization levels, $500\mu V$ apart. The experimental results are presented in Table 6.

Table 6. Comparator transistor sizes for input voltage range at $45nm$ technology

$V_{switching}$	W_{pmos}/L_{pmos}	W_{nmos}/L_{nmos}
$296.3mV$ (V_{start})	$51nm/90nm$	$90nm/90nm$
$327.8mV$ (V_{end})	$163nm/90nm$	$90nm/90nm$

The basic structure of NOR ROM remains the same as the $90nm$ design. However, at $45nm$, W_{pmos}/L_{pmos} = $75nm$/$90nm$ and W_{nmos}/L_{nmos} = $90nm$/$90nm$ have been used.

8. Functional Simulation and Characterization of the ADC at $45nm$ Technology

The functional simulation and characterization of the ADC at $45nm$ **technology are discussed in this section** [Zhao and Cao (2006)].

8.1 *Functional Simulation*

An instantaneous plot of the functional simulation of the ADC is shown in figure 11. Output codes from 0 to 63 are obtained with no missing codes. In this design, a maximum sampling speed of $100MS/s$ has been obtained. This is sufficient for target applications such as digital cameras [Adeniran et al. (2004)].

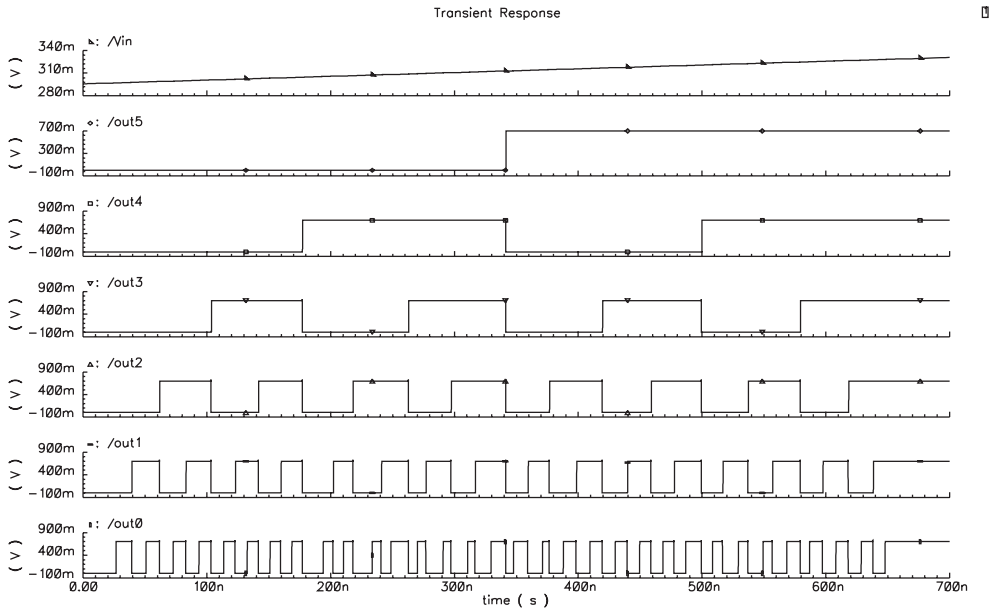

Figure 11. Functional simulation of ADC at $45nm$ node.

8.2 *Characterization*

The ADC has been characterized for INL and DNL. Also the peak and average power consumption have been evaluated.

The histogram method has been used to calculate INL and DNL. The INL and DNL plots of the ADC are shown in figures 12 and 13, respectively. The ADC is observed to have maximum $INL = 0.46LSB$ and maximum $DNL = 0.7LSB$.

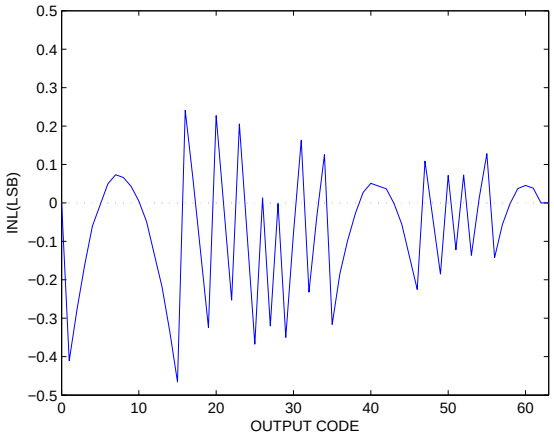

Figure 12. INL plot of ADC at $45nm$ node.

The ADC is observed to consume peak power = $45.42\mu W$, and average power = $8.8\mu W$. The instantaneous power plot of the $45nm$ ADC is shown in figure 14. The complete performance summary of the $45nm$ ADC has been tabulated in Table 7.

9. Conclusion and Future Research

The design of a process and supply variation aware low voltage, high speed flash ADC suitable for video applications **is presented**. The design has been functionally verified and

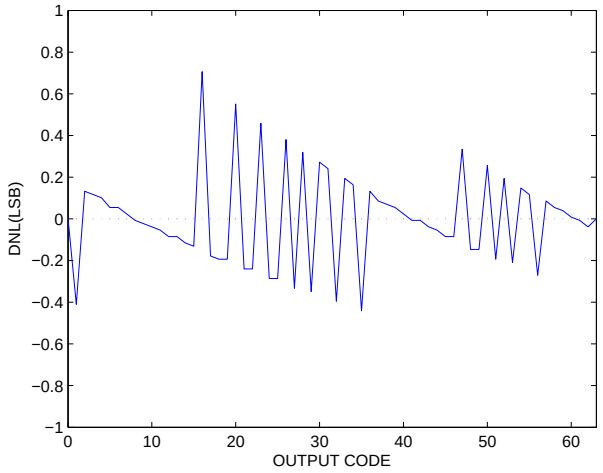

Figure 13. DNL plot of ADC at $45nm$ node.

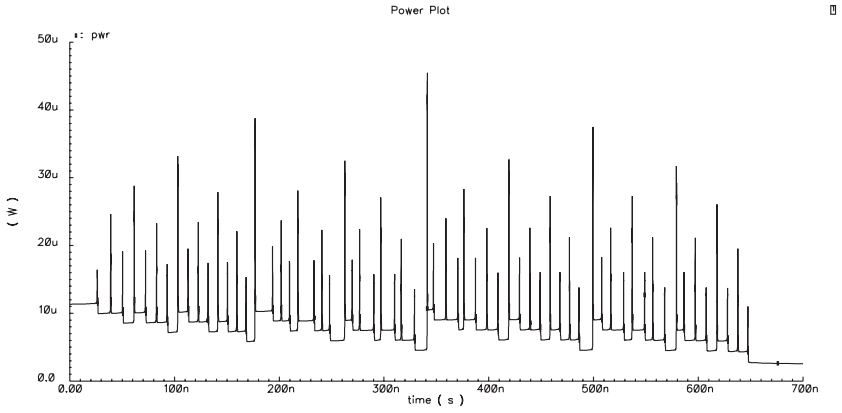

Figure 14. Instantaneous power plot of ADC at $45nm$ node.

Table 7. ADC performance at $45nm$ technology

Parameter	Value
Technology	$45nm$ PTM
Resolution	6 bit
Supply Voltage (V_{dd})	$0.7V$
Sampling Rate	$100MS/s$
INL	$0.46LSB$
DNL	$0.7LSB$
Peak Power	$45.42\mu W$@$0.7V$
Average Power	$8.8\mu W$@$0.7V$
Input Voltage Range	$296.3mV$ to $328.3mV$
V_{LSB}	$500\mu V$

characterized for nanoscale CMOS feature sizes ($90nm$ and $45nm$). The physical design of the ADC is performed using a $90nm$ digital CMOS process to demonstrate its SoC readiness. The comparators have been designed using the threshold inverting technique. The nominal results at $90nm$ show that the ADC has an INL of $0.344LSB$, and a DNL of $0.459LSB$. A corner based variability analysis of the ADC has been carried out which reveals that the ADC is process variation tolerant ($INL, DNL < 0.5LSB$). The analog

supply voltage is $1.2V$. At $45nm$, the ADC exhibits $INL = 0.46LSB, DNL = 0.7LSB$ at a supply voltage of $0.7V$. This is one of the lowest published power supply values used to implement high speed ADCs. Several design issues have also been addressed, and used in the optimization procedure of the ADC, e.g. IR drop, low V_{LSB} etc. It has been demonstrated that the design of low voltage, high speed and SoC ready ADCs which are variability tolerant is possible at nanoscale. For future research, the effect of process variation on the dynamic characteristics of the ADC **will be explored**. A Monte Carlo technique will be adopted for the future variability study.

10. Acknowledgments

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