Impact of Gate-Oxide Tunneling on Mixed-Signal Design and Simulation of a Nano-CMOS VCO ⋆

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Abstract

Design optimization for performance enhancement in analog and mixed signal circuits is an active area of research as technology scaling is moving towards the nanometer scale. This paper presents an approach towards the efficient simulation and characterization of mixed signal circuits, using a $45nm$ CMOS voltage controlled oscillator (VCO) with frequency divider as a case study. The performance characteristics of the analog and digital blocks in the circuit are simulated and the accuracy issues arising due to separate analog and digital simulation engines are considered. The tremendous impact of gate tunneling current on device performance is quantitatively analyzed with the help of an "effective tunneling capacitance", which allows accurate modeling and simulation of digital blocks with almost analog accuracy. To meet the design specifications of the analog VCO using digital CMOS technology, we follow a design of experiments (DOE) approach. The functional specifications of the VCO optimized in this design are the center frequency and minimization of overall power consumption as well as minimization of power due to gate-oxide tunneling current leakage, a component that was not important in previous generations of CMOS technologies but is dominant at $45nm$ and below. Due to the large number of available design parameter (gate-oxide thickness and transistor sizes), the concurrent achievement of all optimization goals is difficult. A DOE approach is shown to be very effective and a viable alternative to standard design exploration in the nanometer regime.

Key words: Nanoscale CMOS, Gate-oxide tunneling, Gate-oxide leakage, Voltage controlled oscillator, Design of experiments

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1 Introduction and Motivation

Analog and mixed signal simulation is becoming an important component of the design cycle that affects both time-to-market and product cost of many modern electronic systems, particularly for system-on-chip (SoC) designs [1]. The operation of analog circuits is very sensitive on mismatches between the components and their dynamic range is limited by noise, offset and distortions. The situation will be further complicated when design will be performed using nanoscale CMOS transistors that are currently being used on the digital side and eventually will be used in analog circuits [2,3].

The effects of decreasing the feature size and power supply due to aggressive technology scaling has resulted in many challenges relating to mixed signal circuit design and simulation [2,3]. Technology scaling in circuits increases the leakage current and as it reaches the nanometer level, leakage current cannot be ignored in the power consumption nor the functionality of the circuits. In particular, as technology scales to $45nm$ and below, an added dimension of leakage current of traditional CMOS devices enters the picture: gate tunneling current. Its impact on the operation of digital circuits has received considerable attention [4,5], but its effects on analog circuitry is still not well understood. Thus, there is a need to develop effective ways to maintain performance and solutions related to analog design and simulation issues in modern nanometer CMOS processes as discussed in this work.

Phase-locked loops (PLLs) are essential components of typical SoCs operating in synchronous mode. Accurate frequency or time reference signals are required practically in every analog, digital or mixed-signal design and PLLs are used to provide such stable references [6]. One of the basic and important components of a PLL is the voltage controlled oscillator (VCO) [7].

VCO design involves the simultaneous satisfaction of a number of design specifications, as well as power optimization, particularly for portable applications. With the introduction of nanometer CMOS processes, geared towards low-power portable designs, an additional leakage mechanism is introduced: gate oxide tunneling current [8]. This mechanism must be carefully accounted for during the design process as it has detrimental effects on both performance and power consumption. As a consequence, the possible factors determining the performance of analog blocks, such as VCOs, increases and makes the exploration of the design space more difficult. We will demonstrate how a design of experiments (DOE) approach [9] is a powerful and viable alternative to traditional design methods.

The rest of the paper is organized as follows: Section 2 presents our contributions in this paper. Section 3 surveys literature relevant to this paper. Section 4 gives a comparative perspective between the analog and mixed signal simulation approaches. In section 5, we present the physical phenomenon of gate oxide leakage tunneling. A

VCO design is presented and SPICE simulation results confirm its functionality in section 6. In section 7 we identify the dominant factors for the performance criteria and analyze our DOE approach. Prediction equations are then derived and simultaneously optimized. Section 8 presents the design and simulation of a VCO with frequency divider. Section 9 gives an overview of the approaches considered for improving the accuracy in mixed signal simulations and quantifies the gate leakage effect. The paper is concluded in section 10.

2 Contributions of this Paper

The contributions of this paper are multi-fold, but can be grouped under two different aspects: use of DOE for designing nano-CMOS VCOs and accounting for gate-oxide leakage effect in mixed-signal design and simulation. To the best of our knowledge, this is the first time that DOE is used for the simultaneous optimization of center frequency and power consumption *with emphasis on gate tunneling leakage power*.

First we designed a voltage control oscillator with frequency divider using a $45nm$ CMOS process. We identified the primary factors affecting the performance of this design and applied a DOE approach in order to satisfy the design criteria for low-power portable applications. We then present a way of quantifying the effect of gate leakage on the operation of the frequency divider as well as means of accurately incorporating this effect into digital behavioral simulations and we also provide quantitative measures of the relative magnitude of gate leakage vs. traditional gate capacitive effects on system operation.

3 Related Research

Several VCO and PLL designs have been already presented in the literature [10]. High performance CMOS based VCO designs have been achieved using analog feedback control [11]. Low-power PLL designs can be achieved by reducing V_{dd} which is a trend identified early in analog CMOS system design [12,13]. In [14], a comparative analysis between NMOS and PMOS VCOs has been performed and it was concluded that NMOS based VCOs are beneficial in terms of high frequency and low voltage. Concepts related to jitter in ring oscillators are discussed in [15]. There are mainly two issues that were considered by the authors of [3] relating to technology scaling: gate leakage and decrease in supply voltage, which would lead to low performance of the circuit. As a solution to the above two issues the critical parts can be operated at high supply voltage by exploiting different combinations of thin and thick oxide transistors. Also the issue of gate leakage is addressed by using active cancelation techniques. They have also introduced a parameter called bias

insensitive frequency f_{gate} which is used for quick estimation of the effect of gate leakage. The authors of [16] examined the behavior of MOS devices with respect to gate leakage and analyzed the performance of common source amplifiers and current mirrors. Ring oscillator VCOs are described in [17] and [18]. Simulation aspects of ring oscillators are examined in [19]. In terms of specific VCO designs, a 20 GHz CMOS VCO is presented in [20], an optimized VCO and mixer are given in [21] and a 0.18 μm CMOS dual-band VCO is presented in [22]. Power optimization of VCOs has been discussed in [23] and [24]. Additional examples of LC-tank VCO designs are given in [25], [26], [27] and [28]. Novel resonant circuits are used in [29] and [30]. Finally, an on-chip calibration system is described in [31].

4 Analog Vs Mixed Signal Simulation: A Comparative Perspective

The main goal of today's large digital CMOS SoCs with analog components built on the same substrate is low power and high frequency of operation. The performance of SoCs is driven by the digital portion of the SoC which follows market dynamics. This can be achieved to a large extent by implementing mixed signal circuits, if the integration of both the analog and digital circuits is made efficient in terms of high frequency, low power, and small area. At the same time, analog figures of merit (such as frequency and phase noise for oscillators) can be met. Digital circuits have become predominant due to their lower power consumption and reliability [32]. As scaling takes place digital circuits have advantages but analog circuits may still be irreplaceable for high precision processing [33]. As a compromise, mixed signal circuits are considered, but these are quite difficult to design as the analog portion of the circuit depends on various metrics which are fundamentally different from the metrics of digital circuits. Low power consumption and smaller area would be the main reasons to implement mixed signal circuits rather than considering purely analog circuits. Mixed-signal circuit designs are beneficial when various techniques to design, isolate noise, and interface the analog and digital components are considered and if the whole process is optimized [34].

Simulating an entire PLL or even subsystems of it, such as the VCO, using analog (SPICE) simulations is time consuming and CPU intensive, particularly at the post-layout stage. As a solution to this, some components are simulated as analog and some as digital blocks using both analog and digital simulation engines (mixed mode simulation.) Mixed signal circuits provide improved system reliability and flexibility [35] and are a combination of analog circuits where the analog signals are continuously varying voltages, currents or frequencies and digital circuits which are discrete in nature. Due to the difference in nature of the simulation techniques and engines used for each discipline. Discrepancies can arise between the simulation results of a given block, depending on whether it is simulated in analog or digital mode. Analog simulation results are always superior but also very time consuming. A common compromise is to simulate a block in analog mode and use the results

to generate a more accurate digital model that includes loading and other second order effects, an approach followed in this work.

5 Phenomenon of tunneling through gate oxide of a Nano-CMOS Device

The continuous shrinkage of the CMOS device dimension has resulted in a corresponding scaling of gate oxide thickness as well. The scaled oxide gives rise to the phenomenon of gate oxide tunneling leakage. A brief overview of the physical phenomenon associated with tunneling leakage is presented in this section.

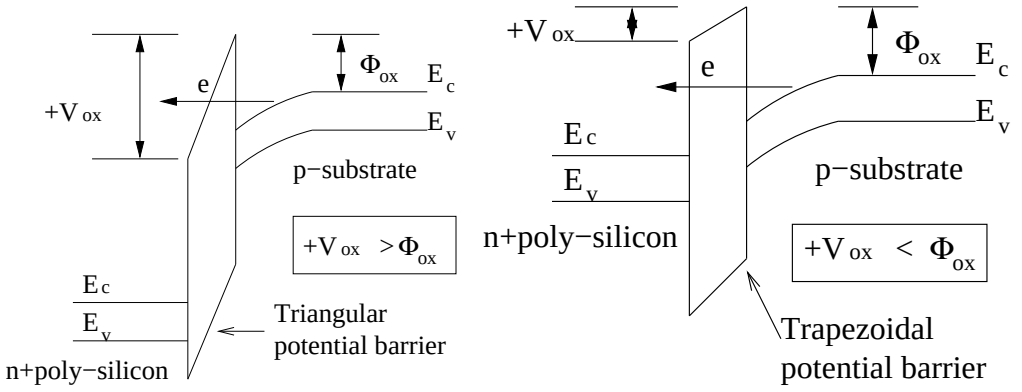
With the decrease in the thickness of the gate oxide, there is a corresponding increase in the electric field across the gate. The increase in electric field along with the decreasing physical thickness of the gate oxide results in tunneling through the oxide. Gate oxide tunneling can involve two different mechanisms, namely, Fowler-Nordheim (FN) tunneling and direct tunneling. Considering the case of only electron tunneling in a MOS with heavily doped n+ polysilicon and p-type substrate, the two tunneling mechanisms can be as shown in Fig. 1. In the case of FN tunneling, electrons tunnel through a triangular potential barrier into the conduction band of the oxide layer when $V_{ox} > \Phi_{ox}$, as shown in Fig. 1(a). FN tunneling is however very small as short-channel devices mostly operate at $V_{ox} < \Phi_{ox}$ [36]. Direct tunneling, on the other hand, is more predominant in CMOS devices with very thin gate-oxide ($< 40nm$). In the case of direct tunneling, electrons do not tunnel into the conduction band as in the case of FN tunneling, but instead they tunnel through the forbidden energy gap into the gate dielectric. Also, it can be seen from Fig. 1(b) that unlike FN tunneling, the direct tunneling of electrons occurs through a trapezoidal rather than a triangular potential barrier. The magnitude of direct tunneling current (J_{DT}) is given by the expression [8,37,38]:

$$J_{DT} = \frac{q^3 V_{ox}^2}{16\pi^2 \hbar \phi_B T_{ox}^2} * \exp\left[-\frac{4\sqrt{2m_{eff}}{\phi_B}^{1.5} T_{ox}}{3\hbar q V_{ox}} * \left\{1 - \left(1 - \frac{V_{ox}}{\phi_B}\right)^{1.5}\right\}\right], \quad (1)$$

where q is electronic charge, V_{ox} is voltage across the gate oxide, $\hbar$ is Planck's constant, T_{ox} is the electrical equivalent oxide thickness, ϕ_B is the barrier height for the gate dielectric, and m_{eff} is the effective mass of electrons.

6 Design of a Nano-CMOS VCO

The design type of VCO selected for this work is of the "current starved" type [39]. This is essentially a ring oscillator, comprised of an odd number of inverters each biased by a complementary pair of transistors operating as current sources, as



(a) FN Tunneling (b) Direct tunneling

Fig. 1. The two mechanisms of tunneling through the gate oxide in a nanoscale CMOS device [8].

shown in Fig. 2. The function of the current sources is to limit the amount of current supplied to the inverter (starve the inverter.) An additional pair of transistors acts as an input stage with very large input impedance.

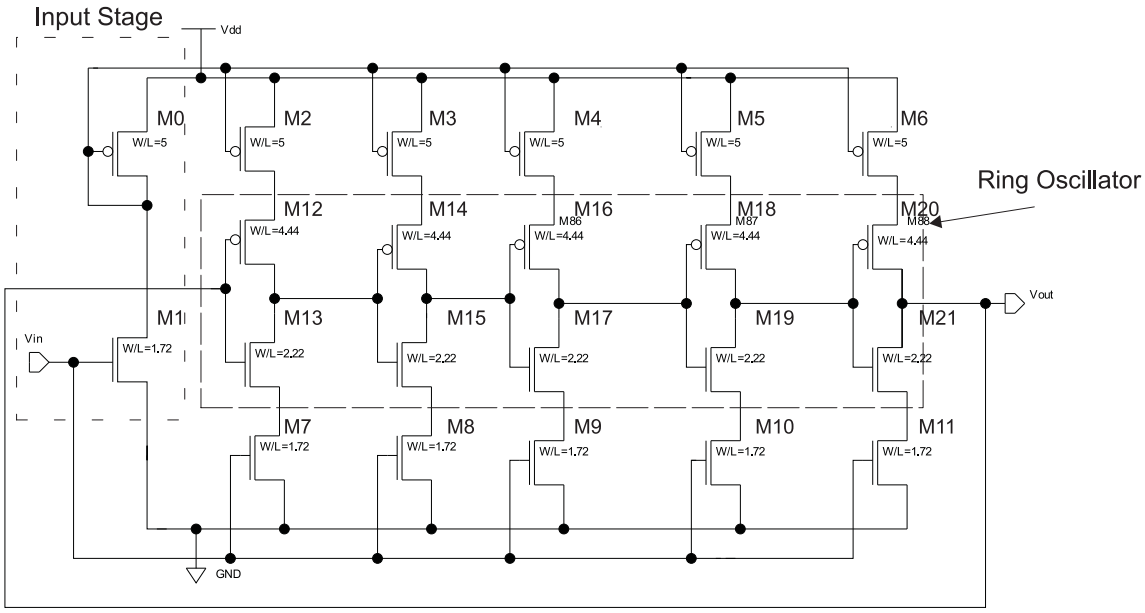


Fig. 2. Schematic diagram of the VCO. It consists of: (1) input stage (transistors M0 and M5,), (2) 5 stages of inverters (center transistors,) and (3) current starve circuitry (top and bottom transistors.)

The operating frequency of the VCO, f_o can be determined by calculating the total time it takes to charge and discharge the capacitance C_{TOT} seen by each inverter stage. Since the charging and discharging takes place during transitions, we can assume that the transistors of the inverter are in the triode region and we can write C_{TOT} as the sum of the input and output capacitances C_I and C_O:

$$C_{TOT} = C_O + C_I \tag{2}$$

$$= \hat{C}_{ox} \times (W_p L_p + W_n L_n) + \left(\frac{3}{2}\right) \times \hat{C}_{ox}(W_p L_p + W_n L_n), \tag{3}$$

which can be further simplified as:

$$C_{TOT} = \left(\frac{5}{2}\right) \times \hat{C}_{ox}(W_p L_p + W_n L_n). \tag{4}$$

In the above expressions, $\hat{C}_{ox}$ is the gate oxide capacitance per unit area, W_n, W_p are the widths and L_n, L_p are the lengths of the NMOS and PMOS transistors, respectively.

If we call I_{inv} the current that flows through the inverter when the input voltage is $V_{dd}/2$ (where V_{dd} is the supply voltage), then the frequency (at that input voltage) is given by:

$$f_o = \frac{1}{N \times T_{TOT}}, \tag{5}$$

where N is the odd number of inverters in the VCO circuit and T_{TOT} is the total time required to charge or discharge the capacitance of each stage of an inverter. T_{TOT} is the sum of two times: t_1, which is the time to charge C_{TOT} from 0 to the inverter switching point, V_{SP}, and t_2, which is the time to discharge C_{TOT} from V_{dd} to V_{SP}. Assuming that the same current, I_{inv}, flows through the PMOS and NMOS during the charging and discharging, respectively, the two times can be calculated as:

$$t_1 = C_{TOT} \times \left(\frac{V_{SP}}{I_{inv}}\right), \tag{6}$$

and

$$t_2 = C_{TOT} \times \left(\frac{V_{dd} - V_{SP}}{I_{inv}}\right). \tag{7}$$

Since $T_{TOT} = t_1 + t_2$, combining equations 5, 6 and 7, we finally have the following result for f_o:

$$f_o = \frac{1}{N \times T_{TOT}} = \frac{I_{inv}}{N \times C_{TOT} \times V_{dd}}. \tag{8}$$

The operating frequency of the VCO can be mainly controlled by an applied DC input voltage which adjusts the current I_{inv} through each inverter stage.

We used the Predictive Technology Model (PTM) $45nm$ BSIM4 models for our design [40,41]. Simulation results are shown in Fig. 3. We present gate oxide leak-

age and average power consumption of the VCO circuit in Table 1. From the table we can see that the total leakage power of the VCO due to gate oxide tunneling is a appreciable portion (almost 10%) of the total power consumed.

Table 1
Gate oxide leakage and average dynamic power dissipation of the VCO circuit. The input voltage was set at $0.7V$.

Transistor type	Transistors	Average Power (μW)	Leakage Power (nW)	Percentage (%)
Input	PMOS (M0)	12.26	0.33	0.003
	NMOS (M5)	4.69	4.82	0.1
Current Starved	PMOS (M75, M76, M77, M78, M79)	1.075	0.35	0.03
	NMOS (M80, M81, M82, M83, M84)	1.275	30.41	2.39
Inverter	PMOS (M4, M85, M86, M87, M88)	4.56	207.07	4.54
	NMOS (M92, M91, M90, M89, M62)	4.16	95.87	2.3
Total		28.02	338.85	9.36

7 Optimization of VCO via Design of Experiments (DOE)

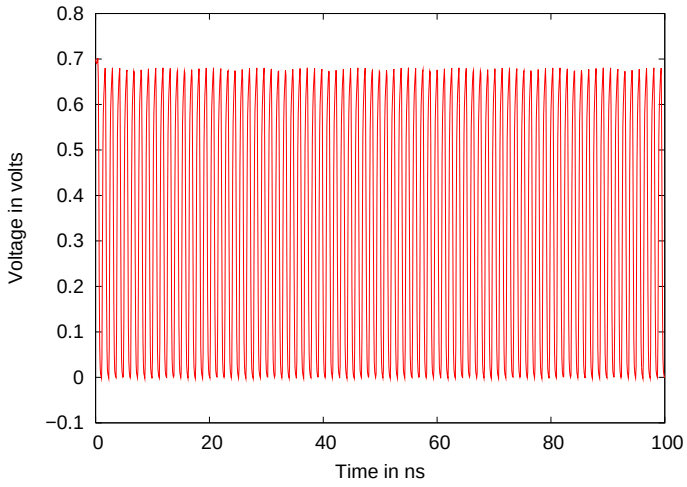
Once a baseline design has been accomplished, we proceeded to optimize its performance. Three basic performance criteria were identified: (1) The frequency response with respect to input voltage (measured by center frequency, achieved when the input voltage is equal to the supply), (2) The total power consumed by the VCO, and (3) The power consumption due to gate oxide tunneling current.

The fundamental parameters under design control are the sizing of the various transistors (W/L ratio) and the oxide thickness (T_{ox}) used in the process. Clearly higher values of T_{ox} will reduce the leakage power but will also reduce the frequency of operation. The optimization problem then becomes quite involved due to the number of variables involved:

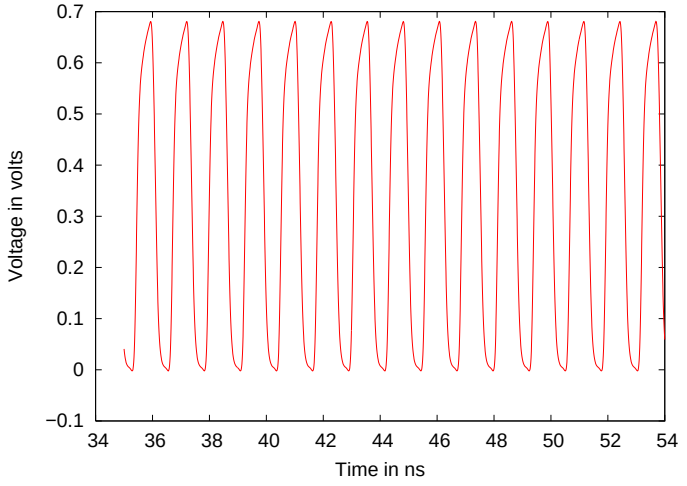
- The gate oxide thickness T_{ox}.
- $\beta_1 = \left(\frac{W}{L}\right)$ ratio for the PMOS inverter transistors.
- $\beta_2 = \left(\frac{W}{L}\right)$ ratio for the NMOS inverter transistors.
- $\beta_3 = \left(\frac{W}{L}\right)$ ratio for the PMOS current starve transistors.
- $\beta_4 = \left(\frac{W}{L}\right)$ ratio for the NMOS current starve transistors.

Thus we have 5 input factors and 3 desired responses. In a circuit of small size, an exhaustive exploration of the design space is feasible in a reasonable amount of time. We chose, however, to use a Design of Experiments (DOE) [9] approach in order to demonstrate the power of this method as well as its feasibility, particularly for large circuits.

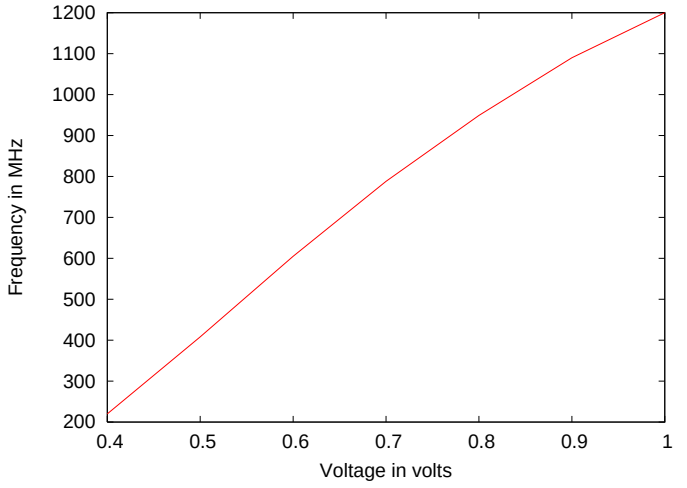
We selected a Taguchi L_8 design matrix [42] and the following upper and lower



(a) Output waveform at $V_{dd} = 0.7V$



(b) Magnification of (a)



(c) Voltage vs. Frequency response

Fig. 3. Functional Verification of the VCO. SPICE simulations were performed for $100ns$ (Figs. (a) and (b).) The input voltage was varied from $0.4V$ to $1.0V$ to obtain the VCO response (Fig. c) while V_{dd} was held at $0.7V$.

design limits:

- $1.4nm$ and $1.7nm$ for T_{ox}
- 5 and 10 for β_1 and β_3.
- 1.72 and 3.44 for β_2 and β_4.

The results are shown in Table 2. We concentrated on the center frequency when presenting the results in tabular form in order to maintain a reasonable balance between amount of data and information. The trend in frequencies below and above the center frequency is very similar and the relative magnitude of the leakage component vs. the average power remains fairly constant. From the tabular data, Pareto diagrams were generated for the three responses, as shown in Fig. 4. Based on the tabular and Pareto results, we obtain the following response equations for our design:

$$f_{osc} = 786.43 - 93.36T_{ox} + 60.3\beta_2, \tag{9}$$
$$P_{av} = 35.05 + 5.7\beta_4 + 3.3\beta_3, \tag{10}$$
$$P_{leak} = 376.35 - 28.58T_{ox} + 29.32\beta_1 + 36.17\beta_2, \tag{11}$$

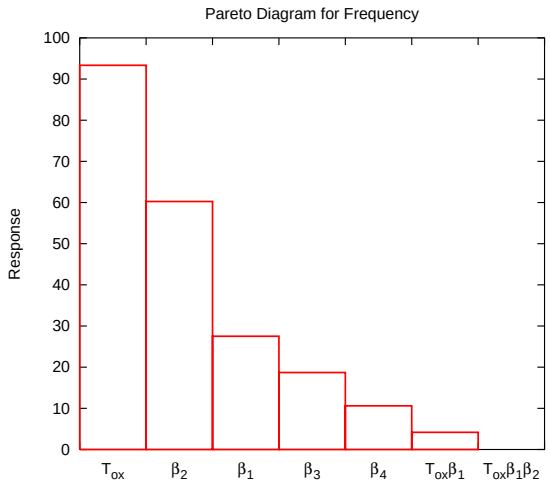
where the design variables take *coded* values from -1 (corresponding to the lower experimental value) to +1 (corresponding to the upper experimental value.)

Table 2
Experimental Results. CS refers to the current starve transistors.

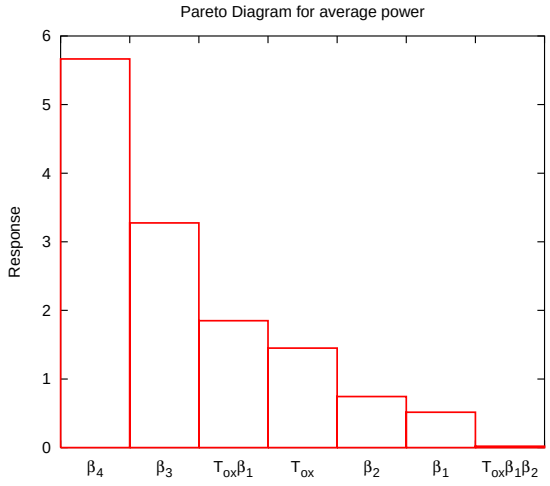
Run	T_{ox}	$\beta_1 = \frac{W}{L}$ for PMOS CS	$\beta_2 = \frac{W}{L}$ for NMOS CS	$\beta_3 = \frac{W}{L}$ for PMOS Input	$\beta_4 = \frac{W}{L}$ for NMOS Input	Freq. f_{osc} (MHz)	Corr. Coeff. $R\,(\%)$	Average Power P_{av} (μW)	Leakage Power P_{leak} (pW)
1	1.4	5	1.72	10	3.44	787.91	99.21	46	342.66
2	1.4	5	3.44	5	1.72	925.04	99.28	29.64	408.83
3	1.4	10	1.72	10	1.72	813.78	99.06	32.05	370.58
4	1.4	10	3.44	5	3.44	992.46	98.91	38.29	497.63
5	1.7	5	1.72	5	3.44	630.65	99.85	32.90	310.35
6	1.7	5	3.44	10	1.72	692.12	99.82	29.57	326.29
7	1.7	10	1.72	5	1.72	672.32	99.77	26.25	337.14
8	1.7	10	3.44	10	3.44	777.18	99.81	45.66	417.31

From Eq. 9 we see that in order to maximize the frequency of oscillation, T_{ox} must be -1 while β_2 must be +1. Similarly, from Eqs. 10 and 11 we see that average dynamic power minimization requires both β_3 and β_4 to be -1. On the other hand, leakage power minimization requires that T_{ox} must be +1 while β_1 and β_2 should be -1. All of these constraints can be satisfied simultaneously with the exception of T_{ox} and β_2. Maximum frequency of oscillation requires thinner oxide but gate leakage requires thicker oxide. Since f_{osc} is the primary design metric we select the value that maximizes it, i.e. $T_{ox} = -1$ and $\beta_2 = +1$.

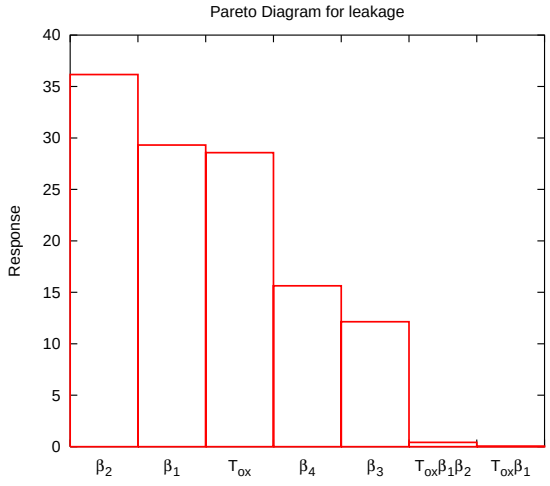
In terms of actual values we see that $T_{ox} = 1.4nm$, $\beta_2 = 3.44$, $\beta_4 = 1.72$ and



(a) Center Frequency



(b) Average Dynamic Power



(c) Average Gate Oxide Leakage Power

Fig. 4. Pareto diagrams showing the effects of various design factors on the center frequency of the VCO (Fig. a,) the total average power consumed (Fig. b,) and leakage power due to gate oxide tunneling (Fig. c.)

$\beta_1 = \beta_3 = 5$ will provide maximum frequency of oscillation, minimum total power consumption and low leakage power due to gate oxide tunneling.

8 Mixed-Signal Simulation of the VCO with Frequency Divider

Usage of nanometer CMOS VCO circuits is necessarily increasing due to their wide usage in many RF based communication systems. For different range of frequencies, different topologies can be used. In a PLL, the frequency from the VCO is changed either by changing the reference signal or the divide by ratio of the frequency divider. Due to the stability of the reference signal, a frequency divider is used which divides the frequency from the VCO, so that the frequency matches with the reference frequency from the phase detector. In this section we consider the design of a VCO with frequency divider along with the simulation approaches used to validate its performance.

The design of a nanometer CMOS VCO should take into consideration different performance issues in terms of power consumption, noise and frequency. Frequency performance is given importance in this paper. A basic block diagram of the VCO with frequency divider is shown in Fig. 5. Transistor level schematics of the VCO and the frequency divider are given in Figs. 2 and 6, respectively. The block diagram in Fig. 5 also has a purely digital block for the frequency divider which is implemented using behavioral Verilog. A loading capacitor C_{Load} is added at the input of the digital frequency divider and will be discussed in section 9.

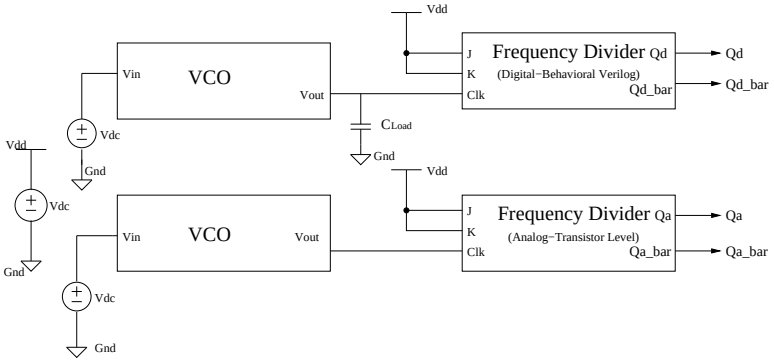


Fig. 5. Block diagram of the VCO along with an analog frequency divider and a digital frequency divider. The role of the capacitor C_{Load} is to model capacitive loading effects, as explained in the text.

8.1 Design of a base line VCO and Frequency Divider

The type of VCO considered in this work is of the current starved type presented in the previous section. The circuit has no stable operating point and it will oscillate at

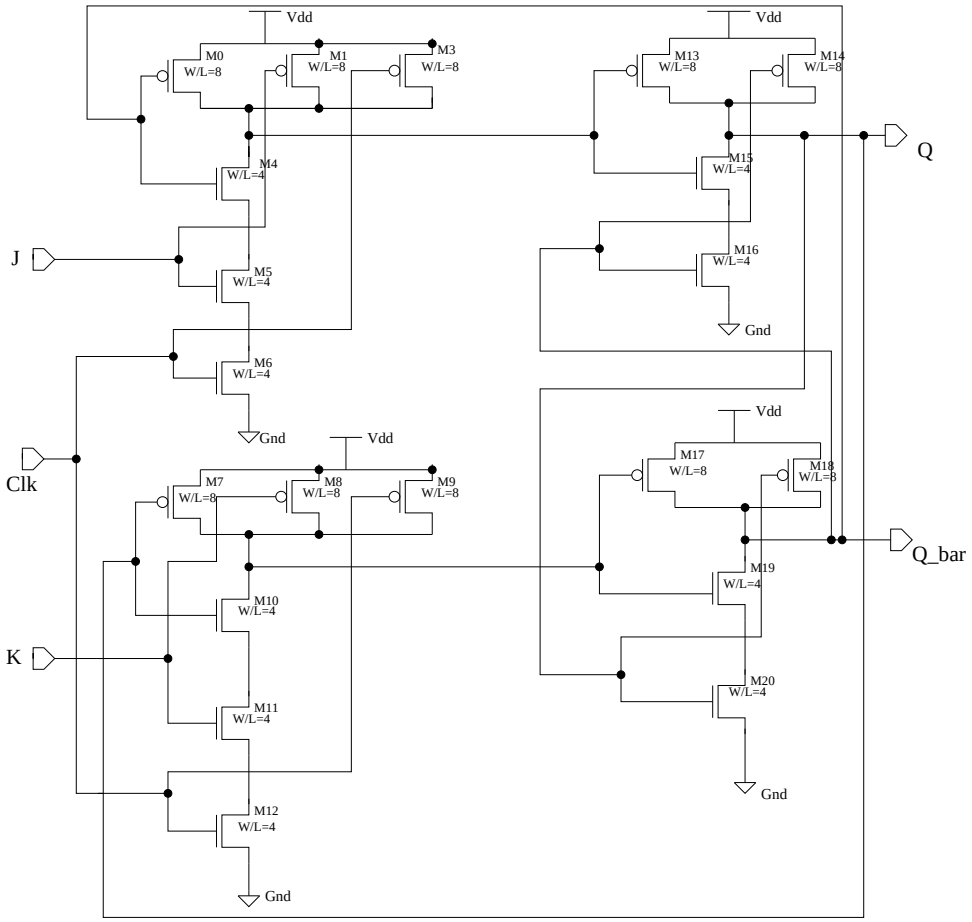


Fig. 6. Transistor level diagram of the frequency divider.

some frequency that is determined by the number of inverters, size of the transistors in the circuit, and the current flowing through the inverter which is dependent upon the input voltage to the VCO.

Next we consider the operation of the analog frequency divide which is implemented via a JK flip-flop. This circuit was built using two 3-input NAND gates and two 2-input NAND gates as shown in Fig. 6. For simulation purposes, we can also consider the frequency divider in terms of behavioral Verilog, as shown in Fig. 5.

8.2 Analog Simulation of the Circuit

The analysis of reaching a state of minimum power consumption at a particular level of performance can be done either by finding a new absolute lower limit for power consumption and using it or by examining the process performance at different levels using different parameters like supply voltage and gate oxide thickness and optimizing the circuit [43]. The analog simulation of the circuit is done by considering both the VCO and the frequency divider as analog components where the

clock output of the VCO is fed to the frequency divider whose output is again a clock but with half the frequency of the input clock as shown in Fig. 7. The SPICE models used in this work are for a $45nm$ CMOS process with gate-oxide thickness $T_{ox} = 1.4nm$ and threshold voltage $|V_{th}| = 0.22V$. The circuit has been simulated using both analog and mixed signal environments and corresponding circuit simulators.

8.3 Mixed Signal Simulation

An analog, transistor-level representation of the VCO along with a behavioral Verilog representation of the frequency divider which is digital in nature are considered for the mixed signal simulations. In this circuit the analog clock output of the VCO is fed to the digital Frequency Divider and a digital clock output with half the frequency is obtained at the output as shown in Fig. 7. To allow communication between the analog and digital components or vice versa in the mixed signal circuit, interface elements have been used and an analog to digital interface is created between the analog VCO and the digital frequency divider. The parameters related to the interface elements can be further customized: the $a2d$ interface used here considers two voltage levels, V_{low} and V_{high} below and above which the signal takes the values of LOW and HIGH, respectively and along with them is a timing parameter called TIMEX according to which a voltage level between V_{low} and V_{high} for longer than TIMEX yields a logic X (undefined). Similarly, the $d2a$ interface also has different parameters like the voltage levels, rise and fall times that can be characterized in accordance with the output required.

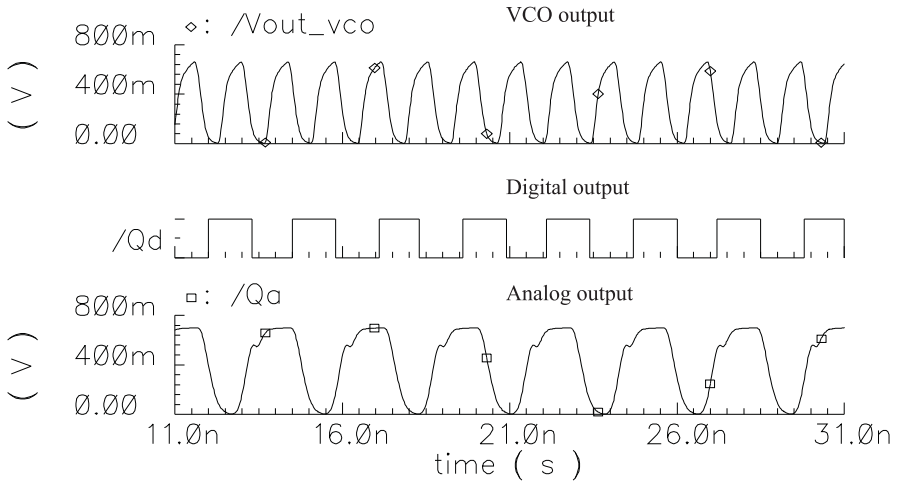


Fig. 7. Output Waveforms of the VCO, Digital Frequency Divider, and Analog Frequency Divider

9 Accuracy in Mixed Signal Simulations: Impact of Gate Leakage and Proposed Remedy

Following the different simulation modes as presented in section 8 the following operating frequencies were obtained:

$$f_{VCO} = 717.96 \quad MHz, \tag{12}$$
$$f_a = 357.9 \quad MHz, \tag{13}$$
$$f_d = 394.03 \quad MHz. \tag{14}$$

In these expression, f_{VCO} is the frequency at the output of the VCO, f_a is the frequency at the output of the analog frequency divider and f_d is the frequency at the output of the digital frequency divider.

It can be seen that there is a significant difference in the simulation results, depending on whether the frequency divider is considered as analog or digital. This discrepancy, $\Delta f = |f_d - f_a| = 36.13 MHz$, is quite large (approximately 10%) and is due to two factors: (i) regular capacitive loading of the VCO by the frequency divider and (ii) transient capacitive loading due to gate oxide tunneling current in the transistors of the frequency divider.

The nature of the transient capacitive loading can be explained by recognizing that gate leakage current is present during both ON and OFF states of a transistor. If these currents are I_{ON} and I_{OFF}, respectively, during an ON-OFF or OFF-ON transition, an effective tunneling capacitive load is then manifested, given by:

$$C_{eff}^{tun} = \left| \frac{I_{ON} - I_{OFF}}{dv_g/dt} \right|, \tag{15}$$

where v_g is the voltage applied on the gate. A thorough discussion of the nature of this capacitance and its importance in modeling nano-CMOS circuits is given by the authors of this work in [44].

In order to account for these capacitive loads, a capacitor C_{Load} is placed at the input of the frequency divider behavioral model, as shown in Fig. 5. Subsequently, an optimization was performed to minimize Δf and it was found that a value of $C_{Load} = 2.49 fF$ satisfies the minimization criterion to within 1%.

For comparison purposes, we calculated the tunneling capacitive loading of the entire frequency divider by monitoring the total gate current due to all the devices in the circuit, $i_g(t)$ and the gate voltage $v_g(t)$ and averaging over several periods of

operation, $\hat{T}$:

$$C_{eff}^{tun} = \frac{1}{\hat{T}} \int_0^{\hat{T}} \left| \frac{i_g(t)}{dv_g/dt} \right| \, dt. \tag{16}$$

This calculation yields $C_{eff}^{tun} = 2.0fF$. It is seen, therefore, that 80% of the capacitive load is due to gate tunneling and only 20% due to traditional gate capacitance.

10 Summary and Conclusions

As a result of technology scaling, there is a degradation in the performance of purely analog circuits due to gate tunneling, as discussed in this paper. An analysis of mixed signal simulations over pure analog simulations for a $45nm$ Voltage Controlled Oscillator and frequency divider was performed which clearly highlights issues in mixed signal simulations due to the additional leakage mechanism. An approach to equalize the frequency at the outputs of analog and digital blocks is given wherein a capacitive load is added before the digital block. The value of this capacitive load is predominantly determined by leakage considerations and not traditional gate capacitance. In traditional ($> 45nm$) CMOS designs its effect is minimal but at $45nm$ and below it rapidly becomes the dominant loading mechanism. The effect of the additional gate tunneling leakage component complicates the design an analog components by introducing a major power consumption factor that must be minimized, or, if total minimization is not possible, must be kept low. Instead of pursuing an exhaustive design space exploration, which is typically not feasible in medium and large designs, DOE allows the designer to reduce dramatically the number of required simulations while providing for near-optimal design. In our test VCO we demonstrated how DOE indicates that the simultaneous maximization of f_{osc} and minimization of P_{leak} are incompatible but provides a solution by minimizing P_{av} instead. Although in this work we did not study the effect of gate leakage on the VCO's phase noise, a thorough investigation at the post-layout stage is underway and will be presented in a future publication. We do note, however, that a phase noise value of -109.13 dBc/Hz at a 10MHz offset frequency is obtained without any optimization. It is anticipated, that by including a phase noise objective function in the optimization loop it will be possible to further improve this figure.

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