

# A single ended 6T SRAM cell design for ultra-low-voltage applications

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**Abstract:** In this paper, we present a novel six-transistor (6T) single-ended static random access memory (SE-SRAM) cell for ultra-low-voltage applications. The proposed design has a strong 2.65X *worst case* read static noise margin (SNM) compared to a standard 6T SRAM. A strong write-ability of logic ‘one’ is achieved, which is problematic in an SE-SRAM cell with a 36% improvement compared to standard 6T SRAMs. A  $16 \times 16 \times 32$  bit SRAM with proposed and standard 6T bitcells is simulated and evaluated for read SNM, write-ability and power. The dynamic and leakage power dissipation in the proposed 6T SRAM are reduced by 28% and 21%, respectively, as compared to standard 6T SRAM.

**Keywords:** SRAM, SNM, leakage, process variation and subthreshold design.

**Classification:** Integrated circuits

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## 1 Introduction

Lowering supply voltage to reduce power (energy) consumption is one of the first choice of designers for ultra-low-power applications. However, ultra-low-power design of high-density SRAMs in which the operating voltage is below the transistor threshold voltage is extremely challenging. This is due to reduced static noise margin (SNM) and increased variability in design and process parameters in the nanoscale CMOS (nano-CMOS) technology. As we move from 130 nm to 65 nm technology node, the area occupied by the memory increases from 71% to 82% [1]. In modern system on chips (SoCs), when total power and total area is dominated by the SRAM, reduction in  $V_{dd}$  for SRAMs can save both active energy and leakage power [2]. Also for system integration, SRAM must be compatible with subthreshold combinational logic operating at ultra-low voltages [4]. However, this leads to an increase in sensitivity of design and process parameter variability. This problem will worsen in nanometer technologies with ultra-low voltage operation and makes SRAM design and stability analysis more challenging. These practical challenges limit standard 6T SRAM cells and architectures to a higher  $V_{dd}$ .

Previously, different types of SRAM cell designs consisting of 7 to 10 transistors have been proposed to improve the data read stability and write-ability [3, 4, 5, 6, 7]. Read stability has been improved in designs [5, 6, 8] by isolating the cell nodes from the bitlines. While, write-ability in the prior designs [3, 4, 5] is enhanced by either weakening of cross-coupled inverters or routing an extra supply voltage. All these features in the prior designs leads to increase in area overhead and power (energy) consumption.

This *paper presents a novel 6T cell and its word-organization for robust, high density and ultra-low voltage SRAM cells. In the proposed 6T SE SRAM cell: (1) read current path is isolated from the data storage node Q and QB, hence, less vulnerable to noise; (2) isolation of read current path improves the read SNM  $2\times$  compared to standard 6T with cell ratio  $\beta = 2$  and at  $V_{dd} = 0.2\text{ V}$  and  $1.0\text{ V}$ ; (3) process variation degrade the read SNM of proposed 6T and standard 6T SRAM cells by up to 13% and 50% respectively thereby,  $2.65\times$  tolerance to process variability; (4) 36% improvement in write-ability is achieved at  $V_{dd} = 0.2\text{ V}$ , compared to standard 6T with the help of a write assist transistor. The dynamic and leakage power dissipation in the proposed 6T design is reduced by 28% and 21%, respectively, as compared to its counterpart design because of single ended input/output feature.*

Therefore, the proposed design is a good candidate for subthreshold SRAM cells, without increasing the area overhead and power (energy) consumption.

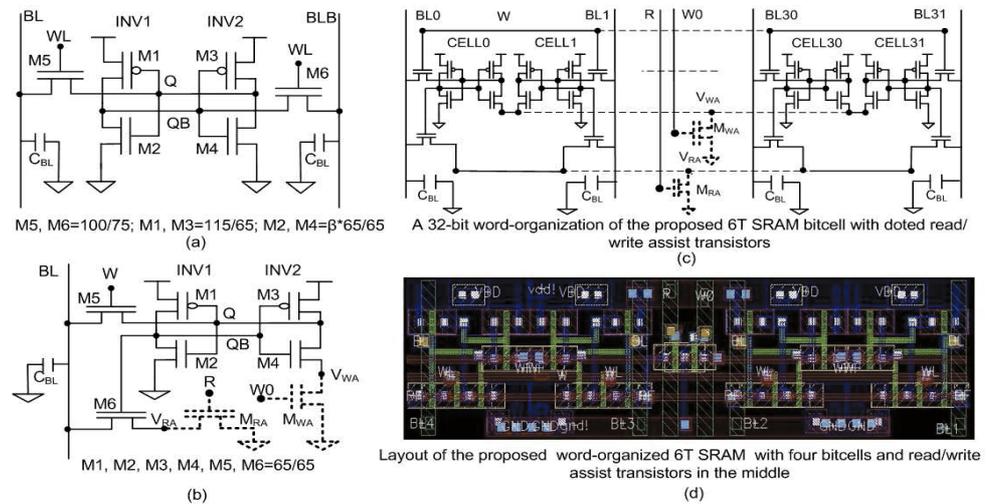


Fig. 1. The proposed single-ended 6T SRAM bitcell.

## 2 The proposed SE 6T SRAM Cell

Fig. 1 (b) presents the proposed single ended 6T SRAM cell with minimum feature sized transistors for a 65 nm CMOS technology. The proposed 6T SRAM cell consists of a cross coupled inverter pair (INV1 and INV2) connected to a bitline (BL) using access transistor (M5) and a data storage node isolation transistor (M6). The dotted transistors in the figure ( $M_{WA}$  and  $M_{RA}$ ) represent read and write assist transistors, respectively, for a memory word. Three control signals W, its complement W0 and R are used for controlling the write and read operations. The write operation is controlled by W and W0. These signals are respectively connected to M5 and  $M_{WA}$ . While read operation is controlled by R which is connected to  $M_{RA}$ . In a word-organized memory, which contains more than 1-bit per word, that is,  $n \geq 2$ , where  $n$  be the number of cells. A word-organization with proposed 6T SRAM cell for  $n = 32$ , is shown in Fig. 1 (c). Since read and write operations access the  $n$  bits of a word simultaneously, we can share the read/write assist transistors of a cell as shown dotted in Fig. 1 (b). Therefore, we need only one read/write assist transistor per word greatly reducing area overhead. Each cell in a word consists of six transistors with two additional (dotted) transistors per word [(Fig. 1 (c)]. Also, writing/reading of a word (cells) is not affected, when other word is accessed for writing/reading, because a word shares read/write assist transistors by row, not by column.

The size of read assist transistors for a word has to be chosen carefully since it forms the critical read access path, which determines the performance of a SRAM. However, write assist transistors can be a minimum sized, because its role is limited to weakening of the cross-coupled inverters during write access.

Fig. 1 (d) shows the layout of a proposed word-organized 6T SRAM cell with four bitcells and read/write assist transistors. We present only four bitcells for clarity. The proposed cell layout area is  $0.68 \mu\text{m}^2$  ( $0.55 \mu\text{m} \times 1.22 \mu\text{m}$ ), which is 8% higher (because of additional contacts) than the standard 6T cell for  $\beta = 2$ . In comparison, the read/write assist transistors occupy merely half of the cell area per word. We have used three metal layers (M1, M2 and M3). Metal layer M1 is used for routing the supply rails ( $V_{dd}$  and  $G_{nd}$ ), M2 is used for routing the shared contacts among cells, read and write signals, while M3 is used for routing the bitlines. The design has been successfully laid-out on silicon for different word sizes. Parasitic were extracted and included in a SPICE deck for simulation results presented in this paper.

## 2.1 Read Operation

Data read out from the proposed SRAM cell is sent via a single ended bitline (data-line). Prior to a read operation, BL is precharged to  $V_{dd}$  and the read signal (R) is asserted high (W is low) to turn on the  $M_{RA}$ , which is needed for reading ‘0’. For reading ‘1’, BL is remains at the precharged level ( $\sim V_{dd}$ ) because transistor M6 is turned off. It is important to notice that only the read ‘0’, high to low transition is affected by the insertion of the  $M_{RA}$ , and that the read ‘1’, low to high transition will not be affected. As a result, reading ‘1’ is directly sensed from the precharged BL. In both cases, either reading ‘1’ or ‘0’, storage nodes are isolated from the read current path. This results in reduced capacitively coupled noise due to BL and hence, significantly enhancing the data stability during read and hold state. Also, compared to standard 6T cell, the read current path has an equal number (two) of series connected transistors with minimum feature sizes resulting in a better performance.

Read static noise margin (SNM) of the proposed 6T and standard 6T SRAM bitcells are shown in Fig. 2 (a)-(d) for a comparative perspective. The proposed 6T cell has an SNM of 0.302 V, while the standard 6T cell SNM is 0.152 V at a supply voltage of 1.0 V and  $\beta = 2$  [Fig. 2 (a)]. The SNM of the proposed 6T cell at a supply voltage of 0.3 V is equal to that of the standard 6T cell at 0.5 V and  $\beta = 4$  [Fig. 2 (b)]. However, the SNM normalized to supply voltage for different bitcell ratio ( $\beta = 2, 3$  and 4) in Fig. 2 (b) shows that the variation of SNM in the proposed 6T cell (for minimum feature size) is smaller than that of the standard 6T bitcell.

For process variation analysis, we assume, a 15% variation in  $V_{th}$  [1] with  $3\sigma$  as an independent random variable for all the transistors in SRAM cell with a Gaussian distribution. The variations in  $V_{th}$  degrade the read SNM of standard 6T and proposed 6T SRAM cell by up to 50% and 13% respectively compared to nominal design as shown in Fig. 2 (c) and (d). The proposed 6T SRAM cell provide 2.65X higher worst-case read SNM as compared to the standard 6T SRAM cell under same process variations. *Thus, the proposed 6T cell has better noise margin and worst-case read stability and is process variation tolerant.*

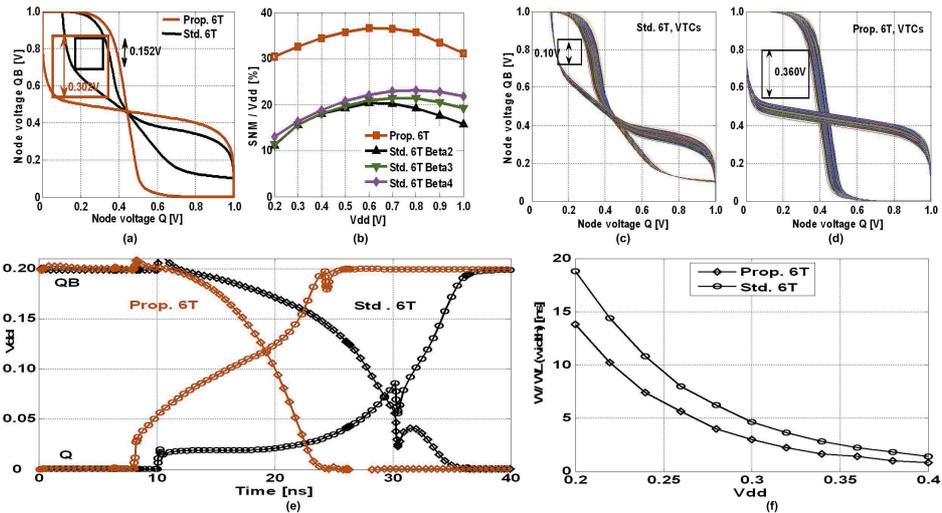


Fig. 2. Data read stability (a)-(d), write ability (e)-(f).

## 2.2 Write Operation

In Fig. 1 (b) and (c), a write assist transistor  $M_{WA}$  is used to alleviate the write problem, which is controlled by W0 for a successful write voltage operation. The usage of  $M_{WA}$  is to weaken the cross coupled inverters during write access time.

The effectiveness (write-ability) of the write operation can be analyzed from Fig. 2 (e) and (f). The write operation of a standard and proposed 6T cell at different  $V_{dd}$  and minimum word-line (W/WL) pulse widths needed for a successful operation is shown in Fig. 2 (f). The realistic simulation results reveal that the proposed design has better write-ability at lower  $V_{dd}$  than the standard 6T cell. At  $V_{dd} = 0.2 V$ , the write operation of the proposed cell is 36% faster, or equivalent to  $V_{dd} = 0.24 V$  of the standard 6T cell.

## 3 Analysis of Power and Leakage Dissipation

A  $16 \times 16 \times 32$  bit SRAM memory with 32 cells in a word using both standard and proposed 6T cell designs was simulated in SPICE, operated at a clock speed of  $1 GHz$  and  $V_{dd} = 1 V$ . The simulation results are based on the BPTM of 65 nm-technology node [9]. The dynamic power consumption of standard and proposed cells under different read and write operations is shown in Fig. 3 (a). Because the proposed cell is asymmetric, its dynamic power consumption pattern is also asymmetric. In Fig. 3 (a), operation W0\_1 stands for writing '1' into the cell while its original content is '0'. Similarly, R1\_0 stands for reading '0' from the bitcell, while its previous output was '1'. For operations W1\_1 and R1\_1, the dynamic power of proposed 6T bitcell is very low as compared to standard 6T bitcell, because both the operations are performed without dis/charging the bitline of the proposed bitcell. Under such operations pre/charged bitline can be used for future read/write operation. Alternatively, in standard cell one bitline has to discharge during these operations. However, the dynamic power for operations R1\_0 and R0\_0 in proposed 6T cell is 21% and 29% higher than the standard 6T bitcell. The

average dynamic power under different read/write operations of the proposed 6T SRAM cell is 28% lower than the standard 6T cell [Fig. 3 (a)].

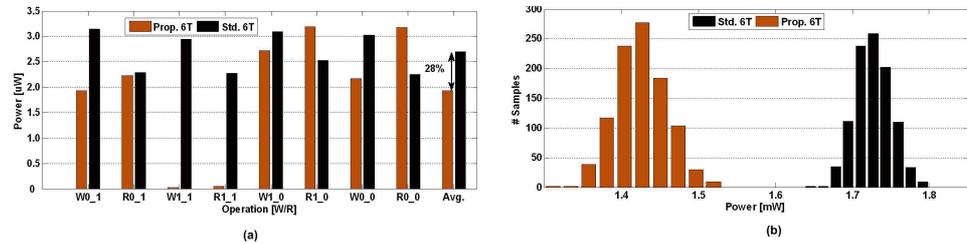


Fig. 3. (a) Dynamic power pattern and (b) leakage distribution.

A  $16 \times 16 \times 32$  bit SRAM memory using proposed and standard bitcells, was tested in a realistic simulation environment. Reading a best case word ‘1110 1110....1110’ consumes an average power of only 31% ( $3.86 \text{ mW}$ ) of the standard 6T SRAM memory because of the reuse of charged bitlines. While, reading a worst case word ‘0001 0001....0001’, it consumes 128% ( $15.94 \text{ mW}$ ) of the standard 6T SRAM memory. Reading a word with alternating values ‘1010 1010....1010’ uses only 68% ( $8.47 \text{ mW}$ ) of the standard 6T SRAM memory power.

The leakage contribution pattern of the proposed cell is also asymmetric. When node  $Q=0$ , it leaks more as compared to  $Q=1$  because the read current path transistor M6 is turned on. However, average leakage contribution in the proposed cell is 37% less than the standard bitcell. For total leakage in  $16 \times 16 \times 32$  bit SRAM memory (using proposed bitcell) in standby mode, when all the bitlines are charged to  $V_{dd}$ , access transistors (M5) of a word are cutoff and control signal read and write are clamped at ‘0’. Similarly, for standard 6T SRAM memory bitlines are charged to  $V_{dd}$ , and control signals are clamped at ‘0’. The leakage distribution under process variation for the proposed and standard SRAM memory is shown in Fig. 3 (b). The average leakage power consumption of the proposed SRAM memory is  $1.4 \text{ mW}$ , which is 21% lower than the counterpart SRAM memory.

#### 4 Conclusions

A SE-SRAM cell design and its word-organization for robust and high density SRAMs is presented. The immunity to process variations (robustness) and high density in the proposed design is achieved by isolating the read current path and using minimum feature size transistors. The improved read and write-ability (data stability), reduced dynamic and leakage power dissipation compared to standard 6T, makes the new approach attractive for nanoscale technology regime, in which process variation is a major design constraint.