Simultaneous Peak and Average Power Minimization during Datapath Scheduling

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***Abstract*— In low power design for deep submicron and nanometer regimes, the peak power, power fluctuation, average power and total energy are equally design constraints. In this work, we propose datapath scheduling algorithms for simultaneous minimization of peak and average power. The minimization schemes based on integer linear programming (ILP) are developed for the design of datapaths that can function in three modes of operation: (1) single supply voltage and single frequency (SVSF), (2) multiple supply voltages and dynamic frequency clocking (MVDFC) and (3) multiple supply voltages and multicycling (MVMC). The techniques are evaluated by estimating the peak power consumption, the average power consumption and the power delay product of selected high level synthesis benchmark circuits for different resource constraints. Experimental results indicate that combining multiple supply voltages and dynamic frequency clocking, yields significant reductions in the peak power, the average power, and the power delay product.**

***Index Terms*— Peak power, Average Power, High-level Synthesis, Datapath Scheduling, Multiple Voltages, Dynamic Clocking**

I. Introduction

The demand for the design of low power integrated circuits has escalated with the increase in chip density and clock frequency. The increasing trend has made reliability a major issue for the designers mainly because of the high on-chip electric fields [1]. Several factors such as the demand for portable systems, thermal considerations and environmental concerns have further driven the area of low power design.

The average power reduction is essential for the following reasons : (i) to increase battery life time, (ii) to enhance noise margin, (iii) to reduce cooling and energy costs, (iv) to reduce use of natural resources and (v) to increase system reliability. The battery life time is determined by the Ah (ampere hour) rating of the battery. The battery life time may reduce due to high ampere consumption. The reduction of average power is essential to enhance noise margin (to decrease functional failure). The cost of packaging and cooling is determined by the average current flow and hence by the average power (energy). The increase in energy and average power consumption, increases the energy bill ($Watt-hours$). As the energy (average power) consumption increases, it necessitates the increase in generation which in turn, escalates the usage of natural resources, affecting the environment. If the average current (power) is high then, the operating temperature of the chip increases, which may lead to failures. It is estimated that every 10^oC increase in the operating temperature roughly doubles the failure rate of the components.

Peak power is the maximum power consumption of the IC at any instance during its execution. In this work, peak power is defined as the maximum power consumption during any clock cycle. The reduction of peak power consumption is essential for the following reasons : (i) to maintain supply voltage levels and (ii) to increase reliability. High peak power can affect the supply voltage levels. The large current flow causes high IR drop in the power line, which leads to the reduction of the supply voltage levels at different parts of the circuit. High current flow can reduce reliability because of hot electron effect and high current density. The hot electrons may lead to runaway current failures and electrostatic discharge failures. Moreover, high current density can cause electromigration failure. It is observed that the mean time to failure (MTF) of CMOS circuit is inversely proportional to the current density.

In this work, we focus on simultaneous peak and average power reduction during behavioral datapath scheduling using integer linear programming (ILP). The rest of the paper is organized as follows. The various related works are outlined in the next section, followed by the ILP formulations and the scheduling algorithms, experimental results and conclusions.

II. Related Work

The use of multiple supply voltages for energy reduction is well researched and several works have appeared in the literature [3], [4], [5], [6], [16], [17]. The energy savings in this scheme is often accompanied by degradation in performance because of the increase in the critical path delay. The degradation in performance can be compensated using DFC [6], multicycling and chaining [7], and variable latency components [8], [9], [10]. In multi-cycling, an operation is scheduled for more than a single control step and in addition, each control step is of equal length. On the other hand, in the case of DFC, an operation is scheduled in one unique control step, but all the control steps of a schedule may not be of equal length and also, the clock frequency may be changed on-the-fly.

In the works reported in [2], the peak power reduction is achieved through simultaneous assignment and scheduling using genetic algorithms for optimization. In [11], ILP based scheduling and force directed scheduling have been proposed to minimize peak power under latency constraints. ILP based models to minimize peak power and peak area have been proposed in [12] for latency constraint scheduling. The authors also introduced resource binding to minimize the amount of switching at the input of functional units. In [14], a time

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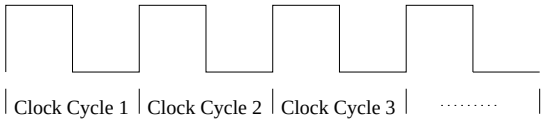
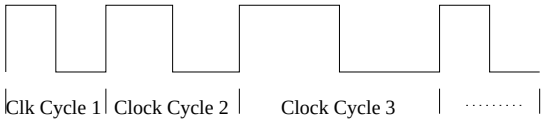


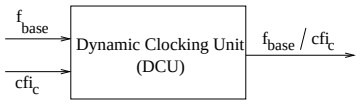
Clock Cycle 1 = Clock Cycle 2 = Clock Cycle 3

(a) Single frequency



Clock Cycle 1 ≠ Clock Cycle 2 ≠ Clock Cycle 3

(b) Dynamic frequency



(c) Dynamic Clocking Unit

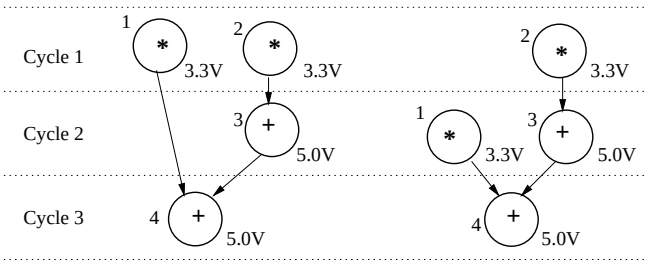
Fig. 1. (a) Shows conventional single frequency clocking scheme in which clock width is the same for every cycle. (b) Shows dynamic frequency clocking scheme in which clock width is not same for every cycle. (c) Shows a scheme for dynamic frequency generation using dynamic clocking unit

constrained scheduling algorithm for real time systems using ILP models that minimizes both peak power and number of resources, is described. The authors in [15] propose the use of data monitor operations for simultaneous peak power reduction and peak power differential. In [18], a heuristic based scheme is proposed that minimizes peak power, peak power differential, average power, and energy altogether. In [19], the authors propose ILP based datapath scheduling schemes for peak power minimization under resource constraints.

In this work, we propose datapath scheduling schemes using ILP for the simultaneous reduction of peak and average power at the behavioral level. One scheduling scheme uses multiple supply voltages and dynamic frequency clocking for power reduction while maintaining performance. The other proposed scheduling scheme uses combined multiple supply voltages and multi-cycling for power reduction. Both the scheduling schemes use multiple type and number of functional units at different operating voltages as resource constraints. The dynamic frequency clocking methodology is more effective for data intensive signal processing applications. Moreover, since power is quadratically dependent on the supply voltage and is linearly dependent on the operating frequency, the judicious choice of supply voltages and operating frequency can reduce significant amount of power.

III. Dynamic Clocking and Multiple Voltages

In multiple supply voltage scheme, different functional units are operated at different supply voltages in order to achieve energy and average power reduction [3], [4], [5]. In this



(a) Energy Efficient Schedule (b) Peak Power Efficient Schedule

Fig. 2. Energy Vs Peak Power Efficient Schedule of the Data Flow Graph. Both DFGs consume same amount of energy, but the peak power consumption of the schedule in (a) is more than that of (b), as in previous DFG there are two energy hungry operators (two multipliers) scheduled in one control step.

scheme, if the off-critical operations can be executed in low voltage functional units, then it is possible to reduce power and/or energy without degradation of performance. On the other hand, the use of low voltage functional units in the critical path can reduce performance. In such situations, the use of dynamic frequency clocking, multi-cycling, chaining, pipelining, variable latency can be considered mechanisms along with the multiple supply voltages to compensate for the performance. We demonstrate the single frequency and dynamic frequency using Fig. 1(a) and Fig. 1(b).

Recently, the use of dynamic frequency clocking (or frequency scaling) is being investigated for energy reduction [6]. Frequency scaling by itself does not help in energy reduction, but it creates opportunity to operate different functional units at different voltages, which in turn, helps in energy reduction. On the other hand, the simultaneous use of multiple supply voltages and frequency reduction can directly reduce power consumption in three folds. This is because power consumption of CMOS circuit is proportional to frequency and square of the supply voltage. It should be noted that judicious use of voltage and frequency reduction is necessary to maintain performance while achieving the power reduction. In dynamic frequency clocking, the clock frequency is varied on-the-fly based on the active functional unit in that cycle. In this scheme, all the units are clocked by single clock line which switches at run time. This scheme, in particular, is suitable for data intensive or compute intensive, DSP applications. The architecture for dynamic clocking based systems consists of a datapath, a controller and a dynamic clocking unit (DCU). The datapath consists of functional units with registers and multiplexors. The controller decides which functional units are active in each control step and those not active are disabled using a multiplexor. The DCU generates the required clock frequency usually using clock divider strategy [20], [21] which are sub-multiples of base frequency. The base frequency is the maximum frequency (or multiple of maximum) of any functional unit at maximum supply voltage. The controller has storage units to store the parameters called, “clock frequency index” ([6]) for each control step which are to be obtained from the datapath scheduling algorithms. This clock frequency index parameter serves as clock dividing factor for the DCU. The cycle frequency is generated dynamically and functional units at appropriate supply voltages are activated. In this

TABLE I
NOTATIONS USED IN DESCRIPTION OF POWER CONSUMPTION

c	: any control step or clock cycle in DFG
N	: total number of control steps in the DFG
R_c	: number of resources active in step c
f_c	: cycle frequency for control step c
$\alpha_{i,c}$	: switching at resource i operating in step c
$C_{i,c}$	: load capacitance of resource i operating in control step c
$V_{i,c}$	: operating voltage of resource i operating in control step c
P_c	: power consumption for the DFG for any control step c
P_p	: maximum power consumption for the DFG
P_a	: average power consumption for the DFG
T	: critical path delay of the DFG
PDP	: power delay product of the DFG

scheme, level converters are other overheads along with the dynamic clocking unit and additional storage in the control unit. The scheme for dynamic frequency generation is shown in Fig. 1(c). Loading a value of cfi_c into the counters provide a divided output clock of frequency, $\frac{f_{base}}{cfi_c}$.

To have a clear understanding of the scheduling for energy minimization and peak power minimization, let us refer to the data flow graph (DFG) in Fig. 2. The figure shows two different possible schedules of the same DFG using multiple supply voltage scheme. Since, in both cases there are two multipliers operating at $3.3V$ and two adders operating at $5.0V$, the energy and average power consumption of both scheduled DFGs is the same. But, the peak power consumption of the schedule in Fig. 2(a) is more than that of Fig. 2(b), as in previous DFG there are two energy hungry operators (two multipliers) scheduled in one control step. Our approach is to generate peak power efficient schedules similar to the one in Fig. 2(b).

IV. PEAK AND AVERAGE POWER MODELING

In this section, we first mention the different notations and terminology needed for a scheduling model. Let us assume that the datapath is represented in the form of a sequencing data flow graph. The datapath uses various resources or functional units operating at different supply voltages. The level converters are considered as resource overheads often needed when the voltage level needs to be stepped up in any control step. The DCU that generates variable frequency is also accounted as a resource that will operate during all the control steps. The notation and terminology are given in Table I. It may be noted that for single frequency and single supply voltage mode of operation, $V_{i,c}$ and f_c are the same for any clock cycle (c) and resource (i). Similarly, for multi-cycling operation f_c is the same for any clock cycle (c).

The power consumption for any control step c is

$$P_c = \sum_{i=1}^{R_c} \alpha_{i,c} C_{i,c} V_{i,c}^2 f_c \quad (1)$$

The peak power consumption of the DFG is the maximum power consumption over all the control steps which is expressed as below.

$$P_p = Max\left(P_c\right)_{\forall c=1,2,\ldots N} \quad (2)$$

We rewrite Eqn. 2 using Eqn. 1 as follows.

$$P_p = Max\left(\sum_{i=1}^{R_c} \alpha_{i,c} C_{i,c} V_{i,c}^2 f_c\right)_{\forall c=1,2,\ldots N} \quad (3)$$

TABLE II
NOTATIONS USED IN ILP FORMULATIONS

O	: total number of operations in the DFG excluding the source and sink nodes (NO-OPs)
o_i	: any operation i, $1 \leq i \leq O$
$F_{k,v}$	: functional unit of type k operating at voltage level v
$M_{k,v}$	: maximum number of functional units of type k operating at voltage level v
S_i	: as soon as possible (ASAP) time stamp for operation o_i
E_i	: as late as possible (ALAP) time stamp for operation o_i
$P(i,v,f)$	: power consumption of operation o_i at voltage level v and operating frequency level f
$x_{i,c,v,f}$	: decision variable which takes the value of 1 if operation o_i is scheduled in control step c using the functional unit $F_{k,v}$ and c has frequency level f
$y_{i,v,l,m}$	: decision variable which takes the value of 1 if o_i is using functional unit $F_{k,v}$ and scheduled in control steps $l \rightarrow m$
$L_{i,v}$	: latency for operation o_i using resource operating at voltage v (in terms of number of clock cycles)

The average power consumption of the DFG is characterized as the mean of the cycle powers (P_c) for all control steps.

$$P_a = \frac{1}{N} \sum_{i=1}^{N} P_c \quad (4)$$

Again using Eqn. 1, we rewrite Eqn. 4 as follows.

$$P_a = \frac{1}{N} \sum_{i=1}^{N} \sum_{i=1}^{R_c} \alpha_{i,c} C_{i,c} V_{i,c}^2 f_c \quad (5)$$

Since the simultaneous reduction of both peak and average power is aimed for, the objective function to be minimized by the scheduling algorithm is the sum of Eqn. 3 and 5.

The critical path delay of the DFG can be calculated as,

$$T = \sum_{i=1}^{N} \frac{1}{f_c} \quad (6)$$

It should be noted that the f_c is the same for single frequency and multi-cycling operations for all values of c and may be different for dynamic frequency clocking operations. The power delay product of the DFG is defined as the product of the average power consumption and critical path delay as shown below.

$$PDP = P_a * T \quad (7)$$

Using Eqns. 4 and 6, the following expression for the power delay product is obtained.

$$PDP = \frac{1}{N} \sum_{i=1}^{N} P_c * \sum_{i=1}^{N} \frac{1}{f_c} \quad (8)$$

Similarly, the following expression for the power delay product is arrived using Eqns. 5 and 6.

$$PDP = \frac{1}{N} \sum_{i=1}^{N} \sum_{i=1}^{R_c} \alpha_{i,c} C_{i,c} V_{i,c}^2 f_c * \sum_{i=1}^{N} \frac{1}{f_c} \quad (9)$$

To study the impact of the scheduling algorithms on the performance of the datapath the power delay product of the scheduled DFGs using the above expression will be estimated.

V. ILP FORMULATIONS

In this section, we discuss the ILP formulations to minimize the peak and average power consumption of a datapath circuit. We first discuss the formulations for MVDFC based system followed by MVMC based system. We assume that the formulations for SVSF based system can be obtained from the MVDFC formulations by relaxing some constraints. The notations used for ILP formulations are given in Table II.

A. ILP formulations for MVDFC

In this section, the ILP formulation for simultaneous peak (Eqn. 3) and average power (Eqn. 5) minimization using MVDFC is described. In dynamic frequency clocking [21], [22], the clock frequency is varied on-the-fly based on the functional units active in that cycle. In this clocking scheme, all the units are clocked by a single clock line which switches at run-time. The frequency reduction creates an opportunity to operate the different functional units at different voltages, which in turn, helps in further reduction of power.

(a) *Objective Function* : The objective is to minimize the peak power and the average power consumption of the whole DFG over all control steps simultaneously. These are already described above in Eqn. 3 and 5.

$$Min \quad : \quad P_p + P_a \tag{10}$$

Using decision variables the objective function can be rewritten as follows :

$$Min : P_p + \tfrac{1}{N} \sum_c \sum_v \sum_{i \in F_{k,v}} \sum_f x_{i,c,v,f} P(i,v,f) \tag{11}$$

It should be noted that the P_p is unknown and has to be minimized. P_p may be the power consumption of any control step in the DFG depending on the scheduled operations and hence is later used as a constraint.

(b) *Uniqueness Constraints* : These constraints ensure that each operation o_i is scheduled to one unique control step within the mobility range (S_i, E_i) with a particular supply voltage and operating frequency. They are represented as, $\forall i$, $1 \leq i \leq O$,

$$\sum_c \sum_v \sum_f x_{i,c,v,f} \quad = \quad 1 \tag{12}$$

(c) *Precedence Constraints* : These constraints ascertain that for an operation o_i, all its predecessors are scheduled in an earlier control step and its successors are scheduled in later control step. These are modeled as, $\forall i, j, o_i \in Pred_{o_j}$

$$\sum_v \sum_f \sum_{d=S_i}^{E_i} dx_{i,d,v,f} - \sum_v \sum_f \sum_{e=S_j}^{E_j} ex_{j,e,v,f} \leq -1 \tag{13}$$

(d) *Resource Constraints* : These constraints establish that no control step contains more than $F_{k,v}$ operations of type k operating at voltage v. These can be enforced as, $\forall c$, $1 \leq c \leq N$ and $\forall v$,

$$\sum_{i \in F_{k,v}} \sum_f x_{i,c,v,f} \quad \leq \quad M_{k,v} \tag{14}$$

(e) *Frequency Constraints* : This set ensures that if a functional unit is operating at higher voltage level then it can be scheduled in a lower frequency control step, whereas if a functional unit is operating at lower voltage level then it can not be scheduled in a higher frequency control step. These constraints are written as, $\forall i$, $1 \leq i \leq O$, $\forall c$, $1 \leq c \leq N$, if $f < v$, then $x_{i,c,v,f} = 0$.

(f) *Peak Power Constraints* : These constraints make certain that the maximum power consumption of the DFG does not exceed P_p for any control step. These constraints are applied as follows, $\forall c$, $1 \leq c \leq N$ and $\forall v$,

$$\sum_{i \in F_{k,v}} \sum_f x_{i,c,v,f} * P(i,v,f) \quad \leq \quad P_p \tag{15}$$

B. ILP formulations for MVMC

In this section, we describe the ILP formulations for simultaneous minimization of both peak and average power consumption of the DFG using MVMC.

(a) *Objective Function* : The aim is to minimize the peak and average power consumption of the whole DFG over all control steps. The expressions given in Eqn. 3 and Eqn. 5 are still valid here, with the only difference being that f_c is the same for all control steps.

$$Min \quad : \quad P_p + P_a \tag{16}$$

In terms of decision variables, the above is written as :

$$Min: P_p + \tfrac{1}{N} \sum_l \sum_{i \in F_{k,v}} \sum_v y_{i,v,l,(l+L_{i,v}-1)} P(i,v,f_{clk}) \tag{17}$$

The P_p is used as a constraint later.

(b) *Uniqueness Constraints* : These constraints confirm that every operation o_i is scheduled in appropriate control steps within the mobility range (S_i, E_i) with a particular supply voltage. It may be operated at more than one clock cycle depending on the supply voltage. These constraints are represented as, $\forall i$, $1 \leq i \leq O$,

$$\sum_v \sum_{l=S_i}^{S_i+E_i+1-L_{i,v}} y_{i,v,l,(l+L_{i,v}-1)} \quad = \quad 1 \tag{18}$$

When the operators are operating at highest voltage, they are scheduled in one unique control step, whereas, when they are to be operated at lower voltages they need more than one clock cycle for completion. Thus, for a lower voltage the mobility is restricted.

(c) *Precedence Constraints* : These constraints guarantee that for an operation o_i, all its predecessors are scheduled in an earlier control step and its successors are scheduled in an later control step. These constraints should also take care of the multi-cycling operations. These are modeled as, $\forall i, j, o_i \in Pred_{o_j}$,

$$\begin{array}{l} \sum_v \sum_{l=S_i}^{E_i} (l + L_{i,v} - 1) * y_{i,v,l,(l+L_{i,v}-1)} \\ \quad - \sum_v \sum_{l=S_j}^{E_j} l * y_{j,v,l,(l+L_{j,v}-1)} \end{array} \quad \leq \quad -1 \tag{19}$$

(d) *Resource Constraints* : These constraints make sure that no control step contains more than $F_{k,v}$ operations of type k operating at voltage v. These can be enforced as, $\forall v$ and $\forall l$, $1 \leq l \leq N$,

$$\sum_{i \in F_{k,v}} \sum_l y_{i,v,l,(l+L_{i,v}-1)} \quad \leq \quad M_{k,v} \tag{20}$$

(e) *Peak Power Constraints* : These constraints ensure that the maximum power consumption of the DFG does not exceed P_p for any control step. These constraints are enforced as follows, $\forall l$, $1 \leq l \leq N$,

$$\sum_{i \in F_{k,v}} \sum_v y_{i,v,l,(l+L_{i,v}-1)} * P(i,v,f_{clk}) \quad \leq \quad P_p \tag{21}$$

VI. Datapath Scheduling Schemes

In this section, we discuss the solutions for the ILP formulations obtained in the previous section. We assume the same target architecture as that of [6], [3], [13] as shown in Fig. 3, and the characterized datapath components used are from [6]. Each functional unit is associated with a register and a multiplexor. The register and the multiplexor will operate at the same voltage level as that of the functional units. Level converters are used when a low-voltage functional unit is driving a high-voltage functional unit [3], [13]. A controller decides which of the functional units are active in each control step and those that are not active are disabled using the multiplexors. The controller has a storage unit to store the cycle frequency index (cfi_c) values obtained from the scheduling, used as the clock dividing factor for the dynamic clocking unit. The cycle frequency f_c is generated dynamically and a corresponding functional unit is activated.

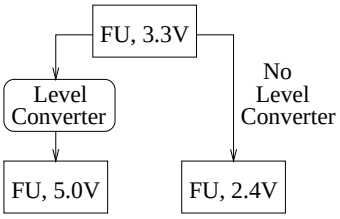


Fig. 3. Level converters are needed when a low-voltage functional unit is driving a high-voltage functional unit for stepping up signal

The datapath is specified as a sequencing data flow graph (DFG). Each vertex of the DFG represents an operation and each edge represents dependency. In this work, we are considering the signal processing applications, in which the dynamic frequency clocking scheme is useful for energy reduction. So, we assume that the datapath circuit is represented as directed acyclic DFG. The DFG does not support the hierarchical entities and the conditional statements are handled using comparison operation. Each vertex has attributes that specifies the operation type. The delay of a control step is dependent on the delays of the functional unit and the multiplexor and register pairs. Let, d_{reg} be the delay of the register, d_{mux} be the delay of the multiplexor, d_{fu} be the delay of the functional unit and d_{level} be the delay of the level converter. The worst case operational delay of a functional unit can be written as :

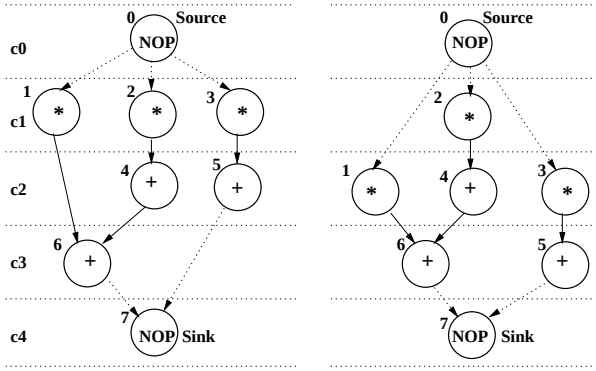
$$d_{FU} = d_{reg} + d_{mux} + d_{fu} + d_{level} \tag{22}$$

The register delays include the set-up and propagation delays. The delay of control step d_c is the delay of the slowest functional unit in the control step c. The worst case delays of the library components are estimated using the above delay model.

Peak and average power consumption of the DFG is minimized by the ILP based scheduler outlined in Fig. 4. The first step is to determine the as soon as possible (ASAP) time stamp of each operation. The second step is the determination of the as late as possible (ALAP) time stamp of each vertex for the DFG. The ASAP time stamp is the start time and the ALAP time stamp is the finish time of each operation.

Step 1 : Find the ASAP schedule of the input DFG.
Step 2 : Find the ALAP schedule of the input DFG.
Step 3 : Determine the mobility graph of each node.
Step 4 : Modify the mobility graph for multi-cycling.
Step 5 : Construct the ILP formulations.
Step 6 : Solve the ILP formulations using LP-Solve.
Step 7 : Find the scheduled DFG.
Step 8 : Determine the cycle frequencies for MVDFC.
Step 9 : Estimate the power consumptions of the DFG.

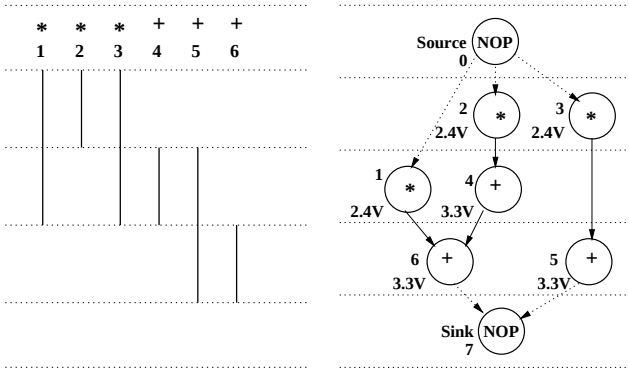
Fig. 4. ILP-based Scheduler for Peak and Average Power Minimization



(a) ASAP schedule (b) ALAP schedule

Fig. 5. ASAP schedule and ALAP schedule for the Example DFG

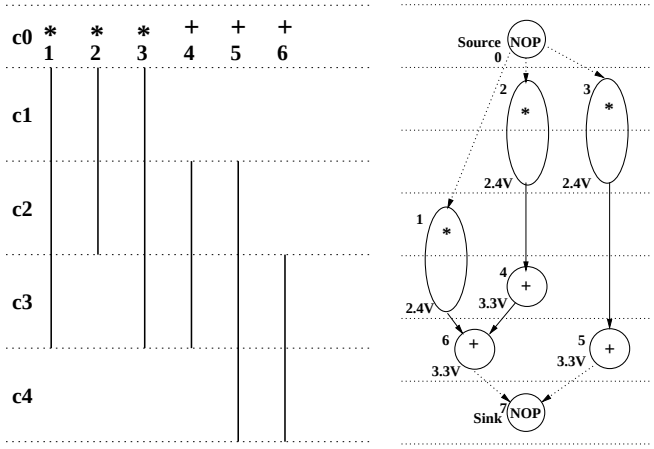
These two times provide the mobility of an operation and the operation must be scheduled in this mobile range. This mobility graph needs to be modified for the multi-cycling scheme. The scheduler is based on the ILP formulations described in Section V. At this point, the operating frequency of a functional unit is assumed as the inverse of its operational delay determined using the delay model given in [18]. The ILP formulations are solved to derive the scheduled DFG. The scheduler decides the cycle frequencies based on the formulas given in [18]. Finally, the power consumption of the scheduled DFG is estimated.



(a) Mobility graph (b) Final schedule

Fig. 6. Example DFG for resource constraint RC3 using MVDFC

We now discuss the solution of the ILP formulations for



(a) Mobility graph (b) Final schedule

Fig. 7. Example DFG for resource constraint RC3 using MVMC

TABLE III
NOTATIONS USED IN EXPRESSING RESULTS

P_{p_S}	: peak power consumption (in mW) for SVSF
P_{p_D}	: peak power consumption (in mW) for MVDFC
P_{p_M}	: peak power consumption (in mW) for MVMC
P_{a_S}	: average power consumption (in mW) for SVSF
P_{a_D}	: average power consumption (in mW) for MVDFC
P_{a_M}	: average power consumption (in mW) for MVMC
T_S	: critical path delay for SVSF operation
T_D	: critical path delay for MVDFC operation
T_M	: critical path delay for MVMC operation
PDP_S	: power delay product (in nJ) for SVSF $(= P_{a_S} * T_S)$
PDP_D	: PDP (in nJ) for MVDFC $(= P_{a_D} * T_D)$
PDP_M	: PDP (in nJ) for MVMC $(= P_{a_M} * T_M)$
ΔP_{p_D}	: percentage peak power reduction using the MVDFC scheme $\left(= \frac{(P_{p_S} - P_{p_D})}{P_{p_S}} * 100\right)$
ΔP_{p_M}	: percentage peak power reduction using the MVMC scheme $\left(= \frac{(P_{p_S} - P_{p_M})}{P_{p_S}} * 100\right)$
ΔPDP_D	: percentage PDP reduction using the MVDFC scheme $\left(= \frac{(PDP_S - PDP_D)}{PDP_S} * 100\right)$
ΔPDP_M	: percentage PDP reduction using the MVMC scheme $\left(= \frac{(PDP_S - PDP_M)}{PDP_S} * 100\right)$

MVDFC scheme and in the process illustrate the corresponding scheduling algorithm. Let us assume an example data flow graph whose ASAP schedule and ALAP schedule is shown in Fig. 5(a) and Fig. 5(b), respectively. Allowable time steps of individual operations are shown in the mobility graph in Fig. 6(a), which are obtained from the above ASAP and ALAP schedules. The ILP formulations are solved using LP-solve and the scheduled DFG is shown in Fig. 6(b) for a resource constraint RC3, listed in the next section.

The solution for the ILP formulation for MVMC scheme is illustrated using the DFG shown in Fig. 7. The ASAP schedule is shown in Fig. 5(a) and the ALAP schedule is shown in Fig. 5(b). The mobility graph shown in Fig. 7(a) is obtained from the ASAP and ALAP schedules. This mobility graph is different from that shown in Fig. 6(a); The mobility graph in Fig. 7(a) considers the multi-cycle operations. Two operating voltage levels are assumed in Fig. 7(a). The multipliers take two clock cycles when operated at low voltage level. The ILP formulations are obtained using this mobility graph. The ILP formulations are solved using LP-solve and the scheduled DFG is shown in Fig. 7(b).

VII. EXPERIMENTAL RESULTS

The ILP-based schedulers for both MVDFC and MVMC schemes were tested with selected high-level synthesis benchmark circuits : (1) Example circuit (EXP), (2) FIR filter, (3) IIR filter, (4) HAL differential equation solver and (5) Auto-Regressive filter (ARF). The notations used to express the various results are given in Table III. The schedulers were tested for each benchmark circuits using different sets of resource constraints shown in Table IV. The number of allowable voltage levels is two $(2.4V, 3.3V)$ and maximum number of allowable frequencies being three. The scheduler uses the modeling language AMPL to model the ILP formulations.

The experimental results for various benchmark circuits are reported in Table V for both MVDFC and MVMC schemes. We perform the characterization of the physical implementations of the library modules available in [6] by applying random input patterns. The results are reported for two supply voltages and for switching $= 0.5$. The power is estimated including the overheads, such as level converters (used in both the schemes) and dynamic clocking units (as needed in MVDFC scheme). In MVDFC scheduling method, the frequencies found are $4.5MHz, 9MHz,$ and $18MHz$. For MVMC scheduling scheme, the operating frequency f_{clk} is $9MHz$. The operating voltage and frequency for SVSF scheme is $3.3V$ and $9MHz$, respectively. The tables show the estimates for peak power consumption, average power consumption, and power delay product for various benchmarks for different resource constraints. The reduction in power values are reported in terms of percentage with respect to SVSF operation mode. Significantly large reduction in both peak power consumption and average power consumption are observed and are consistent for all benchmarks and resource constraints for the MVDFC scheme. On the other hand, for the MVMC scheme the peak power reduction is not appreciable for ARF benchmark, but the reduction in average power reduction is consistent for all the benchmarks under all resource constraints. The reduction in the power delay product is appreciable and consistent for all benchmarks under resource constraints. There is no reduction in power delay product for the MVMC scheme, hence not reported in the experimental table, which indicates that there is no change in the energy consumption of circuits.

TABLE IV
RESOURCE CONSTRAINTS USED FOR OUR EXPERIMENT

Resource Constraints				Resource Constraint Labels
Multipliers		ALUs		
2.4 V	3.3 V	2.4 V	3.3 V	
2	1	1	1	RC1
3	0	1	1	RC2
2	0	0	2	RC3
1	1	0	1	RC4

TABLE V

PEAK POWER, AVERAGE POWER AND PDP ESTIMATES FOR BENCHMARKS USING SCHEDULING SCHEMES

	RC	Peak Power (mW)					Average Power (mW)					PDP Estimates (nJ)			
		P_{pS}	P_{pD}	ΔP_{pD}	P_{pM}	ΔP_{pM}	P_{aS}	P_{aD}	ΔP_{aD}	P_{aM}	ΔP_{aM}	PDP_S	PDP_D	ΔPDP_D	PDP_M
(1)	1	17.28	4.56	73.6	8.76	49.3	8.86	2.41	72.8	6.57	25.8	2.95	1.33	54.9	2.92
exp	2	17.28	4.56	73.6	13.68	20.8	8.86	2.41	72.8	6.98	21.2	2.95	1.33	54.9	3.1
	3	17.28	4.56	73.6	9.12	47.2	8.86	2.61	70.5	5.58	37.0	2.95	1.30	55.9	3.1
	4	8.86	2.39	73.0	8.86	0	6.65	1.88	71.7	6.65	0	2.96	1.36	54.1	2.95
	Average values			73.5		29.3			72.0		21.0			55.0	
(2)	1	17.28	4.56	73.6	8.76	49.3	8.82	2.34	73.5	7.28	17.5	4.9	2.34	52.5	4.85
fir	2	17.28	4.56	73.6	13.68	20.8	8.82	2.35	73.4	7.68	12.9	4.9	2.35	52.0	5.12
	3	17.28	4.56	73.6	13.68	20.8	8.82	2.44	72.3	6.64	24.7	4.9	2.30	53.0	5.12
	4	17.28	6.60	61.8	8.86	48.7	8.82	2.84	67.8	7.35	16.7	4.9	2.68	45.3	4.9
	Average values			70.7		34.9			71.8		18.0			50.7	
(3)	1	25.92	8.88	65.7	17.76	31.5	11.03	3.49	68.4	8.95	18.9	4.9	2.32	52.7	4.97
iir	2	25.92	6.84	73.6	13.68	47.2	11.03	2.98	73.0	7.68	30.4	4.9	1.98	59.6	5.12
	3	17.28	4.56	73.6	9.12	47.2	8.82	2.45	72.2	5.24	40.6	4.9	2.0	59.2	4.66
	4	17.28	6.60	61.8	13.20	23.6	8.82	3.31	62.5	8.05	8.7	4.9	2.57	47.6	5.37
	Average values			68.7		37.4			69.0		24.7			54.8	
(4)	1	17.51	4.62	74.7	13.32	23.9	13.25	3.55	73.2	8.82	33.4	5.89	2.76	53.1	5.88
hal	2	17.51	4.62	74.7	13.68	21.9	13.25	3.55	73.2	9.23	30.3	5.89	2.76	53.1	6.15
	3	17.51	4.67	73.3	9.34	46.7	13.25	3.73	71.8	7.98	39.8	5.89	2.69	54.3	6.20
	4	17.51	6.71	61.7	13.42	23.4	10.59	3.73	64.8	8.90	16.0	5.88	3.52	40.1	5.93
	Average values			71.1		29.0			70.8		29.9			50.2	
(5)	1	8.86	2.34	73.6	8.64	2.5	4.50	1.20	73.3	3.40	24.4	5.00	2.00	60.0	4.85
arf	2	8.86	2.34	73.6	8.64	2.5	4.50	1.20	73.3	3.58	24.4	5.00	2.00	60.0	4.85
	3	8.86	2.39	73.0	8.76	1.1	4.50	1.40	68.9	3.65	18.9	5.00	1.90	62.0	5.0
	4	8.86	2.39	73.0	8.76	1.1	4.50	1.40	68.9	3.46	23.1	5.00	1.90	62.0	5.0
	Average values			73.3		1.8			71.1		22.7			61.0	
Average over all benchmarks				71.5		26.5			71.0		23.3			54.3	

TABLE VI

POWER REDUCTION FOR VARIOUS SCHEDULING SCHEMES

Benchmark Circuits	Percentage average data for various schemes									
	DFC based (This work)		Shiue [11]		Martin [2]		Raghunathan [15]		Mohanty [18]	
	ΔP_p	ΔP_a	ΔP_p	ΔP_a	ΔP_p	ΔP_a	ΔP_p	ΔP_a	ΔP_p	ΔP_a
EXP(1)	73	72	-	-	-	-	-	-	-	-
FIR(2)	71	72	63	NA	40	NO	23	38	71	53
IIR(3)	69	69	-	-	-	-	-	-	-	-
HAL(4)	71	71	28	NA	-	-	-	-	73	70
ARF(5)	73	71	50	NA	-	-	-	-	68	67

The power reductions for the proposed scheduling scheme are listed along with other scheduling algorithms dealing with peak power reduction in Table VI. The objective of including this table is not to compare the techniques, but only intended to provide a general idea of relative performance. While the technique proposed in this paper optimizes both average and peak power the other techniques listed in the table optimize only peak power. Since, the schemes listed have different objectives, constraints, and overheads, a direct fair comparison is not possible. It was observed that the area overheads due to level converters and the dynamic clocking unit for the proposed methodology, are not significant. As an example design, a dual voltage dual frequency digital watermarking chip was designed and verified in [23]. The design required 416 level converters with 6 transistors each in a chip that needed a total of 1.4 million transistors. Moreover, a DCU unit design is carried out in [20], which consisted of 200 transistors. Thus, the overhead due to level converters and the DCU is approximately 0.02%. The low overhead makes the use of dynamic frequency clocking with multiple voltages scheme possible.

VIII. CONCLUSIONS

The reduction of both peak power consumption and average power consumption is important in CMOS design. This paper addresses simultaneous peak power and average power reduction at behavioral level using low power datapath scheduling. Two datapath scheduling schemes, one using combined multiple supply voltage and dynamic clocking and another using combined multiple supply voltage and multi-cycling have been introduced. ILP based optimization techniques were used for both the above modes of datapath operations. The reductions attained in peak power, average power and power delay product by using combined multiple supply voltage and dynamic clocking were noteworthy. *The results clearly indicate that the dynamic frequency clocking is a better scheme than the multi-cycling approach for power minimization.*

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