Dopingless Transistor Based Hybrid Oscillator Arbiter Physical Unclonable Function

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***Abstract*—Transistors are approaching the sub-10nm regime. Due to extensive scaling of devices, the leakage currents are also increasing. FinFETs are also being scaled to 14 nm. To further push the limits of scaling and decrease leakage currents, Dopingless FET (DL-FET) transistors were introduced. DL-FETs show a promising decrease in leakage with low power consumption. An application using these devices, a hybrid oscillator arbiter physical unclonable function (PUF) using DL-FETs is presented here. Two different designs, one speed optimized and one power optimized are presented for different designs such as low power and also high performance. A comparative analysis of the DL-FET based PUF and FinFET based PUF is presented. The DL-FET PUF results in a 30% decrease in average power consumption compared to FinFETs. To the best of the authors' knowledge, the current paper is the first in exploring PUF realization using DL-FETs.**

***Index Terms*—Dopingless Junctionless FET, Physical Unclonable Function, Ring Oscillator**

I. Introduction

Low power high performance devices have been the target of researchers since the invention of the integrated circuit. A single chip is being packed with almost 8 billion transistors [1]. This has been possible with the introduction of FinFETs. Beyond 32nm, high-κ metal gate transistors also started to show signs of high leakage leading to more power consumption and chip overheating [2]. Hence FinFETs were used as a replacement for these transistors.

Junctionless transistors were introduced as a promising solution for these problems [3] but there are some issues with the junctionless FET. Poor switch-off capability, high parasitic capacitance, low on-state current and higher gate work function are some of them [4], [5]. These issues were solved by the introduction of the dopingless FET [6]. Higher band to band tunneling and random dopant fluctuations (RDF) are addressed in dopingless FETs using the thin intrinsic silicon nanowire to form the drain and source instead of heavily doped drain, channel and source [7].

With the increased performance and miniaturization of various devices, home applications for such devices have increased. The Internet of Things (IoT) is one of them [8], [9]. To encrypt the end to end communication of the devices in the IoT, a key that is unpredictable should be incorporated. Hence a Physical Unclonable Function can be used to generate the key and use it for encryption and decryption of communication. A PUF uses the process variation in manufacturing of devices as an advantage to generate different keys that can be used for various applications. In the current paper, the Hybrid Oscillator Arbiter PUF is implemented with the Dopingless FETs [10].

The rest of the paper is organized as follows: Section II presents the novel contributions of the paper, Section IV presents the structure of the dopingless transistor. The design of the PUF is presented in Section V. The simulation results are presented in Section VI. Section VII presents the conclusions.

II. Novel Contributions

Dopingless FETs can be considered a great solution for leakage and scalability issues. These are one of the two focused areas of interest when developing devices. DL-FETs can be manufactured with the current technology available and the leakage currents will also be much reduced. In the current paper, DL-FETs are used to design PUFs. Two PUF circuit designs are implemented: one speed optimized and the other power optimized. The speed optimized design can be implemented in areas where the power consumption is not a main concern such as routers or network switches but the performance of application is of the main concern. The power optimized design can be used in devices where the overall power consumption of the device is of importance like hand held smart devices which run on battery. A comparison to existing FinFET design implementations is also given in the simulation results section.

III. Related Prior Research

Extensive research is being conducted in reduction in leakage power. The leakage issues and short channel effects

for CMOS transistors and high-κ metal gate transistors are presented in [2]. A PVT analysis of circuits like SRAM with different technologies is also presented in [2]. A PVT analysis of FinFETs in analog application is presented in [11]. The Dopingless FETs structure, working and fabrication methodology along with an SRAM implementation was presented in [6]. In the same work, a stress test was conducted on the respective transistors to check the aging resistance of the devices. The transistors show a promising resistance to the aging effects. In [7], a comparison of the DL-FETs with the junctionless transistor was presented. The main issues with the junctionless transistors were presented and as a potential solution, the DL-FET was introduced. A temperature analysis on the DL-FETs is performed in [12], [13].

The IoT is already being implemented in many environments like industries and it is not so far when the entire home will be automated making it a smart home. Research is being conducted extensively in that area. In [14], a health monitoring system is presented which incorporates the IoT and connects different devices and automates the process of monitoring and diagnosing of thyroid function simpler. Modules which can be placed on the patient and a module for the doctor were developed and Bluetooth® technology was used for the communication between the patient module and the doctor module. In [15], different security issues in the IoT were presented. A very detailed description of uses of PUF in security applications is presented in [16].

PUF key generation has been in use for a long time. One of the advantages of PUFs is that the key is never stored in memory and is generated every time it needs to be used. In the current paper, a ring oscillator (RO) PUF is being used. Various designs of PUFs were proposed in [17], [18]. The RO PUF is easy to implement and also occupies smaller chip area and consumes less power comparatively. Conventional RO PUF design is presented in [19]. This paper also proposed a configurable PUF design where multiple keys can be generated using the same circuit which gives an opportunity to change keys when necessary. In [10], the design of the Hybrid Oscillator Arbiter PUF was proposed. Two different designs, power optimized and speed optimized PUFs were presented for implementation in different applications from handheld devices to high performance applications. [20] presents the design of a PUF to generate multiple keys.

IV. Dopingless Transistor - A Brief Introduction

Dopingless FETs were introduced 5to address the problems in junctionless transistors. Fig. 1 shows a 3D structure of the DL-FET and Table I provides the nominal parameters. The symbols for the n-type and p-type DL-FETs are presented in Fig. 2. The DL-FET does not utilize any external ion implantation. An undoped single uniform structure is used from source to drain. In the DL-FET, a thin intrinsic silicon nanowire is used between metal electrodes and gate, source and drain regions. The p-type and the n-type doping regions can be formed using work function engineering inside the undoped thin silicon. The difference between the work function of the undoped silicon film and the metal incorporated for source and drain will be a deciding factor for making the region p-type or n-type doping [7], [21].

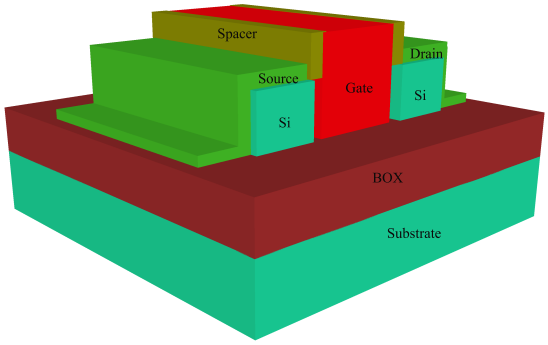
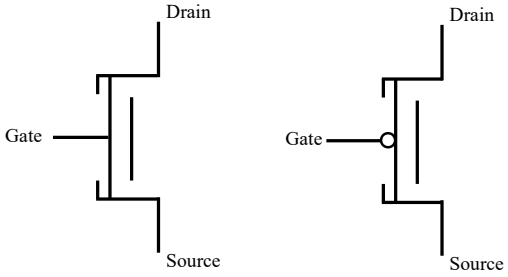


Fig. 1: Structure of Dopingless Transistor.

TABLE I: Device Parameters of Dopingless FET [22].

Parameters	Dopingless FET
Silicon Film Thickness (T_{si})	10 nm
Effective Oxide Thickness (EOT)	1 nm
Gate Length (L_g)	20 nm
Width (W)	1 μm
Source/Drain extension	10 nm
Metal work function/doping for source/drain	3.9 EV (Hafnium)
Metal work function/doping for gate	4.66 eV (TiN)
Doping	$10^{15}/cm^3$



(a) n-Type (b) p-Type

Fig. 2: Symbols for the n-Type and p-Type Dopingless Transistor.

V. Design of Physical Unclonable Functions

A. Conventional RO PUF Design

Fig. 3 shows the design of a conventional RO PUF [19]. In this design of PUF, the ring oscillators are connected to a counter. The oscillations produced are counted using the counter. The output of the counter is given as an input to a comparator. The comparator compares the number of oscillations produced by the ring oscillator over a period of time. Two ring oscillators are selected using the multiplexers and oscillations are counted. Due to process variations, the oscillations will not be the same. There will be a change

in the counter output. Based on the number of oscillations, the comparator produces a 1 or 0. After this, a new set of oscillators is selected and compared. In this manner, a 64 or 128 bit PUF key is generated. Different multiplexer select signals will be different challenges for the design. Here, due to the counter and comparator, the chip area and the power consumption are increased. These issues are addressed in the hybrid oscillator arbiter PUF design.

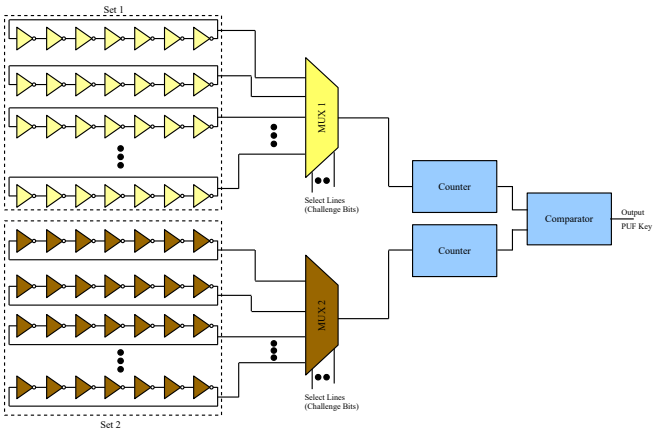


Fig. 3: Conventional Ring Oscillator PUF Design.

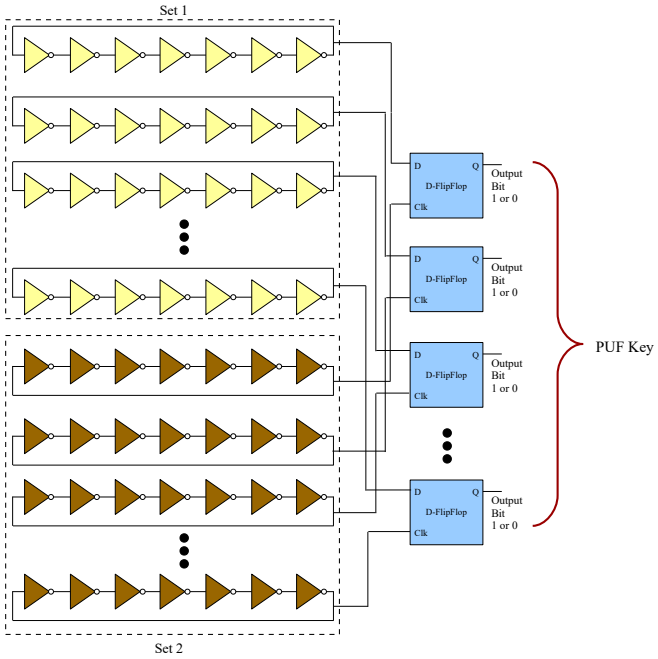


Fig. 4: Dopingless Transistor Based Speed Optimized Hybrid Oscillator Arbiter PUF.

B. Dopingless Transistor Based Speed Optimized Hybrid Oscillator Arbiter PUF

Fig. 4 shows the design of the speed optimized hybrid oscillator arbiter PUF designed using dopingless transistors. The design of this PUF is similar to the traditional PUF, but modified to address the problems associated with the conventional design like chip size and power consumption. This speed optimized PUF is designed for usage in applications where data is needed to be processed fast trading off the power consumption of the overall module. In this hybrid oscillator PUF, all the ring oscillators are divided into two sets: SET-1 and SET-2. Each of the ring oscillators from SET-1 is connected to the D-inputs of different D flip flops and each of the ring oscillators from SET-2 are connected to the clock signal of the D flip flops. The oscillating frequency will be different for ring oscillators due to the process variations. At a chosen point of time, the outputs from the D flip flops is observed. Depending on the oscillations, the D-input and clock values will be different. This will produce different ones or zeros at the output, which is the encryption key.

C. Dopingless Transistor Based Power Optimized Hybrid Oscillator Arbiter PUF

Fig. 5 shows the design of the power optimized hybrid oscillator arbiter PUF designed using dopingless transistors. The speed optimized version consists of a number of D flip flops which consume more power so it cannot be incorporated into hand held devices which run on a battery. The ring oscillators are again divided into sets SET-1 and SET-2. All the oscillators from SET-1 are connected to a multiplexer MUX-1 and all the oscillators from SET-2 are connected to another multiplexer MUX-2. The output of MUX-1 is given to the D input of the D flip flop and the output of MUX-2 is given as clock to the D flip flop. Each of the multiplexers will select a single ring oscillator from the sets and feed the oscillations to the D flip flop. Due to process variations, at a chosen point of time, the values at clock and the D input of the flip flop will vary. So the resultant output of the flip flop will vary for each pair of ring oscillators selected. Here, the select lines of the muxes can be the challenge bits of the PUF.

VI. Simulation Results

For a PUF to be validated, the following properties must be satisfied: Uniqueness, and Reliability. The Figures of Merit (FoMs) considered in this section, along with the uniqueness and reliability, are the average power consumed by the module and the total time taken to generate the PUF key. There are the two main conflicting aspects in the applications as the data processing should be fast while consuming as little power as possible. For high performance, some power should be traded off and for low power consumption, performance trade off will always be needed. Table II shows a comparison of the Hamming distance between the FinFET based PUF and the Dopingless Transistor based PUF.

A. Uniqueness

The uniqueness of a PUF is the ability of the module to produce different PUF keys with a change in challenge bits. It can be checked using the Hamming distance of the keys produced by the circuit. For an ideal PUF, the hamming distance is 50%. Monte Carlo simulations were performed on

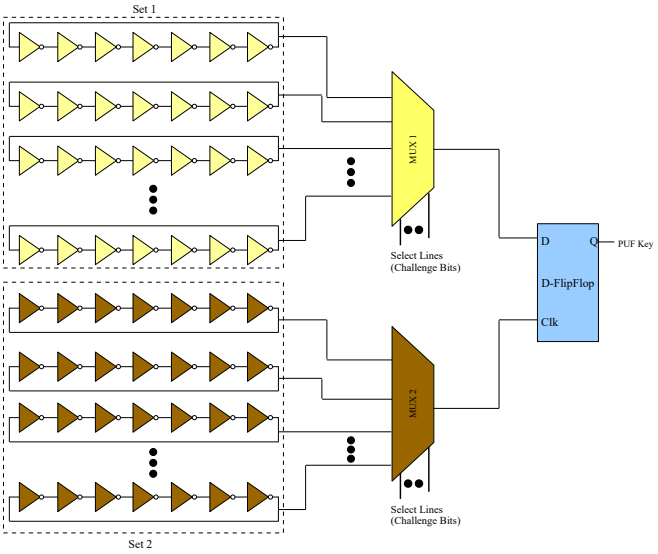


Fig. 5: Dopingless Transistor Based Power Optimized Hybrid Oscillator Arbiter PU.F

TABLE II: Characterization Table for Power and Speed Optimized Designs.

Power Optimized Hybrid Oscillator Arbiter PUF		
Parameter	FinFET	Dopingless Transistor
Average Power	175.5 μW	121.3 μW
Hamming Distance	50.1 %	48
Speed Optimized Hybrid Oscillator Arbiter PUF		
Average Power	251.5 μW	151 μW
Hamming Distance	48.3 %	50 %

the circuit to simulate the process and mismatch variations. 100 runs were performed and the output keys were checked for uniqueness. Fig. 6 shows the frequencies of different ring oscillators in each of the runs. This shows the different frequencies each of the oscillators produce for each run and in a single run. Figs. 7 and 8 show the Hamming distance between the different keys produced in different runs. The power optimized hybrid oscillator arbiter PUF consists of multiplexers and the select lines of the multiplexers can be considered as challenge bits. But in the speed optimized PUF there is not multiplexer present and hence no challenge bits are available. This means it will produce a single key once it is fabricated. For a fair comparison, only the process variation is considered in this case but not the challenge bit variation in both the designs.

B. Reliability

A PUF is not reliable if it cannot create the same key with the environmental variations and supply voltage variations. Environmental effects like temperature variations will affect the working of ring oscillators. In such conditions, the PUF with the same challenge bits should be generating the same key. To test the reliability of the designs, the temperature is varied and the power supply is varied. Figs. 9 and 10 show the Hamming distance of the keys generated by the designs.

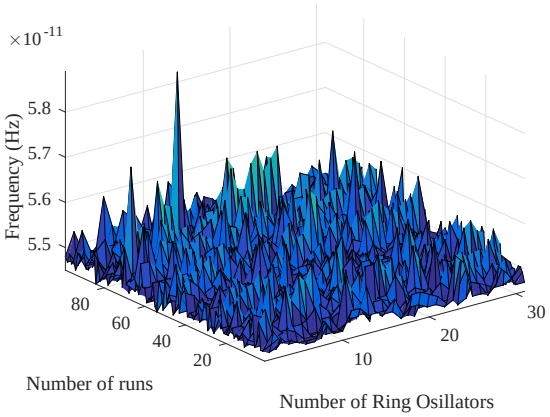


Fig. 6: Frequencies of Ring Oscillators.

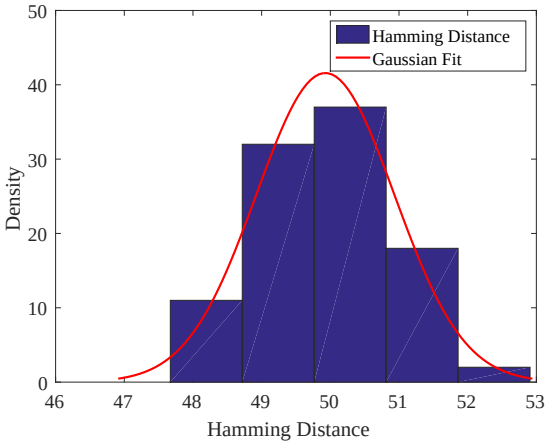


Fig. 7: Inter PUF Hamming Distance of Speed Optimized Hybrid Oscillator Arbiter PUF.

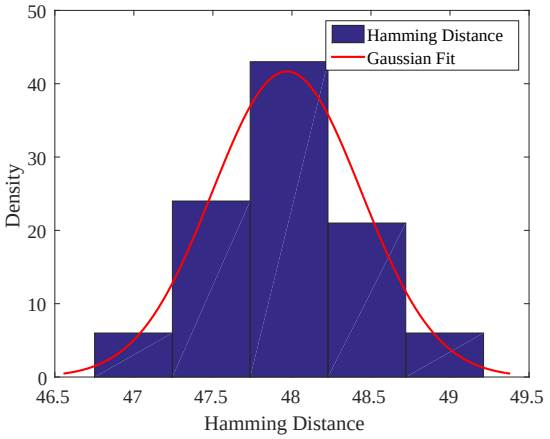


Fig. 8: Inter PUF Hamming Distance of Power Optimized Hybrid Oscillator Arbiter PUF.

The speed optimized PUF does not have much variation but comparatively, the power optimized PUF shows more variation. Table III shows the comparison of FoMs from other published works.

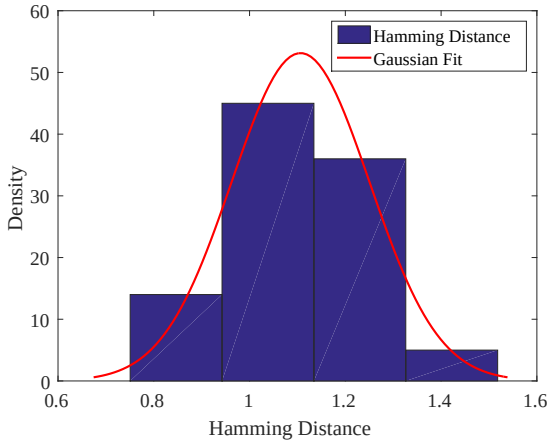


Fig. 9: Intra PUF Hamming Distance of Speed Optimized Hybrid Oscillator Arbiter PUF.

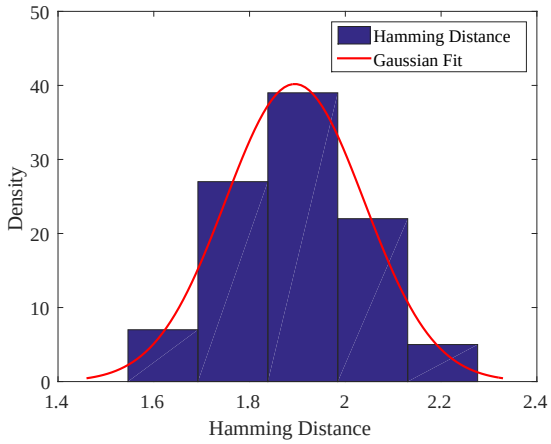


Fig. 10: Intra PUF Hamming Distance of Power Optimized Hybrid Oscillator Arbiter PUF.

C. Average Power

The average power consumed is always a major FoM. In devices that run on battery, low power should be consumed or the introduced module will be of no use at that point. In applications like routers or network switches, speed should be very high to reduce the data latency. Figs. 11 and 12 show the power consumption of the speed optimized and power optimized hybrid oscillator arbiter PUFs. The power optimized design does show lower consumption due to the smaller number of flip flops present in the design. The average power is the sum of all the leakage powers and the dynamic power.

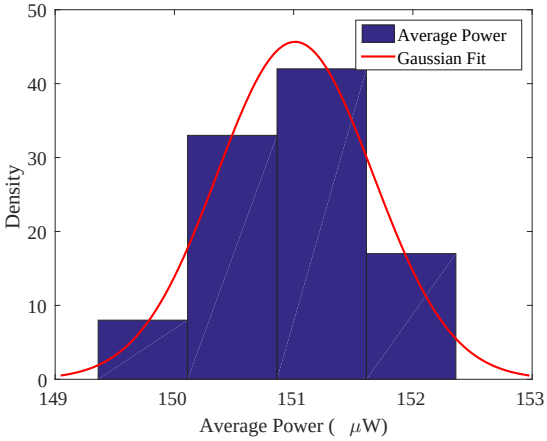


Fig. 11: Average Power of Speed Optimized Hybrid Oscillator Arbiter PUF.

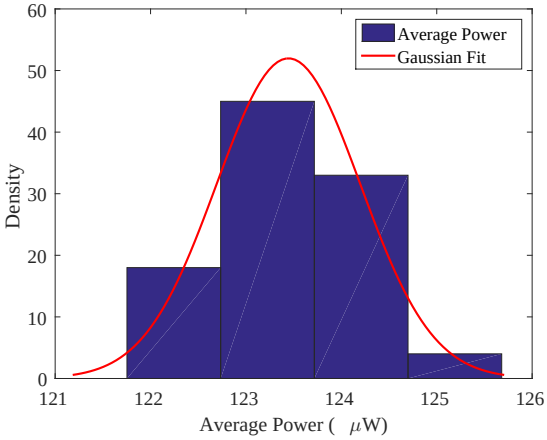


Fig. 12: Average Power of Power Optimized Hybrid Oscillator Arbiter PUF.

D. Time taken to Generate the PUF Key

The time taken to generate the PUF key is another main FoM which plays an important role in high performance devices. In the case of router or network switches, the number of devices connected at a time will be high. So to encrypt and decrypt every incoming and outgoing message, the PUF key generation should be fast. In such cases, to decrease latency, the multiplexers in the power optimized design were removed and a number of D flip flops are added in the speed optimized design. As each pair of oscillators has a separate D flip flop, the time needed to generate the key will be the time the circuit runs until a chosen point of time. For example, in the simulations performed, the output key was recorded after running the circuit for 50ns. In the power optimized design, the total time taken to generate the key will be more than 150ns as the multiplexers are used to select the signals from oscillators and between each selection a small time gap is given. Thus each of the designs can be used for their respective application.

TABLE III: Comparison of Results with Related Existing Research.

Research Works	Technology	Architecture Used	Average Power Consumed	Hamming Distance (%)
Rahman et al. [23]	90 nm CMOS		–	50
Maiti et al. [19]	180 nm CMOS	Traditional Ring Oscillator	–	50.72
Suh et al. [24]	–		–	46.15
Maiti et al. [18]	–	–	–	47.31
Yanambaka et al. (Power Optimized) [20]	32 nm FinFET	Current Starved Oscillator	175.5 μW	50.1
Yanambaka et al. (Power Optimized) [10]	32 nm FinFET	Traditional Ring Oscillator	285.5 μW	50.9
This Paper (Power Optimized)	10 nm Dopingless FET	Hybrid Oscillator Arbiter	121.3 μW	48.0
This Paper (Speed Optimized)	10 nm Dopingless FET	Hybrid Oscillator Arbiter	151 μW	50.0

VII. Conclusion and Future Research

This paper presents two designs of hybrid oscillator arbiter PUFs, a speed optimized and a power optimized design using DL-FETs. A fair comparison of the two technologies, FinFET and DL-FETs is presented in this paper to show a power reduction using these transistors. As a future research, an ultra low power design of PUF can be implemented as these transistors show a promise for usage in low power applications. A newer design of PUF will also be developed with these transistors which will have scope of reconfigurability and generate multiple keys accordingly. An SRAM based PUF using these transistors can also be implemented as DL-FETs are more stable which might give an advantage in designing better SRAMs. The speed optimized design, gives only one key. As a future research, a configurable model of the speed optimized hybrid oscillator arbiter PUF can be designed and characterized.

References

[1] Nvidia, http://www.geforce.com/.

[2] S. P. Mohanty, *Nanoelectronic Mixed-Signal System Design*. McGraw-Hill Education, 2015, no. 9780071825719.

[3] A. Kranti, R. Yan, C. W. Lee, I. Ferain, R. Yu, N. D. Akhavan, P. Razavi, and J. Colinge, "Junctionless Nanowire Transistor (JNT): Properties and Design Guidelines," in *Proceedings of the European Solid State Device Research Conference*, 2010, pp. 357–360.

[4] M. S. Parihar, D. Ghosh, and A. Kranti, "Single Transistor Latch Phenomenon in Junctionless Transistors," *Journal of Applied Physics*, vol. 113, no. 18, 2013.

[5] Z. Chen, Y. Xiao, M. Tang, Y. Xiong, J. Huang, J. Li, X. Gu, and Y. Zhou, "Surface-Potential-Based Drain Current Model for Long-Channel Junctionless Double-Gate MOSFETs," *IEEE Transactions on Electron Devices*, vol. 59, no. 12, pp. 3292–3298, Dec 2012.

[6] C. Sahu and J. Singh, "Potential Benefits and Sensitivity Analysis of Dopingless Transistor for Low Power Applications," *IEEE Transactions on Electron Devices*, vol. 62, no. 3, pp. 729–735, 2015.

[7] C. Sahu and J. Singh, *Junction and Doping-Free Transistors for Future Computing*, ser. Nano-CMOS and Post-CMOS Electronics: Devices and Modelling. Institute of Engineering and Technology, 2015, vol. 1, ch. 5, pp. 139–168.

[8] National Intelligence Council, "Six Technologies with Potential Impacts on US Interests out to 2025," *Disruptive Civil Technologies*, 2008.

[9] S. P. Mohanty, U. Choppali, and E. Kougianos, "Everything You wanted to Know about Smart Cities," *IEEE Consumer Electronics Magazine*, vol. 5, no. 3, pp. 60–70, July 2016.

[10] V. P. Yanambaka, S. P. Mohanty, and E. Kougianos, "Novel FinFET based Physical Unclonable Functions for Efficient Security in Internet of Things," in *Proceedings of the 2nd IEEE International Symposium on Nanoelectronic and Information Systems (iNIS)*, 2016, pp. 172–177.

[11] D. Ghai, S. P. Mohanty, and G. Thakral, "Comparative Analysis of Double Gate FinFET Configurations for Analog Circuit Design," in *Proceedings of the 56th IEEE International Midwest Symposium on Circuits & Systems (MWSCAS)*, 2013, pp. 809–812.

[12] V. Shrivastava, A. Kumar, C. Sahu, and J. Singh, "Temperature Sensitivity Analysis of Dopingless Charge-Plasma Transistor," *Solid-State Electronics*, vol. 117, pp. 94–99, 2016.

[13] M. Panchore, J. Singh, S. P. Mohanty, and E. Kougianos, "Compact Behavioral Modeling and Time Dependent Performance Degradation Analysis of Junction and Doping Free Transistors," in *Proceedings of the 2nd IEEE International Symposium on Nanoelectronic and Information Systems (iNIS)*, 2016, pp. 194–199.

[14] P. Sundaravadivel, S. P. Mohanty, E. Kougianos, and U. Albalawi, "An Energy Efficient Sensor for Thyroid Monitoring Through the IoT," in *Proceedings of the 17th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE)*, 2016, pp. 1–4.

[15] M. O'Neill, "Insecurity by Design: Today's IoT Device Security Problem," *Engineering*, vol. 2, no. 1, pp. 48–49, 2016.

[16] N. Sklavos, "Securing Communication Devices via Physical Unclonable Functions (PUFs)," in *Information Security Solutions Europe*, 2013.

[17] Y. Hori, T. Yoshida, T. Katashita, and A. Satoh, "Quantitative and Statistical Performance Evaluation of Arbiter Physical Unclonable Functions on FPGAs," in *Proceedings of the International Conference on Reconfigurable Computing and FPGAs*, 2010, pp. 298–303.

[18] A. Maiti, J. Casarona, L. McHale, and P. Schaumont, "A Large Scale Characterization of RO-PUF," in *Proceedings of the IEEE International Symposium on Hardware-Oriented Security and Trust (HOST)*, 2010, pp. 94–99.

[19] A. Maiti and P. Schaumont, "Improved Ring Oscillator PUF: An FPGA-friendly Secure Primitive," *Journal of Cryptography*, vol. 24, no. 2, pp. 375–397, 2010.

[20] V. P. Yanambaka, S. P. Mohanty, and E. Kougianos, "Secure Multi-Key Generation Using Ring Oscillator based Physical Unclonable Function," in *Proceedings of the 2nd IEEE International Symposium on Nanoelectronic and Information Systems (iNIS)*, 2016, pp. 200–205.

[21] M. Panchore, J. Singh, and S. P. Mohanty, "Impact of Channel Hot Carrier Effect in Junction and Doping-free Devices and Circuits," *IEEE Transactions on Electron Devices*, vol. 63, no. 12, p. 10.1109/TED.2016.2619621, 2016.

[22] C. Sahu and J. Singh, *Junction and Doping-Free Transistors for Future Computing*, ser. Nano-CMOS and Post-CMOS Electronics: Devices and Modelling. Institute of Engineering and Technology, 2015, vol. 1, ch. 6, pp. 139–168.

[23] M. T. Rahman, D. Forte, J. Fahrny, and M. Tehranipoor, "ARO-PUF: An Aging-Resistant Ring Oscillator PUF Design," in *Proceedings of the Design, Automation Test in Europe Conference Exhibition (DATE)*, 2014, pp. 1–6.

[24] G. E. Suh and S. Devadas, "Physical Unclonable Functions for Device Authentication and Secret Key Generation," in *Proceedings of the 44th ACM/IEEE Design Automation Conference*, 2007, pp. 9–14.