Compact Modeling of Graphene Barristor for Digital Integrated Circuit Design

Zhou Zhao, Xinlu Chen, Ashok Srivastava, Lu Peng
Division of Electrical and Computer Engineering
Louisiana State University
Baton Rouge, LA 70803, U.S.A.
{zzhao13, xchen67, eesriv, lpeng}@lsu.edu

Saraju. P. Mohanty
Department of Computer Science and Engineering
University of North Texas
Denton, TX 76207, U.S.A.
saraju.mohanty@unt.edu

***Abstract*— Graphene barristor, in which a Schottky barrier formed between graphene layer and silicon layer can widen the bandgap with the control of gate voltage, is a promising method to enhance on/off current ratio in digital circuit design. In this work, a theoretical study is presented based on analog behavior modeling in SPICE. We have developed a compact device model to evaluate the performance of graphene barristors. The device simulation results show the on/off current ratio nearly 10^5 under the voltage variation which agrees closely with the reported experimental results. A complementary inverter is designed using the developed model to prove the feasibility of graphene barristor for use in future digital VLSI design. The energy per switching is between 1.1~0.52fJ under voltage variation.**

Keywords—Graphene Barristor, Schottky Barrier, Transistor Modeling, IC Design

I. INTRODUCTION

Graphene-based devices have been recently proposed and can work under a very low power supply with much higher mobility than the widely used silicon devices [1, 2, 3]. However, the property of zero bandgap is a major problem blocking graphene to be integrated in current digital IC design [4]. The suitability of a transistor used for digital circuits depends on that the transistor channel to be semiconducting so as to provide a large on/off current ratio. Both graphene nanoribbon and bi-layer graphene have demonstrated to be semiconducting with a desirable bandgap for transistor switching action. Graphene nanoribbon FET and bilayer graphene FET have been reported [5, 6]. The graphene nanoribbon FET can be used for the digital circuit design for low-power operation [7]. But the current fabrication process cannot support complex nanoribbon embedded into chips and the edge effect can largely influence the practical performance. Bilayer graphene FET needs high voltage to get the required bandgap which is not suitable for energy saving design.

A new graphene based device, graphene barristor, has been introduced recently [8, 9]. The difference between a graphene barristor and a normal graphene transistor is that a Schottky barrier, formed by the graphene layer and the silicon layer, is added to generate barrier height between the gate node and the source node. This barrier height can largely widen the bandgap

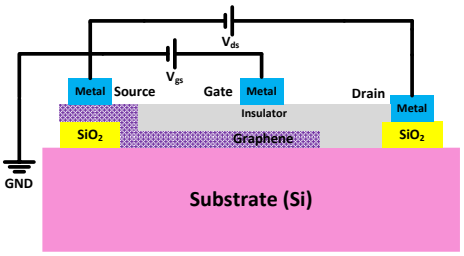


Fig. 1. Cross section view of graphene barrister.

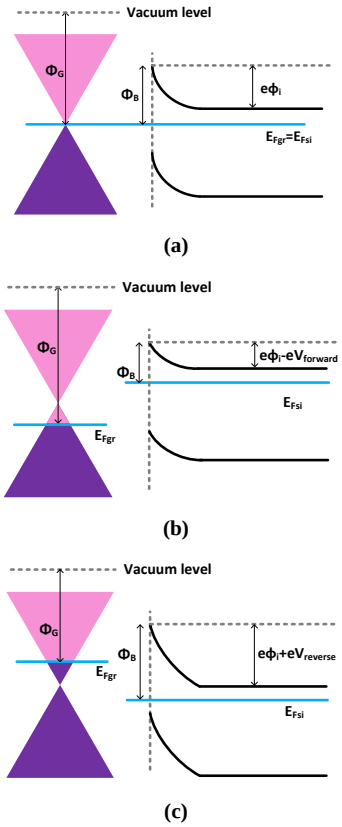


Fig. 2. Energy band diagram of graphene/n-type silicon under a) zero bias, b) forward bias and c) reverse bias.

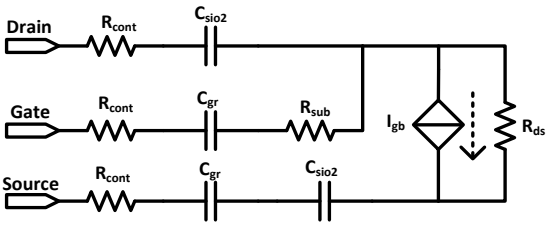


Fig. 3. Equivalent circuit of a graphene barrister.

so that the device can be used for digital logic. Design and analysis of graphene barrier-based integrated circuits require a physical device model which can be used either in SPICE or Verilog-A for simulations.

In this work, we have used analog behavior modeling in SPICE to model the graphene barristor and its circuits. The analog behavior modeling method can dynamically adjust each current and voltage in the device according to the variation of voltage. At the same time the parasite passive devices can be changed due to voltage/current variation and at the same time increase the simulation accuracy. Using analog behavior modeling, we have developed an accurate device model including source block and passive devices to simulate graphene barristor. We have demonstrated the feasibility of use of graphene barristers through the design of a complementary inverter.

The paper is organized as follows. Section II presents physics behind the modeling of graphene barrister, the equivalent circuit model and analog behavior modeling in SPICE. Section III presents design of a complementary inverter based on graphene barrister followed by the conclusion in Section IV.

II. Modeling Graphene Barristor

The cross section view of a graphene barristor is shown in Fig. 1. It can be seen that there is a graphene-silicon Schottky barrier formed around the source node and the gate node. The study regarding the graphene-silicon junction has been reported in [10]. For the analysis, it is defined that forward bias and reverse bias are positive voltage applied in graphene layer and silicon layer, respectively. Taking the graphene/n-type silicon junction as an example, the energy band diagrams under thermal equilibrium, forward bias and reverse bias conditions are shown in Fig. 2. When forward bias is applied as shown in Fig. 2 (b), the built-in potential will be reduced so that electrons are easy to go from silicon to graphene generating a forward bias current. A very different phenomenon compared to the traditional metal-silicon Schottky junction is that the Fermi level of graphene in this case will be moved down due to negative charges in graphene which need to mirror positive charges in silicon. While in the case of reverse bias, the tendency of graphene Fermi level

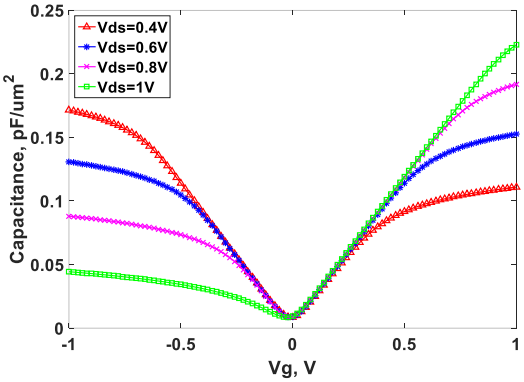
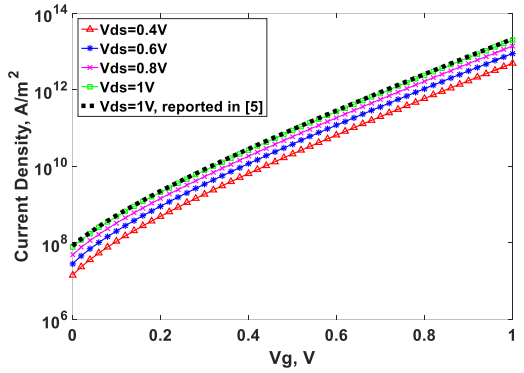
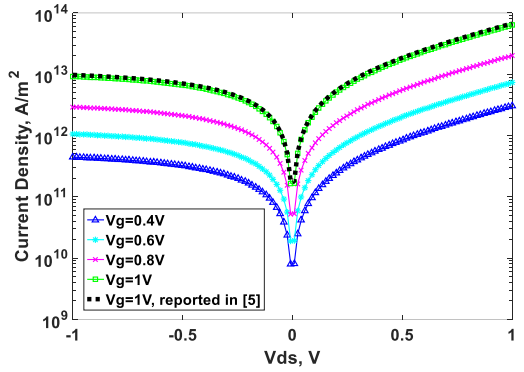


Fig. 4. Graphene capacitor variation versus gate voltage for different drain-source voltages.



(a)



(b)

Fig. 5. The simulated current: a) gate voltage dependence and b) drain-source voltage dependence.

and built-in potential are opposite. The essence of the graphene/silicon junction is formation of a diode with two nodes. To achieve a three-node device needed for a digital circuit, a drain node is added to extend the diode to a FET-like structure. The potential of the drain can control the whole

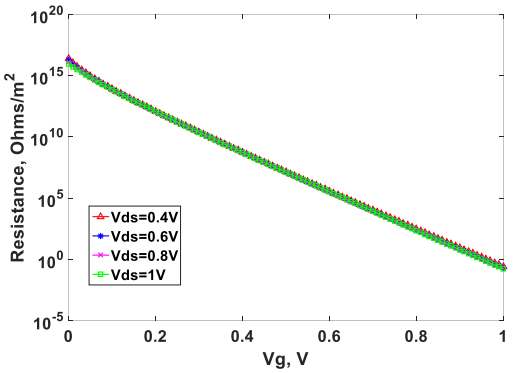


Fig. 6. Output resistance variation versus gate voltage.

current going through the device. When the potential of the drain is the same as of source, from the view of the device, the net current will be zero since there is no voltage difference between the source and the drain. Thus, with the gate control and drain-source control the graphene barristor can perform like a typical FET with three nodes that can be used in digital circuit design. The following section mathematically analyzes the I-V characteristics and parasite passive devices existing in graphene barristor.

We make few practical assumptions based on the dimensional restriction of graphene barrister which are as follows.

1) The graphene layer in a graphene barristor is not as narrow as in a graphene nanoribbon, we can use ballistic directed moments for 3D carriers to analyze the current transport and ignore edge effects.

2) The graphene layer of the barristor is over the silicon substrate, we can ignore the surface states and other effects like crystal defects, and traps between the interface and substrate.

3) The effective length of graphene layer forming the Schottky junction is very short. We do not take scattering effect into consideration.

4) The current through the device is in horizontal direction. Thus, the image force existed in vertical direction can be neglected.

According to Fig. 1, the equivalent circuit of graphene barristor can be shown as in Fig. 3. Once each parameter in equivalent circuit is determined, the model in SPICE using analog behavior modeling can be developed.

For the calculation of capacitor in a graphene barristor, first start with the charge balance considering metal, silicon, and oxide silicon [11] which can be expressed by the Eq. (1) as follows:

$$\begin{cases} Q_m + Q_{gr} + Q_{si} = 0 \\ Q_m = \dfrac{\varepsilon_m (V_g - V_{gr})}{t_{ox}} \\ Q_{gr} = \dfrac{2q}{\pi}\left(\dfrac{kT}{\hbar v_f}\right)^2 \left[\zeta_1\left(-\dfrac{qV_{gr}}{kT}\right) - \zeta_1\left(\dfrac{qV_{gr}}{kT}\right)\right] \\ Q_{si} = \dfrac{\Phi_d}{|\Phi_d|}\sqrt{2\varepsilon_{si}kTN_d}\sqrt{\left[\exp\left(-\dfrac{q\Phi_d}{kT}\right) + \dfrac{q\Phi_d}{kT} - 1\right] + \dfrac{n_i^2}{N_d^2}\left[\exp\left(\dfrac{q\Phi_d}{kT}\right) - \dfrac{q\Phi_d}{kT} - 1\right]} \end{cases} \quad (1)$$

where ε_m and ε_{si} are the permittivity constants of metal contact and silicon, respectively. t_{ox} is the thickness of silicon dioxide, V_g is the external gate voltage, V_{gr} is the potential of graphene surface, q is the unit electron charge, k is the Boltzmann constant, T is the temperature (default temperature is 300K for the following analysis), is the reduced plank constant, Φ_d is the potential of silicon surface, v_f is the Fermi velocity in graphene, n_i is the intrinsic carrier concentration in silicon, N_d is the doping concentration in silicon. ζ_1 is the Fermi-Dirac integral of order one. To obtain the value of capacitor, it is obvious that in above equations both Φ_d and V_{gr} need to be obtained. The function Φ_d with these two parameters can be expressed as follows:

$$\Phi_d = \Phi_{bo} - V_{gr} + V_{ds} + \frac{kT}{q}\zeta_{1/2}^{-1}\left[\frac{N_d h^3}{2(2.16\pi m_o kT)^{3/2}}\right] \quad (2)$$

Where Φ_{bo} is the barrier height for the device under zero bias, and is set to 0.5V in the case of graphene/silicon junction. h is the Planck's Constant, and m_o is the unit electron mass. And $\zeta_{1/2}^{-1}$ is the inverse Fermi-Dirac integral with order of 0.5.

The next step is to transfer charge value to a capacitance value. The silicon oxide capacitor is contributed by the voltage difference between the gate and graphene layer. The graphene capacitor is contributed by the potential of the graphene layer. Using above analysis with t_{ox}=1nm, T=300K, and $N_d=10^{22}m^{-3}$, the graphene capacitor dependence on the gate voltage for four drain-source voltages is shown in Fig. 4. We can see that graphene capacitor is below 0.25pF/μm^2 with voltage variations. The graphene capacitor is proportional to the drain-source voltage, meaning that when drain-source voltage increases, the control ability for logic switch will be stronger from the perspective of circuit design. Another capacitor, silicon dioxide capacitor also exists in the silicon oxide layer, which depends upon the gate voltage.

In the analysis regarding capacitance, we can get potentials of the graphene surface and the silicon layer, which are needed to calculate the current. The original current density function can be expressed as follows [11]:

$$J = A^* T^2 \exp\left(-\frac{q\Phi_b}{kt}\right)\exp\left[1 - \exp\left(-\frac{qV_{ds}}{kt}\right)\right], \quad (3)$$

where A^* is the effective Richardson constant. For Φ_b, the barrier height, it can be expressed by the following:

$$\Phi_b = \Phi_{bo} - V_{gr}. \quad (4)$$

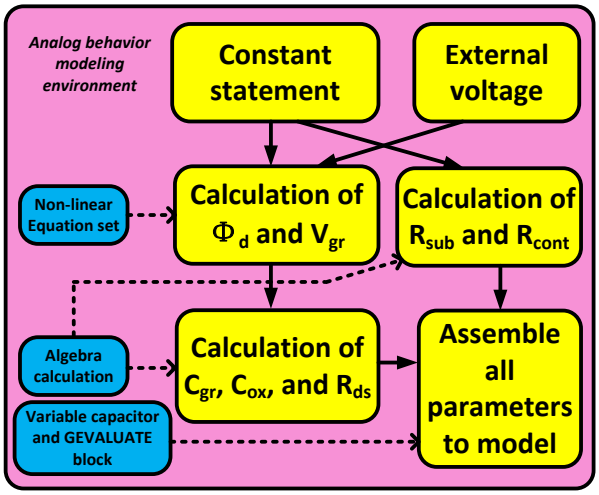


Fig. 7. Modeling of a graphene barristor.

Thus, the current density can be shown as follows:

$$J = A^{*}T^{2}\exp\left(\frac{q\left(V_{gr}-\Phi_{bo}\right)}{kt}\right)\left[1-\exp\left(-\frac{qV_{ds}}{kt}\right)\right] \tag{5}$$

To verify the current analysis, first we use the gate voltage as the variable under fixed drain-source voltage to calculate the current density. Then take the drain-source voltage as a variable under the fixed gate voltage to simulate the current density. Both results are shown in Fig. 5, which are in agreement to the reported results in [8] from the quantitative view. It can be seen that the ratio of switch-on current to switch-off current is closed to 10^5, which is a practical value to use with graphene barristor based digital circuit design.

The output resistor between the drain and the source can be obtained by taking a derivative of current function with respect to drain-source voltage. The simulated result is shown in Fig. 6. We observe from Fig. 6 that the output resistance of graphene barristor is not sensitive to the drain-source voltage. This fact is due to the modulation by the potential of the silicon layer and the potential of the graphene layer. The resistance of the substrate can be calculated by [12]:

$$R_{sub} = \frac{2t_{sub}}{q\mu_e N_d A_{cont}}, \tag{6}$$

where t_{sub} is the thickness of substrate, μ_e is the electron mobility in silicon substrate, and A_{cont} is the effective contact area between silicon substrate and graphene layer contributing current channel.

The resistance of metal/graphene contact, which connects the drain, source, and gate nodes also contributes to the performance of circuit operation. We extract the experimental result from [13] for the case of monolayer graphene contacting with metal. The contact resistance is set to 800Ω for our modeling. It can be seen that I-V characteristics presented in Fig. 5 agrees with the experimental results of [8] which proves the validity of the current transport model of graphene barrister presented in this work.

The device modeling in SPICE can be done by a controlled source (e.g. VCCS, CCCS, VCVS, and CCVS), a look-up table, and fixed passive devices. However, the controlled source provided by SPICE only can implement simple linear calculations to get approximated voltage/current results. But emerging novel devices require much non-linear analysis to accurately narrate device characteristic. The look-up table is an efficient method to model a novel device. This method can also reduce simulation time since there is only read and write request. Going to circuit design, imperfect logic transferring due to clock skew and inadequate charge/discharge will cause large pulse currents or voltages. In this case, if an overlarge voltage or current is not stored in the look-up table, the simulation will fail due to lack of enough information to be searched. The unwanted pulse current or voltage is also randomly generated according to circuit structures. Thus, it is very difficult to calculate and store all needed information in the look-up table dealing with various circuits.

Analog behavior modeling [14, 15] is a module in SPICE, which can implement complex non-linear calculations regarding both voltage and current. The detailed calculation function includes addition, subtraction, multiplication, division, calculus, absolute function and exponential function, all of which can well satisfy our modeling needs according to the previous analysis. With the help of these calculation functions, analog behavior modeling can solve non-linear equations. Besides, analog behavior modeling has a limitation block which can restrict input signal in a reasonable range to avoid unwanted signal processing reducing the simulation accuracy. For the transmission between voltage and current to achieve the voltage-control device and capacitor, analog behavior modeling has an evaluate block which can transfer voltage to current under self-defined principles. Analog behavior modeling has the function of parameter statement, which means that all constants can be stated globally, and used for the entire modeling. This function largely improves the design efficiency.

For the modeling of graphene barristor with our previous analysis, we can find both potentials of the graphene surface and the silicon surface, two important variables which are related to graphene capacitance, silicon oxide capacitance, output resistance, and device current. When these two parameters are solved, with the definition of other constants and the input voltage such as gate voltage and drain-source voltage, required graphene capacitance, silicon oxide capacitance, output resistance, the device current can be solved smoothly. For other parameters serving for modeling, substrate resistance and graphene/metal resistance, these can be easily calculated by constants without variables.

In our modeling, the dimension of graphene layer is set to be the same as in [9]. The length is 20nm and width is 1μm. The

Table I. Comparison between graphene barristor and emerging technologies.

	FinFET			Bilayer Graphene FET	This work		
	By the Year				By the Supplied Voltage		
	2019	2024	2027		1V	0.8V	0.6V
t_{ox} (nm)	0.9	0.8	0.8	N/A	1	1	1
L_{ch} (nm)	12	8	6	40	20	20	20
V_{dd} (V)	0.7	0.5	0.45	0.2	1	0.8	0.6
I_{on}/I_{off}	5.5×10^{7}	2×10^{7}	8.5×10^{6}	2.91×10^{3}	0.94×10^{5}	0.93×10^{5}	0.92×10^{5}
Cg (fF)	1.47	1.24	1.24	0.32	1.12	1.07	1.06
E_{switch} (fJ)	1.89	0.94	0.63	0.013	1.1	0.607	0.52

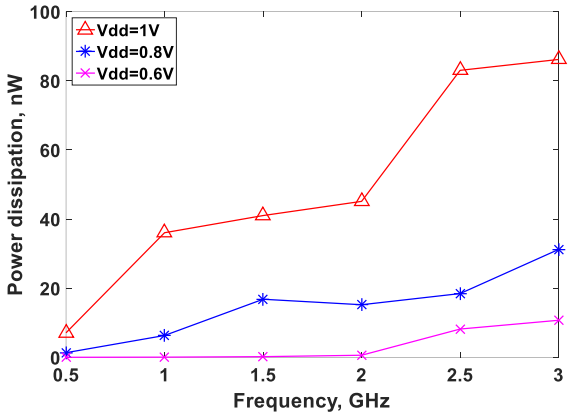


Fig. 8. Graphene barrister based inverter performance: power dissipation dependence on frequency.

thickness of the silicon oxide and the substrate are 1nm and 0.3mm, respectively. The modeling flow of graphene barristor is shown in Figure 7 and described as follows:

1) State all constants which will be used for the mathematical analysis.

2) Calculate both potentials of silicon surface and graphene surface. These two parameters can be solved with a set of Eq. (1) and Eq. (2).

3) Using stated constants and both potentials of silicon surface and graphene surface calculated in Step 2, calculate graphene capacitance, silicon oxide capacitance, and device current. Two kinds of capacitors are outputted by the variable capacitor. The current of graphene barristor is outputted by GEVALUATE which is a block and can transfer voltage to current by a self-defined equation in SPICE. At the same time, using constants, calculate substrate resistance and graphene/metal contact resistance.

4) Combine all calculated parameters in Step 3 following the equivalent circuit model in Fig. 3.

Using modeling flow in Fig. 7, we can model both n-type and p-type graphene barristors with different doping categories.

III. Graphene Barristor Based Circuit Design

The analyses of the current means that both forward bias and reverse bias conditions have a current to achieve a digital logic. We notice that the current under reverse bias is smaller than under the forward bias. And the on/off current ratio under the forward bias is larger than under the reverse bias, which means that using graphene barristor under the forward bias is more suitable for the digital logic design. We use both forward bias and reverse bias operation to design a circuit finding that even though the power dissipated in reverse bias condition is smaller than in the forward bias condition, the signal integrity in reverse bias condition is much worse than in the forward bias condition. Thus, we choose the way of forward biasing to build the circuit. With this method, the logic design using graphene barristors is same as in traditional CMOS and FinFET, which has both pull-down n-type tree and pull-up p-type tree combined to obtain a complementary topology.

For low power design, in the simulation, we set 1V, 0.8V, and 0.6V as three supply voltages cases to study. To evaluate the performance of digital circuit using the proposed model of graphene barristor, we designed a complementary inverter for power dissipation versus frequency dependence. Figure 8 shows the simulation results. From the simulation results, we can see that in most of the cases gate logic under 1V supply dissipates more power than under the reduced supply voltages. To evaluate the feasibility of the proposed device, we compared few parameters, on/off current ratio, gate capacitance and switching energy with other emerging devices [16, 17, 18]. The results are summarized in Table I. From Table I, we can observe that the barristor uses relatively large channel length and I_{on}/I_{off} ratio is

within the acceptable range; and from the view of power dissipation and gate capacitance, graphene barristor is a competitive candidate which can be used for the digital circuit design.

IV. Conclusion

In this work, a compact and simple current transport model of a graphene barristor is presented. Using analog behavior modeling, an accurate SPICE model is proposed. The proposed model can be adjusted dynamically by the voltage variation for accurate simulations. The simulation results show that graphene barristor can be used for low power digital circuit design. The future work would focus on the scaling of device dimension and improvement in I_{on}/I_{off} ratio.

Acknowledgment

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