Graphene Nanoribbon Field Effect Transistor based Ultra-Low Energy SRAM Design

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***Abstract*—Silicon-based Static Random Access Memory (SRAM) has not been keeping pace with technology trends due to the limited improvements in power, performance and density. This paper explores graphene based SRAM as a potential replacement of silicon SRAM for future digital electronics. Due to its higher current on-to-off ratio, the graphene nanoribbon field effect transistor (GNRFET) has been considered in this paper. In the nanometer regime, process variation is not only inevitable but also very pronounced. To mitigate its effects as much as possible, the Schottky-Barrier type GNRFET is considered which presents lower variation in its characteristics due to doping variation. The results show that graphene nanoribbon has a great potential in digital circuit design. The GNRFET based SRAM design presented in this paper leads to significantly lower power consumption, approximately 93% compared to 45 nm silicon technology. This upper bound can be quite achievable as the fabrication technology of graphene reaches maturity.**

***Keywords*-Graphene Nanoribbon FET (GNRFET), Static Random Access Memory (SRAM), Ultra-Low Power Design**

I. Introduction

The semiconductor industry has been depending heavily on silicon based Field Effect Transistors (FETs) for digital circuit implementation. However, as the Complementary Metal Oxide semiconductor (CMOS) technology reaches the fundamental power wall, i.e. the non scaling of KT/q and hence of V_{th} and V_{DD} below the 10 nm regime, it may not be an easy choice for future electronic devices. Attention has shifted to new device concepts and new device materials such as graphene and carbon nanotube (CNT), as a suitable substitute for conventional transistors. Graphene and CNT based FETs are considered to be a viable solution to the problem due to graphene's high field-effect mobility (as high as 15000 $cm^2/(Vs)$ [1]–[4] and a high Fermi velocity ($\sim 10^8$ cm/s) even at room temperature. Carbon nanotube FETs (CNTFETs) suffer from fabrication problems like gate alignment and incompatibility to planar technology, so it is very likely that graphene would be more suitable to substitute silicon without the need to replace the existing multi-billion dollar silicon based technology.

There are two varieties of GNRFETs: Schottky-Barrier (SB)-type and Metal Oxide Semiconductor (MOS)-type. MOS-type GNRFET has several advantages over SB-type GRFET such as larger maximum on-off ratio due to absence of ambipolar transport, much larger on current, larger transconductance, better saturation behavior due to smaller output conductance, larger cutoff frequency, faster switching speed giving very small delay, and large transconductance [5]. On the other hand, the most important advantage of SB-type GNRFET over MOS-type GNRFET is that there is no doping required in the channel or in the terminals. This reduces the technical difficulties during fabrication as well as the major source of variability [6]. In this work, SB-type GNRFET is considered for the design of digital circuits. A graphene nanoribbon based SRAM is designed and its performance is compared with the 45 nm PTM MOSFET model. The paper uses the novel GNRFET model from [6] and the circuit is implemented and characterized in Cadence.

The rest of this paper is organized as follows: In section II the novel contributions are highlighted. In Section III, the geometry of the graphene nanoribbon field effect transistor (GNRFET) is briefly presented. Section IV illustrates the 6-transistor (6T) SRAM cell based on GNRFET along with experimental results. Conclusions and some possible future directions are examined in section V.

II. Novel Contributions of this Paper

The paper compares the advantages of GNRFET SRAM with silicon based SRAM at the 45 nm technology node, providing detailed cell level characterization as well as array based characterization. To the best of the authors' knowledge, this is the first paper to provide such a detailed level of comparison between GNR and silicon SRAMs in terms of stability and power consumption. In a relevant work [7], a comparison of graphene based SRAM with conventional silicon based SRAM is just limited to power consumption.

III. Graphene Nanoribbon FET

The double gate SB-type GNRFET structure is considered in this paper as it provides better gate control over the channel giving higher on-to-off current ratio. As shown in fig. 1, the SB-GNRFET consists of a GNR-based channel while the gate, drain, and source are metal electrodes. Thus the interface between drain-channel and source-channel forms a Schottky

barrier at the graphene-metal junction. The SB-type GNRFET exhibits ambipolar properties where the minimum current is:

$$V_{GS} = (1/2)V_{DS}. \quad (1)$$

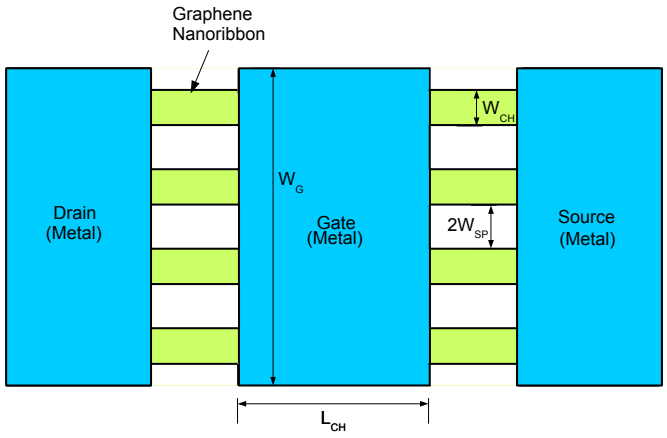


Fig. 1. SB-type GNRFET.

Since the objective in this paper is to determine an upper bound of performance of GNRFET in SRAM applications, edge roughness has not been included. As the fabrication technology matures, the impact of edge roughness will be minimized. Since the channel length is 10 nm, which is less than the mean free path in graphene, carriers exhibit ballistic transport [8]. The GNRFET device geometric parameters used in this work are summarized in Table I.

TABLE I
GNRFET DEVICE PARAMETERS.

Device Parameter	Default Values
Physical channel length	10 nm
Substrate oxide thickness	20 nm
Tog-gate dielectric material thickness	0.95 nm
Spacing between adjacent GNRs	2.0 nm
Number of GNRs	6-10
Number of dimer lines in GNR lattice	12
Edge roughness percentage	0 (Ideal)

IV. GNRFET Based SRAM and Experimental Results

This work considers a 6T configuration. The data is stored in two inverters (T_1, T_2, T_3 and T_4) connected back-to-back as shown in Fig. 2 [9], [10]. SRAM transistor sizing is presented in Table II.

To analyze the SRAM cell stability, normally the butterfly curve and N-curve approaches are used. The N-curve provides information about both read and write stability within a single plot, hence it has become the preferred way of defining SRAM stability [1], [11].

A. Read Stability for SRAM Cell

SRAM cells become less stable with technology scaling due to low supply voltage, increased leakage and increased

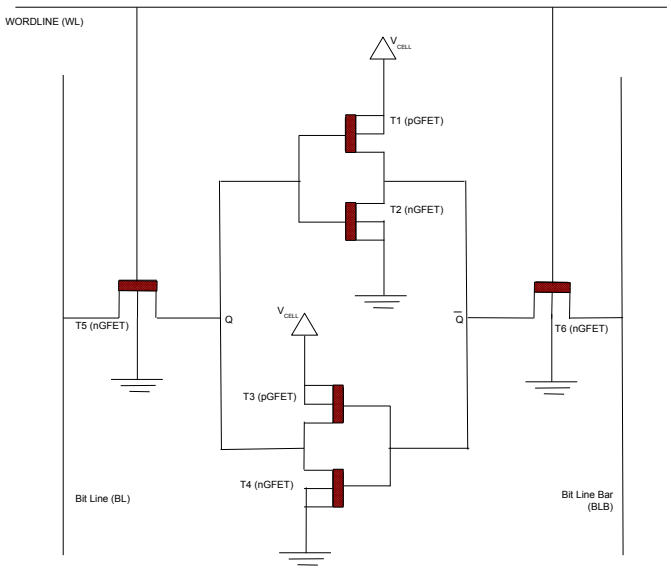


Fig. 2. 6T SRAM configuration.

variability. Considering that node Q is holding "0", during the read operation the voltage at node Q rises above 0 V to the voltage determined by the access transistor T_5 and the pull-down transistor T_4 between the Bitline (BL) and the storage node Q. The voltage at which the memory cell flips its stored state is called the cell trip point. If the voltage at node Q exceeds the trip point of the inverter T_1 and T_2 then the cell will flip its state, causing the read upset. Thus the read stability is determined by the cell ratio (CR) of the cell.

1) Read static noise margin(RSNM)
RSNM, extracted from the read voltage transfer characteristics (VTC), is often used to quantify the SRAM read stability. RSNM represents the maximum DC noise voltage tolerated at each node $(Q/\bar{Q})$ before causing a read upset.

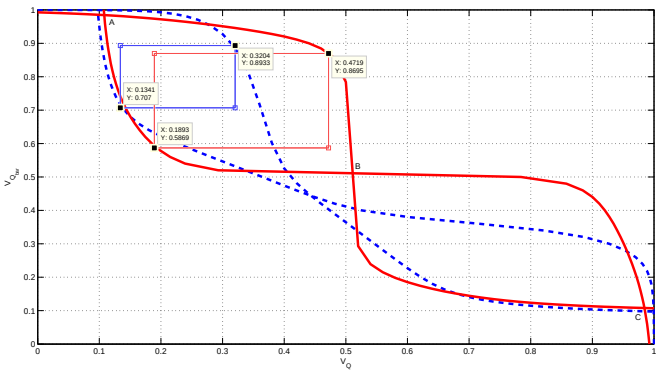


Fig. 3. Simulated waveform for RSNM calculation for GEFT based SRAM (shown by solid red line) and silicon transistor based SRAM (shown by dotted blue line).

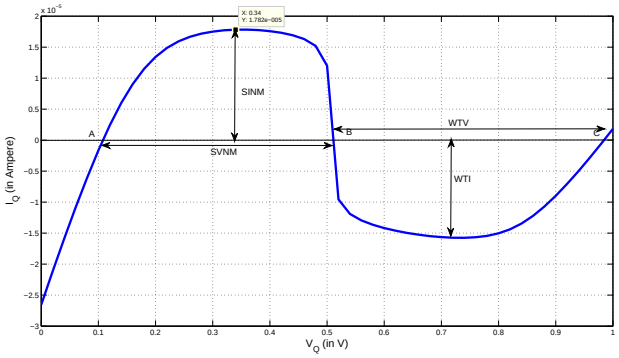
2) Static voltage noise margin (SVNM) and Static current noise margin (SINM)
An alternative approach to measure SRAM stability is

TABLE II
SRAM TRANSISTOR SIZING.

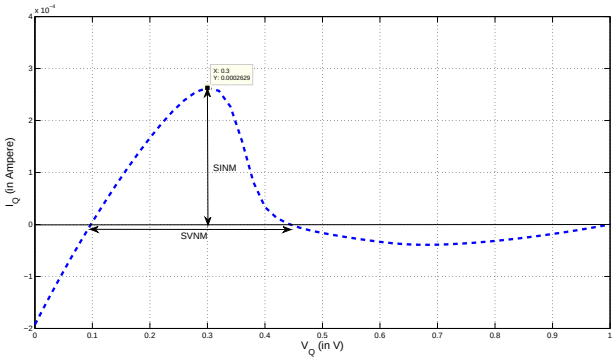
Transistor Type	GNRFET Value	Silicon FET Value
Pullup Transistor	$n_{Rib} = 6$	100 nm (W)
Pulldown Transistor	$n_{Rib} = 10$	400nm nm (W)
Access Transistor	$n_{Rib} = 7$	150 nm (W)

based on the N-curve, which can be easily measured by an inline tester and provides both voltage and current information required for characterizing the read stability of the cell.

To plot the N-curve, the voltage at the storage node Q (or $\bar{Q}$) is swept while keeping the wordline and both bitlines (i.e. BL and BLB) biased at V_{DD} and measuring the external current sourced into node Q (or $\bar{Q}$).



(a) Graphene based SRAM.



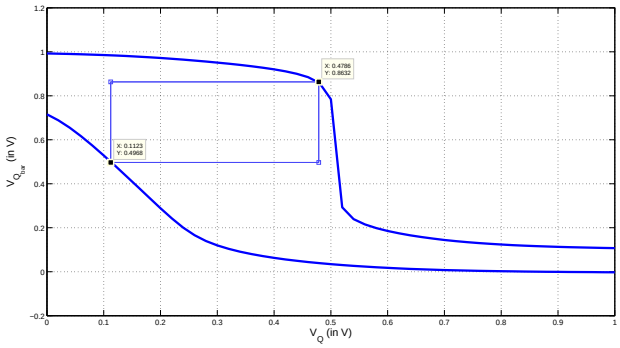
(b) Silicon transistor based SRAM.

Fig. 4. Simulated waveform for SINM calculation.

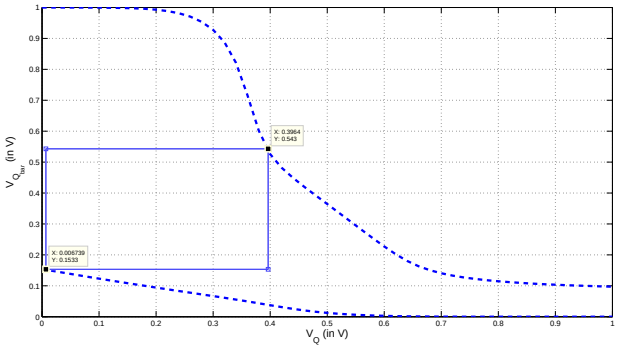
It can be seen from Fig. 4 that graphene SRAM offers higher SVNM, which is approx. 400 mV compared to that of the silicon based SRAM, which is around 340 mV. However the SINM value in graphene based SRAM is much smaller than that of silicon based SRAM.

B. Write-ability for SRAM Cell

Considering the internal storage node Q is holding "0", if the transistor pairs T_5 and T_1 pull the voltage at node $\bar{Q}$ below the trip point of the inverter, a successful write operation can be performed. Thus the write noise margin (WNM) can be extracted using read VTC and write VTC, where write VTC is measured by sweeping the voltage at the storage node Q while keeping BL and WL biased at V_{DD} and BLB to ground and monitoring the voltage at node $\bar{Q}$. The side of the smallest square between the read VTC and write VTC gives the WNM. If the write VTC and the read VTC intersect each other, then the cell is not able to write correctly.



(a) Graphene based SRAM.



(b) Silicon transistor based SRAM.

Fig. 5. Simulated waveform for WNM calculation.

As can be seen from Fig. 5 the write noise margin is less in GFET based SRAM as compared to silicon transistor based SRAM. The WNM for GFET based SRAM is 366 mV while that in silicon based SRAM is 390 mV.

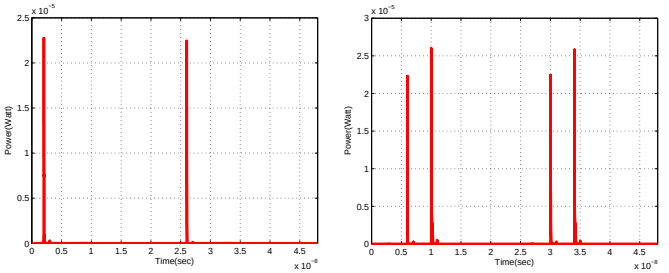
TABLE III
CELL STABILITY COMPARISON.

Description	GFET Based SRAM	Silicon FET Based SRAM
RSNM	282.6 mV	186.3 mV
WNM	366.4 mV	389.7 mV
SVNM	400 mV	340 mV
SINM	17.82 μA	262.9 μA
WTV	470 mV	430 mV
WTI	-16 μA	-40 μA

Table III compares the cell stability of the two SRAMs. SINM (SVNM) is strongly related to read stability while WTI (WTV) is strongly related to writeability. Fig 6 shows the instantaneous power consumption of the GNRFET based SRAM for various cells in the array.

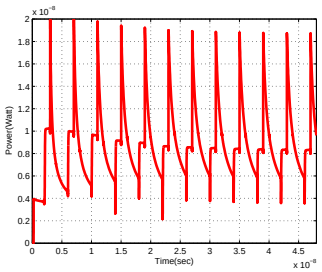
The power consumption profile of the GFET based SRAM with the conventional silicon transistor based SRAM is compared in Table IV.

From Table IV, it can be seen that the average power consumption of the silicon based memory cell far exceeds the

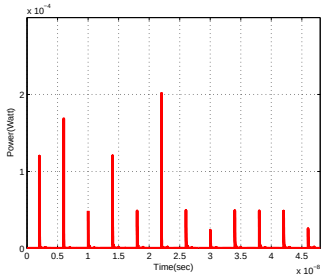


(a) Cell storing '0'

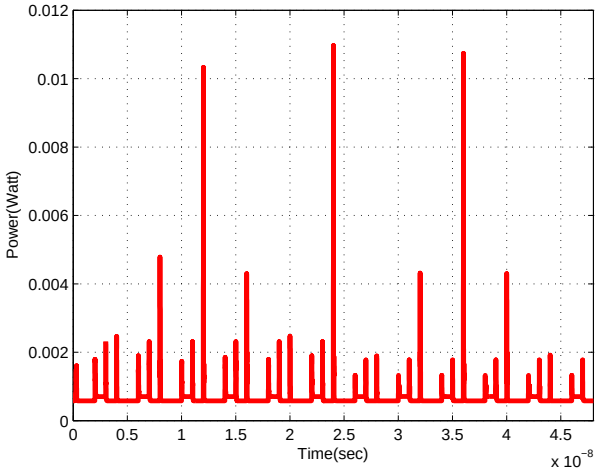
(b) Cell storing '1'



(c) Other cells



(d) All Cells



(e) All circuits

Fig. 6. Instantaneous Power Consumption of GFET based SRAM.

TABLE IV
AVERAGE POWER CONSUMPTION COMPARISON OF SRAM.

Description	GFET Based SRAM	Silicon FET Based SRAM
Cell storing 0	28.71 nW	221.3 nW
Cell storing 1	84.7 nW	330.5 nW
Other cells	8.686 nW	137.4 nW
Array	796.4 nW	11.49 μW

average power consumption by the graphene based memory cells. The use of graphene based SRAM reduces the average power by 93% while maintaining the read and write stability as compared to silicon based SRAM. Hence graphene based circuits are very much applicable in both power constraints as well as area constraint applications.

V. CONCLUSIONS AND FUTURE RESEARCH

The design of digital circuits using graphene nanoribbon has been analyzed under ideal condition with an SRAM used as a case study. The results show that graphene nanoribbon has a great potential in the digital circuit design leading to significant less power consumption, which is approximately 93% as compared to 45 nm silicon technology. The performance degrades with device imperfections like nanoribbon edge roughness etc. However the performance is expected to be close to the ideal, once the technology matures. In future work, a fully functioning 1K$\times$8 array with GNRFET periphery will be designed and characterized.

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