# Compact Behavioral Modeling and Time Dependent Performance Degradation Analysis of Doping and Junction Less Transistors for Analog Designs

Meena Panchore[1], Jawar Singh[2], Saraju P. Mohanty[3], and Elias Kougianos[4]
[1,2]Electronics & Communication Engineering, Indian Institute of Information Tech. Design & Manufacturing, Jabalpur, India.
[3,4]NanoSystem Design Laboratory, Computer Science and Engineering, University of North Texas, Denton, TX 76207, USA.
Email: [1]p.meena@iiitdmj.ac.in; [2]jawar@iiitdmj.ac.in; [3]saraju.mohanty@unt.edu; [4]elias.kougianos@unt.edu

***Abstract*—The time dependent performance degradation of both conventional and dopingless JLFETs under channel hot carrier (CHC) stress for different time spans is investigated at device as well as circuit level. Compact behavioral Verilog-A models of both devices were developed. It was observed that the voltage gain of a Common Source (CS) amplifier designed with conventional JLFET is degraded by 20.2% and 32.6% due to CHC stress of 2000 and 6000 sec., respectively. However, the dopingless JLFET experiences 10-15% degradation for the same time span.**

The dopingless (DL) JLFET has recently attracted the attention of the research community as a potential candidate that relaxes the requirements of high work function of gate metal electrode and heavy doping throughout the source, channel and drain regions, while all the innate benefits of conventional JLFETs are preserved. The DL-JLFET employs intrinsic silicon nanowire, whereas the source and drain regions were formed through charge-plasma [1], thereby it provides better immunity towards process variation induced random dopant fluctuations.

The conventional and dopingless JLFETs are simulated using the Silvaco ATLAS device simulator with default parameters of silicon [3]. Shockley-Read-Hall (SRH) and Auger recombination models have been incorporated to account for minority carrier recombination. The Lombardi mobility model (CVT) has been considered because it gives accurate results with large temperature ranges. The Energy Balance Transport model (EBT) is included for non local transport effects. For analyzing the device degradation (shift in threshold voltage, degradation of transconductance and other parameters) the device degradation model (DEVDEG) is enabled.

The electrical characteristics ($I-V$ and $C-V$) of both devices were extracted using two dimensional TCAD tool for bias conditions varying finely over a wide operating range. The extracted electrical characteristics from the TCAD simulator were used to produce two-dimensional look-up tables. These tables include $I-V$ and $C-V$ data extracted from transfer characteristics of drain current $I_{DS}$, gate to source capacitance $C_{GS}$ and gate to drain capacitance $C_{GD}$ as functions of ($V_{GS}$, $V_{DS}$) across a wide rang of operating voltages through DC and small-signal simulations. Hence, the developed Verilog-A models for both devices are capable of capturing both DC and transient characteristics accurately. We have calibrated our Verilog-A models with TCAD simulations and reproduced the previously reported transfer characteristics of both conventional JLFET and DL-JLFET, as shown in Fig. 1(a-b).

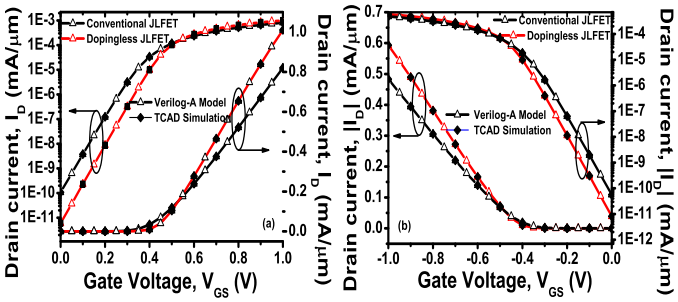


Fig. 1. Calibration of Verilog-A models (open symbols) with TCAD simulations (solid symbols) for transfer characteristics of both conventional (JLFET) and dopingless (DL-JLFET) devices (pre-CHC) at $V_{DS}$= $\pm 1V$ (a) n-type device, and (b) p-type device.

For evaluation of CHC stress, we have applied the stress voltage higher than the nominal stress voltage, therefore the most damaging CHC stress condition at room temperature for short channel transistors has been considered: $V_G$=$V_D$=1.9V for 2000 sec. and 6000 sec. Fresh and degraded device characteristics were estimated by the cumulative measure-stress-measure approach [2].

For CHC stress of 2000 sec., the conventional JLFET experiences drain current degradation of 20.5 % in contrast to dopingless JLFET of 10.4% for $V_G$ = $V_D$ = 1.9 V. Degradation in drain current for both devices mainly occurs due to shift in threshold voltage under CHC stress. However, for lower gate biases both devices experienced less degradation in drain current which is consistent as well as in line of applied electric field. The time dependent degradation in drain current due to CHC stress was also observed for 6000 sec., where drain current degradation was slightly higher for both devices.

## References

[1] R. J.E. Hueting, B. Rajasekharan, C. Salm, and J. Schmitz, "The Charge Plasma P-N Diode," *IEEE Electron Device Letters*, vol. 29, no. 12, pp. 1367-1369, Dec. 2008.

[2] P. Magnone, F. Crupi, N. Wils, H. P. Tuinhout, and C. Fiegna, "Characterization and Modeling of Hot Carrier-Induced Variability in Subthreshold Region," *IEEE Transactions on Electron Devices*, vol. 59, no. 8, pp. 2093-2099, Aug. 2012.

[3] ATLAS Device Simulation Software [Online], Silvaco Inc, Santa Clara, CA, USA, (2014), Available: http://www.silvaco.com.