A Low-Cost Mixed Clock Generator for High Speed Adiabatic Logic

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***Abstract*—Low power and robust circuitry are permanent hotspots in VLSI design. Adiabatic logic is one of potential breakthroughs for these goals. Especially, designing reliable clock tree is very significant for adiabatic logic due to four-phase clocked power required for pipelined data transmission in adiabatic system. In this paper, we present analysis of charging speed and clock types that influence power dissipation in adiabatic logic and comparison of current mainstream clock generators suitable for adiabatic system. Based on the characteristics of current designs, using TSMC 180nm fabrication process, we propose a novel mixed clock generator, including four-phase source, switch controller and clock MUX to build a robust clock using only one reference clock. The test shows that below 600MHz, the proposed design has negligible signal attenuation with low power dissipation. We have also compared our work and current designs in device cost, and suitable work frequency based on circuit structure.**

Keywords—Adiabatic logic; slow charge; mixed clock generator

I. INTRODUCTION

Adiabatic logic is one of effective methods of low power VLSI design [1]. The essence of adiabatic logic includes lowering charging speed and clocked power supply, both of which can reduce power dissipation to a large degree. Lots of work [2, 3, 4, 5] proposed the optimization of adiabatic circuitry, and reported the breakthrough in the view of system using adiabatic logic [6, 7]. Besides, how to drive adiabatic logic using clocked power decides the performance of following system. Currently mainstream adiabatic systems need four-phase clocked power to achieve energy recovery and correct data flow, and most of well used designs are built by integrating passive devices to clock block [8, 9, 10], which occupies more chip area. This paper presents a low cost clocked power driving adiabatic system without passive devices. The main work is described as follows: 1) We mathematically analyzed the slow charge and three types of clocked powers used for adiabatic logic in the view of power dissipation; and 2) Based on the mainstream designs of clocked power, we proposed a novel mixed clock generator without passive devices, driven by a single sinusoidal signal. We used *SPICE* simulation to demonstrate the feasibility of our design.

The rest of this paper is organized as follows. Section II is the analysis of slow charging process and three types of clocked power used in adiabatic system; the proposed design is discussed in Section III; the test results are reported in Section IV; and the summary is presented in Section V.

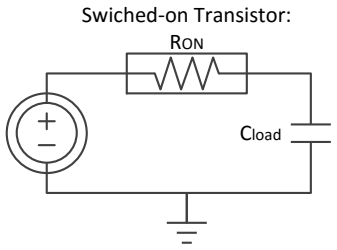


Figure 1 Simple charging model.

II. SLOW CHARGING IN ADIABATIC LOGIC

For digital VLSI, heat is dissipated during fast charging and discharging via switch-on transistors. Figure 1 intuitively shows this process. The current going through the circuit can be shown as follows:

$$i(t) = C_{load}\frac{\partial v_{out}(t)}{\partial t} = \frac{v_{in}(t) - v_{out}(t)}{R_{ON}} \tag{1}$$

Solving above equation, we obtain the following:

$$v_{out}(t) = v_{in}(t)\left(1 - e^{-\frac{t}{R_{ON}C_{load}}}\right) \tag{2}$$

$$i(t) = \frac{v_{in}(t)e^{-\frac{t}{R_{ON}C_{load}}}}{R_{ON}} \tag{3}$$

Thus, power dissipated in the switch can be calculated by:

$$P_{diss} = \frac{v_{in}^2(t)e^{-\frac{2t}{R_{ON}C_{load}}}}{R_{ON}} \tag{4}$$

If input voltage rises from 0 to V_{DD} in linear way, the rise time is T, power dissipation can be described as follows:

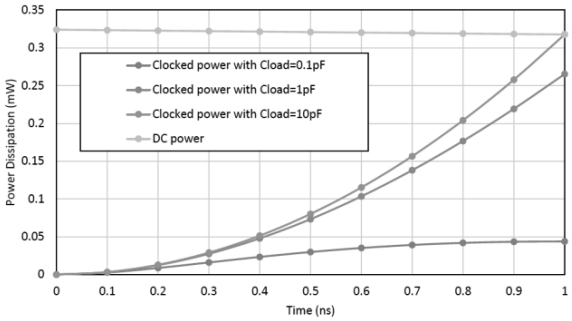


Figure 2 Comparison of power dissipation between constant power and clock power with different loads.

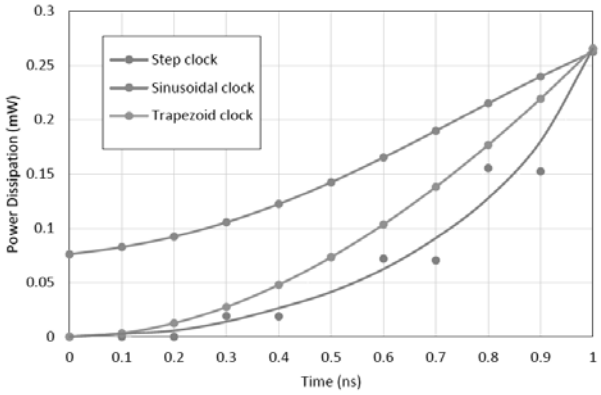


Figure 3 Comparison of power dissipation between three types of clocked power in evaluate/recover stage.

$$P_{diss} = \frac{V_{DD}^2 t^2}{T^2 R_{ON}} e^{-\frac{2t}{R_{ON} C_{load}}} \quad (5)$$

Setting power supply is 1.8V, T is 1ns, R_{ON} is 10kΩ, the power dissipation under DC power and clocked power can be plotted in Figure 2. It gives an indication that the clocked power with slow charge/discharge and small load can reduce power dissipation notably.

Commonly used adiabatic system requires four intervals [1] serving logical transmission (evaluate interval, hold interval, recover interval, and wait interval). To achieve these four intervals, three types of clocked power including step clock, sinusoidal clock and trapezoid clock, are popularly used. The power dissipation of step clock and sinusoidal clock in evaluate stage or recover stage can be shown as follows:

$$P_{diss\_step} = \frac{\left(\frac{V_{DD}}{\alpha}\right)^2 \left[\frac{t}{T_S}\right]^2 e^{-\frac{2T_S}{R_{ON} C_{load}}}}{R_{ON}} \quad (6)$$

$$P_{diss\_\sin} = \frac{V_{DD}^2 \left[\sin\left(\frac{\pi}{2}\frac{t}{T_{\sin}} - \frac{\pi}{4}\right) + 1\right]^2}{4R_{ON}} e^{-\frac{2t}{R_{ON} C_{load}}} \quad (7)$$

where for the step clock, stepping period is T_s, and each interval has α steps, and for the sinusoidal clock, the period is

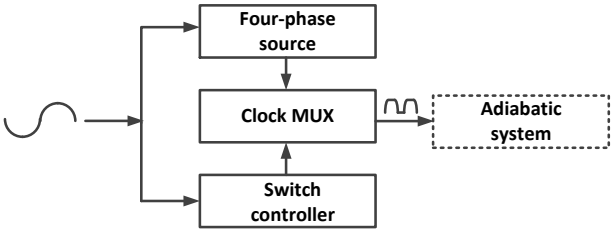


Figure 4 The block diagram of the proposed clock generator.

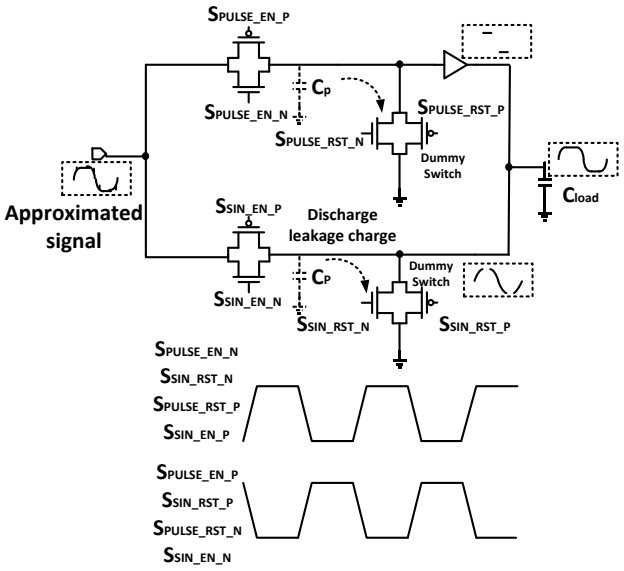


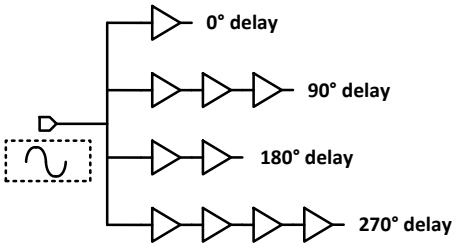
Figure 5 The circuit diagram of clock MUX.

T_{sin}. For the trapezoid clock, it is familiar to the analysis in Eq. (5) for the power dissipation of linear charging process.

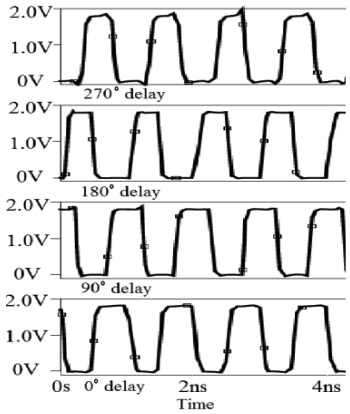
Setting V_{DD} to 1.8V, charging time, 1ns, $R_{ON,}$ 10kΩ, C_{load}, 1pF, and α to be 4 for the step clock, we can get Figure 3 that shows the comparison of power dissipation between three types of clock signals. According to this figure, we can see that for a given load, when only power dissipation is considered, step clock is the best choice for clocked power supply. But from the view of circuit implementation, only power dissipation taken into consideration is not enough [11].

III. MIXED CLOCK GENERATOR

For the step clock, tank capacitor is normally used [8]. For sinusoidal clock, LC oscillator is commonly used [9]. To serve entire adiabatic system, a four-phase (phase difference is 90°) LC-based clocked power with low noise is proposed in [10]. All of above designs have lots of passive devices. For trapezoid clock, we found that analog integrator is a good choice due to its robust property. But the amplifier in the feedback loop has high power dissipation that goes against our goal of energy saving design. Without above methods restricted by the single signal input, multiphase clocked power using multi-pad can prevent passive devices integrating into chips. But growing it can largely increase the noise due to off-chip interface, and reduces bandwidth.

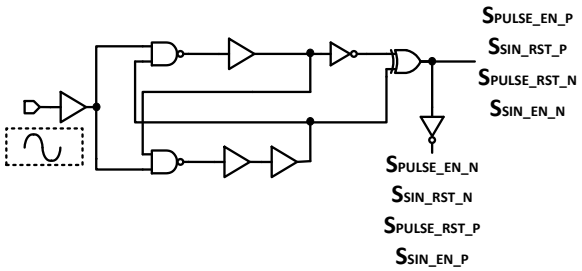


(a)



(b)

Figure 6 Four-phase source: a) Circuit diagram implemented in a parallel buffer chain; b) Simulation result.



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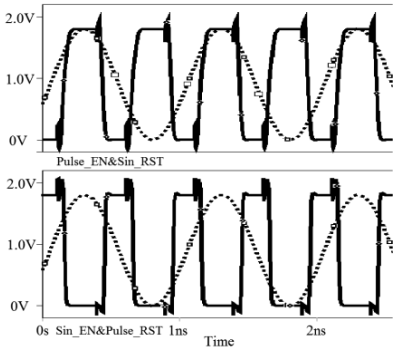

(b)

Figure 7 Switch controller: a) Circuit diagram based on the modification of non-overlapping clock; b) Simulation results.

We propose a mixed clock generator, which is driven by a single sinusoidal source, in both evaluate stage and recover

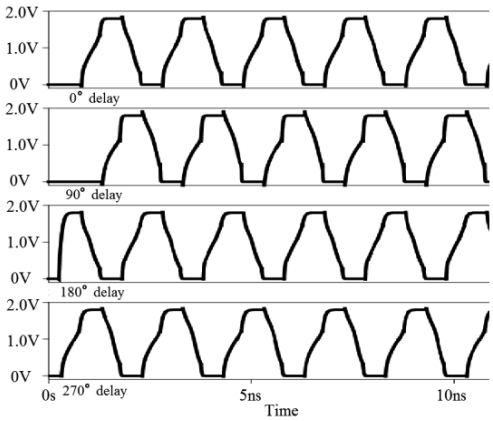

Figure 8 Simulation result of the proposed mixed clock under 500MHz sinusoidal input.

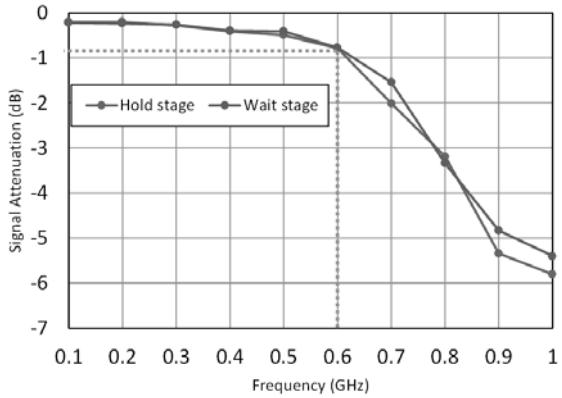

Figure 9 Signal attenuation versus frequency in hold stage and wait stage.

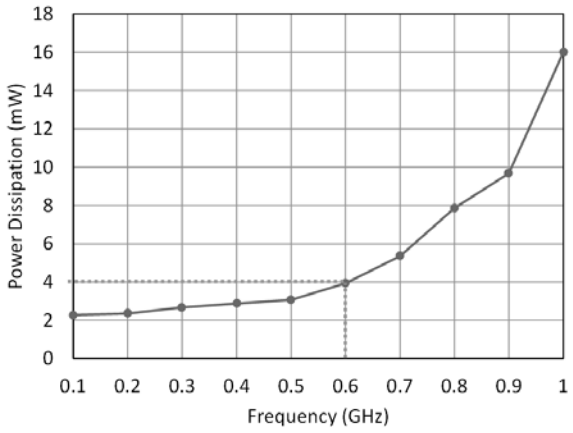

Figure 10 Predicted power dissipation versus frequency under 2pF load.

stage, the clock signal is achieved by trapezoid-like signal, while stable pulse signal is used in both wait stage and hold stage. Figure 4 shows the entire block diagram of the proposed design. It includes clock MUX, four-phases source, and a switch controller.

Figure 5 shows the circuit of clock MUX. It calibrates the approximate signals from four-phase source. In evaluate stage and recover stage, trapezoid-like signal is enabled to achieve

slow charge/discharge. In wait stage and hold stage, the input signal is buffered to supply stable low or high voltage. Under high frequency, charge injection will influence the clock accuracy. Dummy switch [12] is widely used in sample and hold circuit to release undesired charge to ground. Hence, two CMOS switches are added as dummy switches, mitigating the effect of charge injection.

Four-phase source can keep the following adiabatic logic working in correctly pipelined flow. To achieve four phase signals with an important prerequisite that without passive devices, we use parallel buffer chains as a delay circuit to roughly built a four-phase signal with 90° phase shift. Figure 6 shows the circuit of four-phase source and its simulation results under 1GHz sinusoidal input. One problem is that, since the transistor size is fixed, fall time and rise time in output under different frequencies cannot be adaptively adjusted to build four-phase signals with 90° phase shift. But the output in this block will be calibrated by clock MUX at the cost of the uneven time of four stages. This uneven would not cause incorrect logic transmission since timings of the beginning and end of one period are fixed by the clock MUX.

For switch controller, its main function is to control CMOS switches in the clock MUX. Based on our design, it is that when trapezoid-like signal is about to reach max/min peak value, the signal will be buffered. In the rest of rise and fall time, slow charging and discharging will be performed. We modified classical non-overlapping clock [13] to achieve two signals adaptively controlling CMOS switches in clock MUX. Figure 7 shows the design of switch controller and the simulation results under 1GHz sinusoidal input.

IV. Experimental Results

Figure 8 shows clock results of our final design when the frequency of input sinusoid is 500MHz. It can be seen that during both evaluate stage and recover stage, charging signal and discharging signal are trapezoid-like signals, and in hold stage and wait stage, clock is achieved by flat high or low voltage. Figure 9 is the test of signal attenuation during wait stage and hold stage. Figure 10 shows the results regarding predicted power dissipation of the proposed design under 2pF load. It is concluded that the best working frequency for our design is under 600MHz, considering both signal integrity and power dissipation.

In the experimental validations, we focus on the comparison between tank capacitor, oscillator, and our design in number of transistors and passive devices used: a) For tank capacitor with four steps, 876 transistors and 16 capacitors are used; b) For LC oscillator, 222 transistors, 2 inductors, and 4 capacitors are used; c) For our work, only 122 transistors without passive device are used. Note that to build four-phase source and enhance the ability of sampling in clock MUX, the size of some transistors is increased. In our design, 32 transistors of 25μm/0.2um, 34 transistors of 6μm/0.2um, 20 transistors of 4μm/0.2μm, and rest of transistors normally of 0.25μm/0.2μm are used. It can be concluded in the view of device cost, our design is the best choice comparing with tank capacitor and LC oscillator. Secondly speaking of suitable work frequency, LC oscillator can work in very high frequency (over 1GHz) with high reliability. Tank capacitor is suitable for low frequency application with extremely low power dissipation. Previous simulations indicated that our design can work well under 600MHz. Over this frequency, signal integrity of the proposed design will degrade rapidly.

V. Summary

We analyzed the essence of adiabatic logic. In depth, we analyzed three mainstream clocked power theoretically. Going to circuit level, it is the inspiration of removing passive devices, we proposed a low cost mixed clock generator used for adiabatic logic. Future work would focus on using an adiabatic system to verify the feasibility of our design.

ACKNOWLEDGMENT

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