SBPG: A Secure Better Portable Graphics Compression Architecture for High Speed Trusted Image Communication in the IoT

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***Abstract*—This paper proposes a hardware architecture for a Secure Digital Camera (SDC) integrated with Secure Better Portable Graphics (SBPG) compression algorithm. The proposed architecture is suitable for high performance imaging in the Internet of Things (IoT). The objectives of this paper are twofold. On the one hand, the proposed SBPG architecture offers double-layer protection: encryption and watermarking.On the other hand, the paper proposes SDC integrated with secure BPG compression for real time intelligent traffic surveillance (ITS). The experimental results prove that the new compression technique BPG outperforms JPEG in terms of compression quality and size of the compression file. As the visual quality of the watermarked and compressed images improves with larger values of PSNR, the results show that the proposed SBPG substantially increases the quality of the watermarked compressed images. To achieve a high performance architecture three techniques are considered: first, using the center portion of the image to insert the encrypted signature. Second, watermarking is done in the frequency domain using block-wise DCT size 8×8. Third, in BPG encoder, the proposed architecture uses inter and intra prediction to reduce the temporal and spatial redundancy.**

I. Introduction

The Secure Digital Camera (SDC) is a novel approach in capturing digital images. A simple Digital Camera (DC) is only able to capture digital images and maintain a visual record of events.The SDC on the other hand, with is unique components is capable of tracking the identity of the photographer, corroborate image veracity and maintain the chain of custody with detailed records in time, day, time, year and other significant information [1]. The rest of the paper is organized as follows: Section II describes the contributions of this paper, followed by section III which presents related studies. Section IV illustrates the SDC integrated with SBPG for IoT: A broad application perspective. Section V discusses the architectural overview of the SBPG integrated SDC. Secure Better Portable Graphics: algorithm and architecture are illustrated in section VI, followed by experimental results in section VII and conclusions in section VIII.

II. Novel Contribution of this Paper

The main objective of this paper is to describe a hardware architecture of a secure better portable graphics (SBPG) compression encoder that is integrated with an SDC. The proposed architecture meets modern technology requirements: high quality and smaller size because of using BPG compression. To the best of the authors' knowledge, this is the first ever proposed hardware architecture of SDC that is integrated with SBPG compression encoder. The novel contributions of this work include: (1) The first-ever architecture for hardware SBPG compression integrated with SDC, (2) the concept of SBPG that is integrated with SDC, which is suitable for real time intelligent traffic surveillance (ITS), (3) A Simulink® -based prototype of the algorithm implementation, and (4)an experimental analysis and comparison of the proposed architecture.

III. Related Prior Research

Mohanty in [1] demonstrated a unique approach of secure digital camera with a double-layer of protection, integral watermarking and encryption capabilities. The proposed architecture considers hiding binary images and their secure authentications. It also provides a method for field programmable gate array (FPGA) implementation. Darji *et al.* [2] show hardware capable of entrenching invisible watermark using LeGall 5/3 (Discrete Wavelet Transform) DWT. In [3], a novel scheme is introduced to support pictures and illustrations captured by digital cameras. Lastly, the study in [4] provided an innovative approach for putting into practice the two digital image-watermarking methods.

In the smart traffic surveillance domain, [5] considers the effectiveness of an embedded smart front-end camera for implementing complex algorithms. The essence of the research presented in [6] lies within the proposed Scale Adaptive Object Tracking (SAOT) algorithm used for real-time trailing of the traffic from a motionless camera.

In [7], authors offer a prototype for a new smart camera that can be used for smart surveillance of traffic. Wafi *et al.* [8] investigated camera-video-surveillance abilities that could be used for distinguishing moving vehicles in diverse and variable street settings. The study in [9] proposes an original approach in the form of a camera capable of transmitting and receiving ways in multitude of dimensions when used along with pan-tilt-zoom (PTZ).

IV. SDC Integrated with SBPG for IoT: A Broad Application Perspective

SDC is a device that has the standard features of a digital camera and built-in facility for real-time operation, low-cost

and power [10]. In this paper, we present a novel concept of a secure Better Portable Graphics (SBPG) with built-in watermarking and encryption facility. BPG compression has several advantages over JPEG including high quality with lower size than JPEG, which makes it suitable for real time and bandwidth requirements. The SDC is integrated with SBPG and typically designed as an SoC. Using a double-layer of protection, watermarking and encryption, the SDC addresses many DRM-related tasks including ownership rights, tracking usage, extent of tampering, and facilitating content authentication. Thus, SDC is arguably one of the best proven ways to facilitate real-time rights management, and is considered to be suitable for real time applications such as the IoT in highway surveillance systems, which is introduced in this paper as shown in Fig. 1.

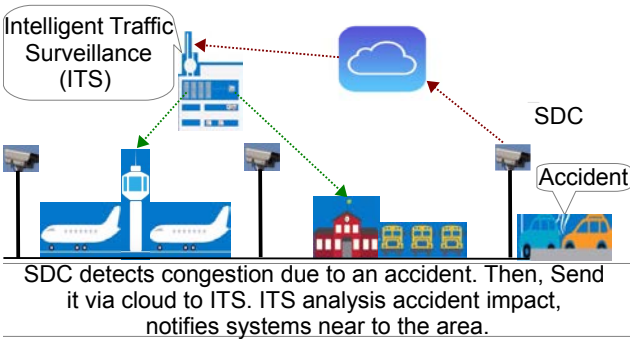

Fig. 1: Potential benefits of introducing the IoT in ITS system.

V. Architectural Overview of SBPG Integrated SDC

An Architectural overview of the proposed SBPG compression integrated SDC is shown in Fig. 2. The proposed architecture is a digital camera with built-in capabilities: watermarking and encryption. It consists of an active pixel sensor (APS) unit, analog-to-digital converter, liquid crystal display, encryption unit, watermarking unit, and compression unit.

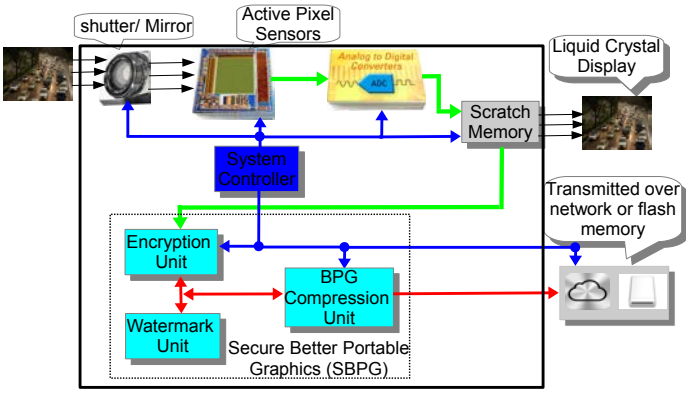

Fig. 2: System-level block diagram of SBPG integrated with SDC.

VI. Secure Better Portable Graphics: Algorithm and Architecture

A. Algorithm and Architecture of Encryption and Watermark Unit

The proposed encryption and watermarking unit in the context of SBPG operation flow is shown in Fig. 3.

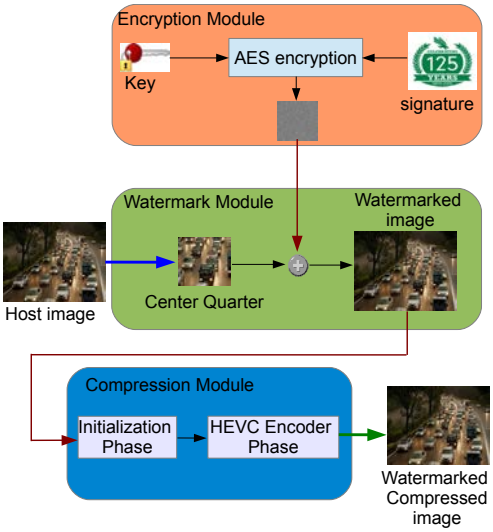

Fig. 3: Schematic overview of the proposed SBPG module.

The invisible-robust-blind watermarking algorithm is summarized as follows:

1) Optimization of robustness, quality, and computational load because of using the center portion of the image, which contains the main information about the image. Also, encryption and watermarking insertion at this center quarter increases robustness.
2) Watermarking is done in the frequency domain using the Discrete Cosine Transform (DCT) that will increase watermarking insertion speed.
3) The insertion of the watermark is done in the mid-frequency of the image block so that will increase the robustness since any removal of high or low frequency components of the watermarked image by operations does not significantly affect the watermark.

B. Algorithm and Architecture of BPG Compression Unit

Fig. 4 shows the BPG image encoder algorithm. Details of its design are given in Albalawi *et al.* [11].

The BPG compression encoder block diagram is presented in Fig. 5. It is divided into two phases: the pre-encoding (initialization) phase and HEVC encoding. The encoder does an initialization processes to read meta data, color space, bit depth, etc. In the second phase, HEVC uses an 8×8 block as the basic coding unit, and the Discrete Cosine Transform (DCT) or the Discrete Sine Transform (DST) as the transformation mechanism to the frequency domain. HEVC encoding is performed in three stages: prediction, reconstruction, and bitstream core.

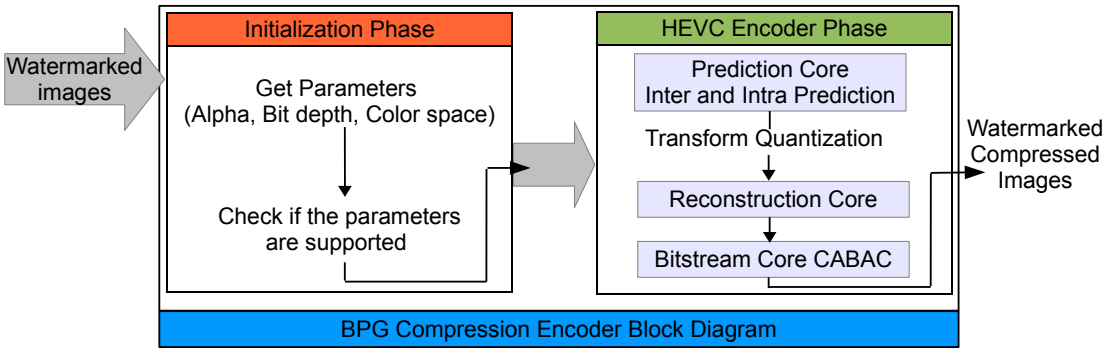

Fig. 5: BPG compression encoder block diagram.

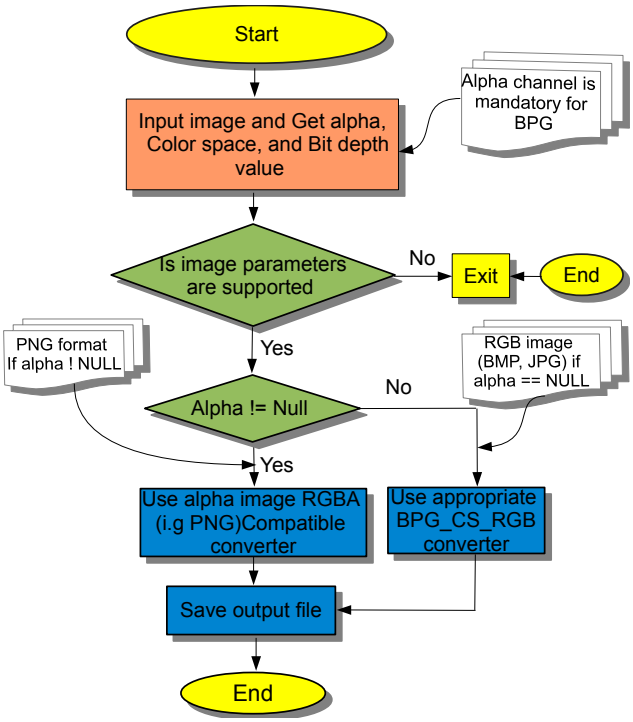

Fig. 4: BPG Encoder Algorithm.

The controller unit, as shown in Fig. 2, is responsible for controlling the entire sequence of processes and is modeled as finite state machine (FSM) with fifteen states.

VII. Experimental Results

The SBPG architecture is implemented in MATLAB® /Simulink® Version 8.3 (R2014a), with the computer vision System Toolbox Version 9.7 [12]. Implementing the algorithm in MATLAB® gives a better understanding of the low-level implementation while Simulink® model provides a top-level functional and dataflow visualization.

A. Insertion Watermarking and Compression Image using SBPG Encoder

Five standard images are selected randomly from a large set of images of the Joint Picture Expert Graphics (.jpg)

(a) Cover Image. (b) Watermarked Image (c) Watermarked Compressed Image

Fig. 6: Secure BPG Compression of PepperImage (512×512).

with different spatial and frequency characteristics. The cover image, watermarked image, and corresponding BPG image are shown in Fig. 6 for a sample image. The other images used in this work are not shown but the results of their BPG compression are included in the following discussion.

B. Graphs of RMSE and PSNR to and Quality Assurance

In order to measure the robustness and the strength of the watermarked images and the corresponding BPG images, two performance measure are considered: the Root Mean Square Error (RMSE) [13] and the Peak Signal-to-Noise Ratio (PSNR) [14].

Table I illustrates the related metrics for each watermarking and BPG compression technique and test image. It can be seen that the value for PSNR is maintained above 47.9 dB for all cases. As the visual quality of the watermarked and compressed images improves with larger values of PSNR, this result shows that the proposed SBPG maintains the quality of the watermarked images so that it is impossible for the human eye to detected the signature of any watermark in it. Higher value of PSNR also show how robust the algorithm is to different types of attack. In addition, it substantially increases the quality of the compressed images. The graphs of PSNR and RMSE versus size of the watermarked and watermarked compressed images for all tested images are shown in Fig. 7 and Fig. 8. From Table I, the PSNR value for the "Pepper" image is maximum at 55.4 dB, where for the "Forest" image it is minimum. The RMSE is reversed, as presented in Fig. 9 and Fig. 10.

TABLE I: Quality Metrics for the Watermarking and Compression Techniques and Test Image

Test Image	Code	Size (KB)	RMSE	PSNR
Cover Baboon Image (16.7KB)	Watermarked Image	20.0	0.76	50.4
	Watermarked Compressed Image	16.1	0.50	53.1
Cover Forset Image (25.1KB)	Watermarked Image	28.2	0.92	47.9
	Watermarked Compressed Image	24.0	0.60	51.3
Cover IceClimb Image (83.3KB)	Watermarked Image	48.0	0.58	52.7
	Watermarked Compressed Image	46.0	0.42	55.0
Cover Lena Image (32.0KB)	Watermarked Image	40.2	0.89	49.1
	Watermarked Compressed Image	38.8	0.85	51.9
Cover Pepper Image (39.3KB)	Watermarked Image	40.0	0.52	53.6
	Watermarked Compressed Image	39.0	0.41	55.4

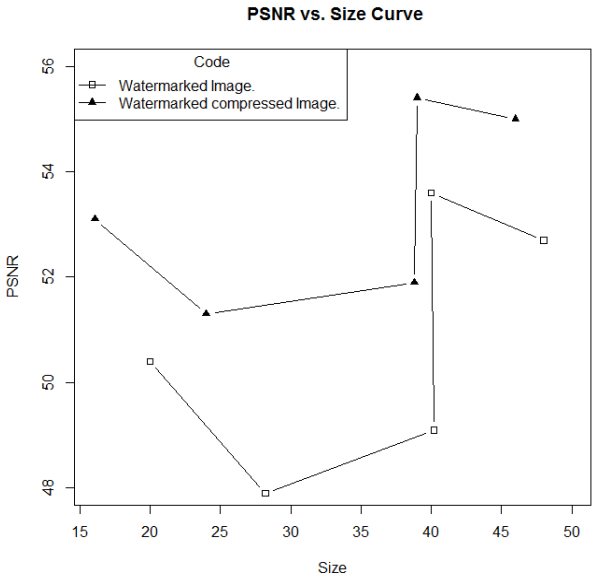

Fig. 7: PSNR vs Size Curve.

A comparative perspective of this architecture with respect to existing secure digital camera works is presented in Table II.

C. Testing for High performance

It is imperative to consider watermark and compression quality and performance trade-offs. From Table I, it can be argued that the proposed SBPG architecture gives high quality since the value of PSNR is maintained above 47.9 dB for all cases. To achieve a high performance architecture the following are considered:

1) Optimization of robustness, quality, and computational load because of considering just the center portion of the image, which contains the main information about the image. Thus, the speed is increased when the algorithm considers a portion of the image,

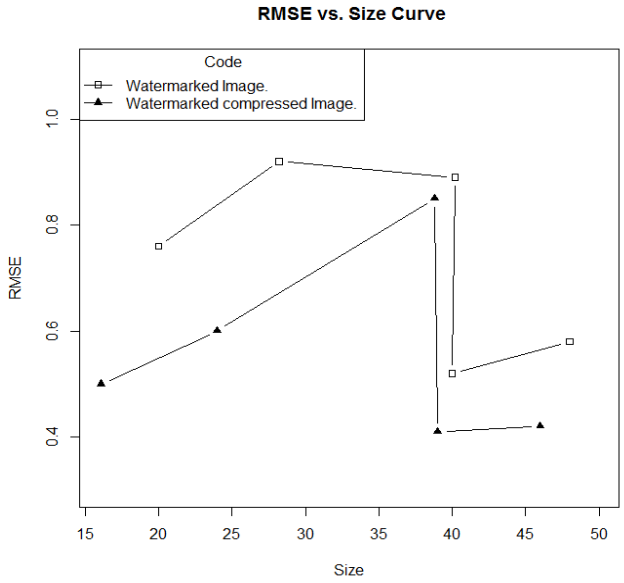

Fig. 8: RMSE vs Size Curve.

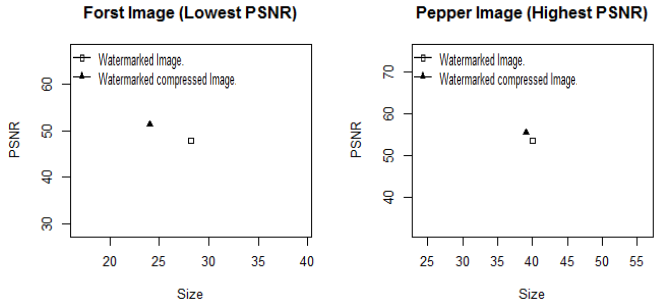

Fig. 9: Highest and Lowest value of PSNR.

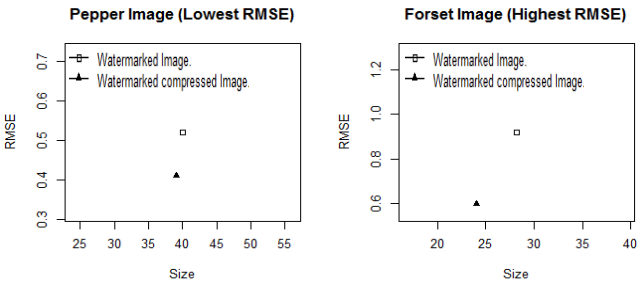

Fig. 10: Highest and Lowest value of RMSE.

TABLE II: Comparative Perspective with Existing Secure Digital Camera Architecture.

Prior Research	Built-in Security Function		Domain	Built-in	object
	Watermarking	Encryption		Compression	
Mohanty *et al.* [1]	Invisible Robust	AES	DCT	None	Image
Anand *et al.* [15]	Invisible Feasible	None	DWT	None	Image
Mohanty *et al.* [16]	Visible	None	DCT	JPEG Encoder	Image
Lei *et al.* [17]	Semi-Fragile and Robust	None	DWT	None	Image
Mohanty *et al.* [12]	Visible	None	DCT	MPEG-4 Compression	Video
This paper	Invisible Robust Blind	AES	DCT	BPG Encoder	Image

not the whole image. Also, the watermarking insertion at this center quarter increases the robustness because any attempt to remove the watermark will result in degradation of image quality.

2) Watermarking is done in the frequency domain using block-wise Discrete Cosine Transform (DCT) of size 8×8 that will increase watermarking insertion speed.
3) In the BPG encoder, the proposed architecture uses inter and intra prediction to reduce the temporal and spatial redundancy, which improves the computational speed.

To calculate the frame-rate, the Simulink® model is fed with 30 random images as inputs. The time taken to obtain the outputs (30 watermarked compressed images) is 1.27 s. Thus, the maximum throughput of the proposed SBPG is 25 frames/sec at a clock speed of 2400 MHz.

VIII. Conclusions And Future Directions of Research

In this paper, a hardware architecture to perform secure BPG compression encoder is presented as a built-in function in secure digital camera (SDC), which is used in image communications in the Internet of Things (IoT). The proposed architecture is prototyped in Simulink®. The experimental results prove that the new compression technique BPG outperforms JPEG in terms of compression quality and size of the compression file. As the visual quality of the watermarked and compressed images improves with the larger values of PSNR, the results show that the proposed SBPG maintains the quality of the watermarked compressed images.In the BPG encoder, the proposed architecture uses inter and intra prediction to reduce the temporal and spatial redundancy, which improves the computational speed. To the best of the authors' knowledge, this is the first ever proposed hardware architecture for SBPG compression integrated with SDC. Further work could include developing an energy-efficient architecture of SBPG as well as introduce the SBPG in medical image communication in the IoT.

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