Simscape based Ultra-Fast Design Exploration of Graphene-Nanoelectronic Systems

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***Abstract*—This paper presents non-EDA based design simulation using Simscape® for graphene based nanoelectronic systems. The objective of this paper is to explore ultra-fast design for analog devices using substitutes to conventional but time intensive EDA simulations such as SPICE. A GFET behavioral model is presented where the model is based on the drift-diffusion conduction mechanism of the dual-gate device. The kink region of the $I-V$ characteristic is modeled via a displacement current. A case study design circuit, an all graphene based low noise amplifier (LNA) is presented. The results show this to be a viable alternative approach to simulate GFET based circuits and systems in addition to existing SPICE, VHDL-AMS or Verilog-A based flows. To the best of the authors' knowledge, this is the first ever paper presenting a Simscape® model of a GFET device and also performing design exploration of GFET based RF circuits using Simscape®.**

***Index Terms*—Nanoelectronic System, Design Simulation, Simscape® Modeling, Graphene Field Effect Transistor, All-Graphene Low-Noise Amplifier**

I. Introduction and Motivation

Nanoelectronic devices are some of the most complicated structures produced by modern manufacturing technology. With transistor count already reaching billion in a die, it is becoming extremely challenging to shrink the transistor further down, particularly at 22 nm and below, in order to follow Moore's law. However relentless demand for smaller, cheaper and lower power consumption electronic products has forced designers to explore in depth two possible options: (1) combine analogue, radio frequency (RF) and digital components into a single chip, leading to analog mixed signal systems on chip (AMS-SoC) [1], [2] and (2) search for alternative technologies which can replace silicon to meet future demand. The former option necessitates a fusion of two design domains, namely analog and digital while the latter demands alternative material to silicon. AMS-SoC designs undergo a series of simulationa with SPICE in order to accurately simulate their behavior at layout level (with parasitics) [3]. However the major drawbacks associated with the SPICE simulation are the following: (1) heavy computational needs which prolongs the design time and increases the non-recurrent design cost of the chip, (2) the need of fab data or TCAD simulations which may not always be available for new or emerging technologies, and (3) design optimization support is very limited. In order to overcome these difficulties associated with SPICE based flows, this paper proposes a non-EDA design flow. This Simscape® based design flow offers two distinct advantages over conventional SPICE: (1) it can model emerging technologies without the need for fab data, (2) it provides fast and easy optimization at system level.

Motivated by the requirements to design smarter devices, researchers are actively opting for an alternative technology to conventional CMOS. Some of these technologies that are promising as an alternative to silicon FET are graphene FET, tunneling FET, BisFET, and spinFET [4]. This paper considers the graphene FET for design of nanoelectronic systems. A Simscape® [5] bahavioral model of a GFET based low-noise amplifier (LNA) is modeled. The LNA has significant applications in real-life circuits and systems. The model accuracy is verified with data available from MATLAB® [6], SPICE [7], VHDL-AMS [8] or Verilog-A [9] models presented in the existing literature.

The rest of this paper is organized in the following manner: Section II discusses the novel contributions of the current paper. Section III discusses background information on GFETs and GFET based circuits. Section IV presents the Simscape model that was developed as part of this work. Section V presents a GFET based RF circuit where an LNA design used as case study. Section VI presents our conclusions and directions for future research.

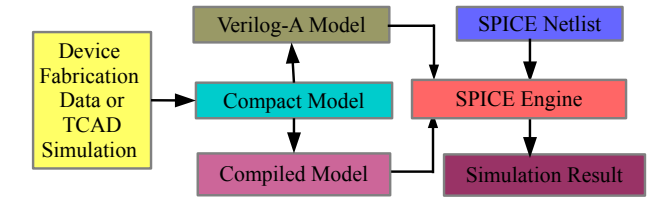
II. Novel Contributions of this Paper

The **novel contributions of this paper** to the state-of-art are the following:

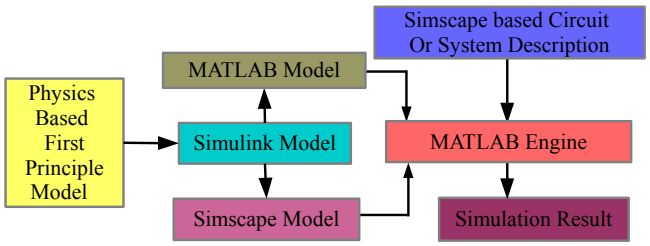
1) A Simscape® based ultra-fast design exploration which is a non-EDA flow and a paradigm shift.
2) Modeling of graphene FET devices using Simscape®.
3) Modeling of a GFET based LNA using the Simscape® graphical environment.
4) Experimental validation of the Simscape® device level models with existing VHDL-AMS or Verilog-A models.
5) Characterization of GFET based case study circuits and comparison with Verilog-A based designs.

Fig. 1 shows a comparative perspective of the proposed non-EDA based design flow with the well-accepted conventional EDA based flow. In the conventional flow, fab data or process information for a specific technology is needed,

which introduces delay in its implementation for emerging technologies. Fig. 1 shows the conventional EDA based design flow where the compact model is first derived from the fab data or technology computer-aided design (TCAD) simulation. The compact model is then converted into a compiled or Verilog-A model, which is used in SPICE. These are quite effort intensive tasks and may increase the design cost as well as slow the simulation process. For large circuits, the SPICE based EDA design flow has heavy computational requirements and does not have comprehensive design optimization options. However, the proposed Simscape® based non-EDA design flow does not require any fab data. Instead it relies on the first principle models published in the physics/semiconductor literatures. As shown in Fig. 1(b), the device level models presented in the MATLAB®, Simulink®, or Simscape® languages are simulated in the MATLAB® engine. The target circuit or system is designed using the Simscape® graphical based tool interface.



(a) SPICE based Design Simulation Flow



(b) Simscape based Design Simulation Flow

Fig. 1. SPICE versus Simscape® based Design Simulation Flow.

III. Graphene based Nanoelectronics

Due to thermal fluctuation caused by the heat generated in nanoelectronic circuits, silicon below 10 nm can not exist as a crystalline solid and it becomes amorphous. Thus due to continuous downsizing of the channel size in modern circuitry, silicon will soon reach its fundamental limitations and a suitable substitute needs to be investigated. Carbon falls in the same group with silicon in the periodic table (VI-A column) and due to its impressive allotrope, it is being treated as a suitable substitute for silicon.

In recent years, various forms of carbon structures have been studied such as three dimensional (diamond, graphite), two dimensional (graphene), one dimensional (nanotube) and zero dimensional (fullerones) [10]–[12]. Among those structures, nanotubes and graphene have been the dominant contenders to substitute silicon. The charge carrier mobility of of graphene is found to be above 200,000 cm^2/Vs at room temperature. Apart from this, graphene shares the same set of processing techniques as used for silicon. Due to these advantages graphene is considered in this paper.

A. Graphene FET: Structure

Several graphene transistor structures such as back-gated graphene transistor, dual-gate graphene transistor and epitaxial graphene from SiC and transistor structures have been studied in recent years. However in this paper, the dual-gate graphene transistor is used and Fig. 2 shows a cross-sectional view of such a GFET structure. A single layer of graphene is placed on top of a SiO_2 substrate, which is separated from the top gate by a thin layer of oxide. A back gate lies below the substrate which controls the resistance of a symmetric source-drain arrangement. By applying an electric field perpendicular to the graphene channel, a tunable bandgap can be opened which can be then modulated by the gate voltage. There have been three regions of operation identified for a bilayer GFET: triode region, unipolar saturation region and the ambipolar saturation region. The drain-source $I-V$ characteristics for the triode and the uniploar saturation region are equivalent to that of the MOSFET. However in the ambipolar saturation region, with increase in the drain voltage, there is an increase in the drain current. Such a behavior in the ambipolar region is referred as a second linear region. Ambipolar condition occurs when the electrons and holes have the same contribution to the total current whereas in other regions, either electron or hole dominates the total current.

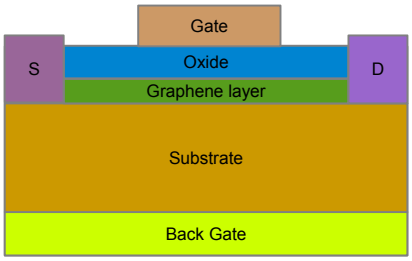


Fig. 2. Dual-gate graphene field effect transistor (GFET) cross-section. The graphene layer is indicated in green, below the oxide layer.

B. Graphene FET Based Circuits

Due to unique properties of graphene such as high carrier mobility and saturation velocity, high stability, low noise, graphene makes a good candidate for high frequency electronic applications. However there are some challenges associated with bulk graphene namely it is difficult to turn off the transistors, and the I_{on}/I_{off} ratio is low. These challenges makes them like unrealistic for digital circuits, since these applications need to save power during the off state. However this is not the case for analog and radio frequency (RF) applications. These applications always operate in the ON-state and also high carrier mobility (hence frequency) is the main requirement for these application over power saving. So, GFETs are well suited for these applications. Currently,

expensive group II-IV elements are used for high electron mobility transistors (HEMTs) for high carrier mobility and saturation velocities. So GFET can be a cost effective solution to these applications.

Furthermore, reports have suggested that using sophisticated technology, these GFETs can also be used for digital circuits. For example, dual-gate and bi-layer GFETs in [13] were measured to have an I_{on}/I_{off} ratio of 100. Thus reports have shown GFETs being used in all analog, digital as well as RF circuits such as inverters [14], [15] and [16], frequency multipliers [17], [18], and [19], an RF mixer [20], amplifiers [21], and [22], a photo detector [23], and low-noise amplifiers (LNAs) [24] and [25]. The concept of wafer scalable analog circuits was verified with an RF mixer example in [26]. In the current work, an LNA is chosen as case study circuit for GFET based circuit design utilizing the Simscape® graphene model.

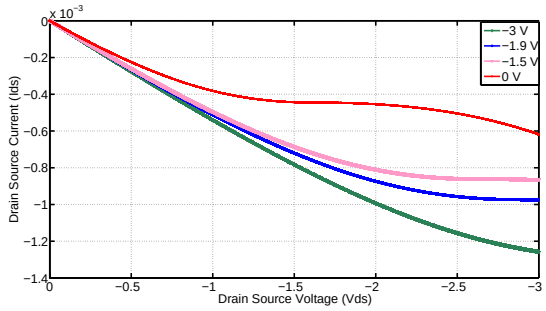
IV. Simscape® Modeling of Graphene FET

Simscape® is part of MATLAB® /Simulink® which is capable of multi-domain, multi-discipline modeling and simulation of physical systems. The Simscape® framework includes a variety physical component libraries. Essentially, there are two ways to build custom Simscape® models for emerging devices like the GFET: (i) a graphical method using fundamental Simulink® /Simscape® blocks, or (ii) textually with the Simscape® physical modeling language. Since the later approach offers better portability and is easier to maintain, the current paper adopts this approach. In addition, this approach makes hierarchical modeling and simulation of complex system easier as well. In order to compare the proposed Simscape® model with well accepted EDA model, the paper considers the GFET model based on the VHDL-AMS model from [8] and the Verilog-A model from [9]. The Simscape® simulation results show good agreement with the prior results presented in [6], [8], [27]–[29].

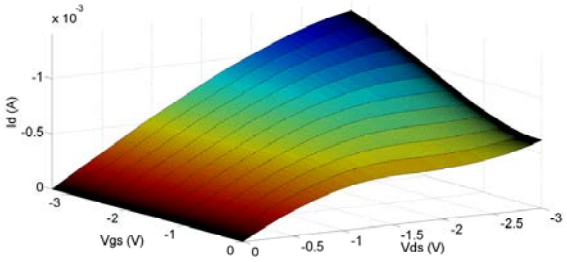
Fig. 3 and Fig. 4 show the GFET drain-to-source current-voltage characteristics. For a negative V_{bs}, the GFET source/drain region is P-type [6], [8], [27] and the mobility $\mu = 700$ cm^2/V/s, $R_s = 800\Omega$, and $E_c = 4.5$ kV/cm. In Fig. 3, top-gate voltages of 0 V, -1.5 V, -1.9 V and -3 V were used and V_{ds} is varied from 0 to -3 V. For positive V_{bs}, the source/drain region is n-type with $\mu = 1200$ cm^2/V/s, $R_s = 1500\ \Omega$, and $E_c = 15$ kV/cm. In Fig. 4, top-gate voltages of -0.8 V, -1.3 V, -1.8 V, -2.3 V, and -2.8 V were used and V_{ds} is varied from 0 to -3 V. The device parameters selected are based on published results [13]. The resultant $I-V$ characteristic curves are similar to the results obtained in VHDL-AMS [6], [8] and in Verilog-A models discussed in [9].

V. Graphene FET based Amplifier Circuit Design

As a specific demonstration of Simscape® based design simulation flow, an amplifier circuit simulation is presented in this Section. Design simulation of widely used circuits such as LC-VCO has been similarly performed, but has not been presented in this paper for brevity.

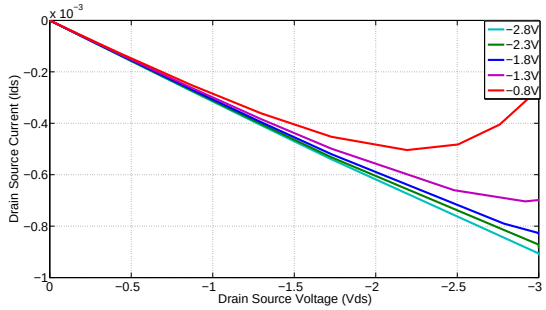


(a) I-V Characteristics

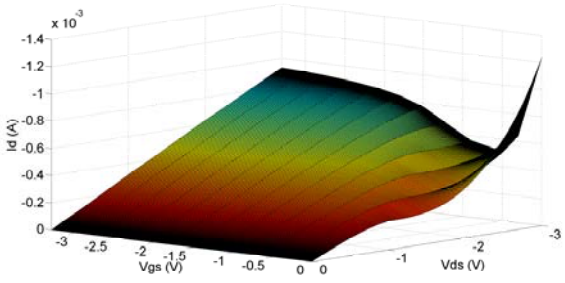


(b) Surface Plot

Fig. 3. $I-V$ characteristics for discrete and continuous values of V_{gs} for P-type GFET.



(a) I-V Characteristics



(b) Surface Plot

Fig. 4. $I-V$ characteristics for discrete and continuous values of V_{gs} for N-type GFET.

A. Theoretical Perspective

The Low-Noise Amplifier (LNA) is an electronic component which is used to amplify very weak signals in RF circuits. It is usually located very close to the detection device so as to reduce losses and is highly susceptible to electromagnetic, thermal and transmission noise. Since it can detect even a small change at the receiver, the LNA must have intrinsically low noise. The four important design parameters in LNA design are the following: (1) gain, (2) noise figure (NF), (3) non-linearity, and (4) impedance matching. Low NF results in better signal reception and in order to process signals effectively, high gain is necessary. If the LNA does not have high gain then the signal will be affected by the noise in the LNA circuit itself. However the general design trade-off is to minimize the noise of the circuit by accepting fairly low gain. The low gain is alleviated in subsequent stages of the receiver.

Fig. 5 shows the schematic diagram of a simple possible all-graphene LNA consisting of a common source amplifier and a load [25]. In the circuit, G_1 acts as a load and G_2 acts as a common source amplifier transistor. The circuit is amenable to exhaustive design exploration. This simple circuit is used as a test case to validate the Simscape® model developed for the current paper.

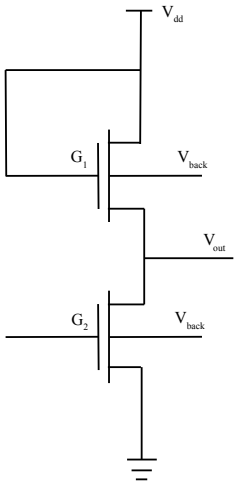


Fig. 5. Schematic of a GFET based LNA circuit. G_1 is the load transistor and G_2 is the amplifier.

The graphene nanoribbon widths W_1 and W_2 for devices G_1 and G_2 are chosen as the design variables. The gain (G), bandwidth (F_T) and power consumption (P_{LNA}) are considered as the figures-of-merit (FoMs) of the LNA.

B. Simscape® Modeling of the LNA

Fig. 6 shows the Simscape® experimental setup for LNA circuit characterization. In the LNA simulation, GFETs with $T_{ox} = 1$ nm, $H_{sub} = 2.85$ nm, and $L = 50$ nm were used. W was varied for both transistors for all simulations.

The result in Fig. 7 shows the inverse relationship between the band-gap and gain as demonstrated in [25]. Similarly, Fig. 8 shows how the bandwidth and the load resistance are related under constant gain G=15.75 dB. Finally, as shown in Fig. 9, the GFET based LNA is shown to have a small-signal bandwidth of 3.119 GHz. Table I summarizes the basic characteristics of the LNA for two different transistor sizes.

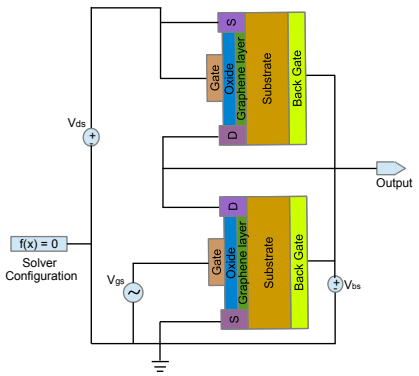


Fig. 6. Simscape® Experimental Setup for LNA Simulation.

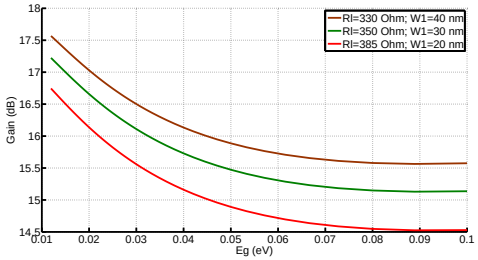


Fig. 7. Gain (G) vs. E_g at different R_L values.

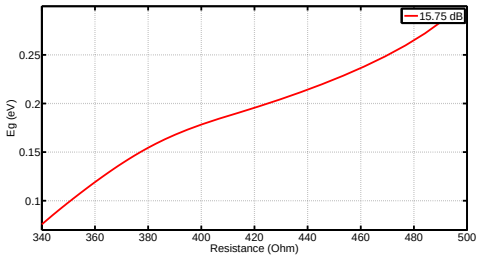


Fig. 8. E_g vs. R_L at constant G = 15.75 dB.

TABLE I
GFET BASED AMPLIFIER FIGURES-OF-MERIT

Parameters	Values	Values
W_1	20 nm	30 nm
W_2	10 nm	15 nm
Gain (G)	14.54 dB	15.41 dB
Bandwidth (f_T)	3.12 GHz	3.12 GHz
Power (P_{LNA})	23.8 mW	27.2 mW

VI. CONCLUSIONS AND FUTURE RESEARCH

A Simscape® based behavioral model of graphene FETs, suitable for design exploration at high levels of abstraction,

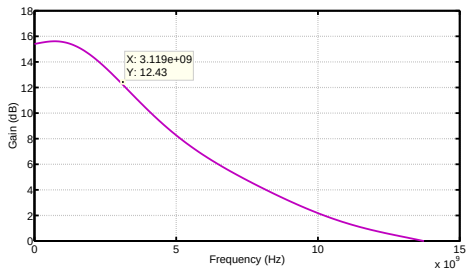


Fig. 9. The simulated frequency characteristics of the GFET based LNA.

has been presented in this paper. The model has been verified by extensive $I-V$ characterization of the GFET. A study circuit (LNA) is considered and the results are compared with the well-accepted EDA models. The results obtained in this paper show that the Simscape® based model can be used as a substitute for more detailed but time consuming EDA simulations such as SPICE with Verilog-A and VHDL-AMS models. Thus the ability to perform mixed high-level (behavioral) and transistor-level simulations for RF systems with an integrated design environment provides RF designers with unique design exploration and verification tools.

As a future research, additional functionalities for noise, transfer function and non-linear RF analyses such as periodic and quasi-periodic steady state can be incorporated within the Simscape® model. Optimization techniques using particle swarm-based optimization (PSO) algorithms such as artificial bee colony and ant colony optimization for GFET based circuits will be explored within MATLAB®/Simscape®.

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