

Ultra-Fast Variability-Aware Optimization of Mixed-Signal Designs using Bootstrapped Kriging

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Abstract—Analog/Mixed-Signal (AMS) circuits present significant challenges to designers with the increase of design complexity and aggressive technology scaling. Design optimization techniques that account for process variation while presenting an accurate and fast design flow which can perform design optimization in reasonable time are still lacking. As a trade-off of the accuracy and speed, this paper presents a process-variation aware design flow for ultra-fast variability-aware optimization of nano-CMOS based physical design of analog circuits. It combines Kriging bootstrapped Neural Network (KBNN) metamodels with a Particle Swarm Optimization (PSO) algorithm in the design optimization flow. The KBNN provides a trade-off between analog-quality accuracy and scalability and can be effectively used for large and complex AMS circuits while capturing correlations in process variations. The effectiveness of the design flow is demonstrated using a 180nm CMOS based PLL as a case study with 21 design parameters. The KBNN metamodel is 24× faster than NN metamodeling.

Index Terms—Nano-CMOS, Process variation, Mixed-Signal Circuit, Geostatistics, Kriging, Particle swarm optimization

I. INTRODUCTION

The design of Analog/Mixed signal (AMS) systems continues to present significant challenges, especially in design optimization. Metamodeling design techniques are used to aid the design process by reducing the design time while maintaining accuracy. There still is a need to improve the metamodels currently used to increase time efficiency and accuracy. Another issue is the effect of process variation. Metamodeling techniques can be improved to account for these effects early in the design process to ensure designs are process variation-aware. Particle Swarm Optimization (PSO) is one of many optimization techniques that have been explored to improve accuracy in deep nanometer regions [1], [2]. While PSO and Neural Network (NN) metamodels have demonstrated increased accuracy [3], certain design factors such as device parameter variations continue to pose a significant concern to circuit performance estimation.

In this paper we present a process aware design flow that is incorporated into different levels of the design process. It combines a Kriging bootstrapped NN (KBNN) metamodel with a PSO algorithm in the design optimization flow. The effectiveness of the design flow is shown using a PLL as a case study.

II. NOVEL CONTRIBUTIONS

This paper presents the following *novel contributions* to the state-of-the art of analog/mixed-signal CAD: 1) Fast and accurate physical design and optimization flow incorporating process awareness in analysis, characterization and optimization of performance measures. 2) Process-variations aware accurate and scalable metamodeling using Kriging bootstrapped Neural Networks. 3) Adaptation of Particle Swarm Optimization (PSO) algorithm for nano-CMOS based process-variation aware optimization. 4) A case study exploration using a 180 nm CMOS based PLL design. It may be noted that a generic overview of Kriging metamodeling is presented in [4]. Kriging metamodel for process variation analysis is presented in [5]. The current paper presents a natural progression of our research to ultra-fast physical design optimization of large analog blocks through the use of Kriging metamodeling.

III. RELATED RESEARCH

Polynomial regression methods which include response surface methodology (RSM) [6], [7], [8] are one of the most common and reliable methods explored. Non-polynomial based metamodels, particularly built from Neural Network (NN) training have also been reported to surpass polynomial regression techniques [9], [10], [11], [12]. NN techniques use a learning process to continuously train weights used in approximating these models. The weight training process is critical in the development of NN models and research in exploring techniques for optimizing this process is currently active. A technique popularly used is applying optimization algorithms to optimize the weight training of NN models [3]. Use of Kriging training for the NN architecture provides a trade-off between the accuracy of Kriging and scalability of the NN method [5]. In the current paper, we propose to infuse the characteristics of Kriging based techniques by bootstrapping the sample data points which are then used for the NN training process. We believe that the bootstrapped data points will enhance the modeling of process variation effects.

IV. PROCESS VARIATION AWARE ULTRA-FAST DESIGN OPTIMIZATION FLOW FOR MIXED-SIGNAL CIRCUITS

We propose a novel design flow that integrates a Kriging bootstrapped metamodeling process with the PSO algorithm

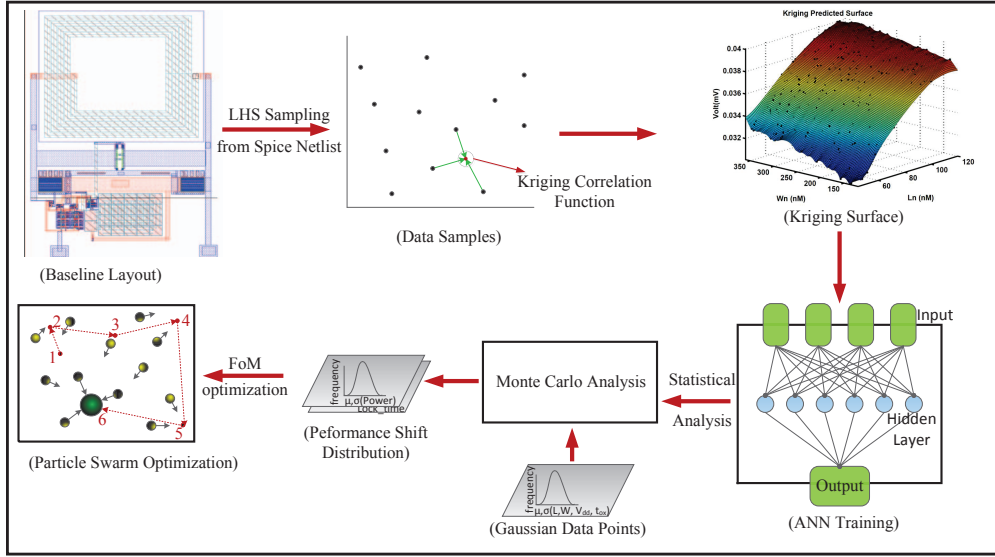


Fig. 1. Proposed high level design flow.

for the design optimization of nano-CMOS circuits as, depicted in Fig. 1. The key idea is to generate a Kriging surface using a small number of analog simulations with latin hypercube sampling (LHS) of the variables. An NN architecture is then trained to create a metamodel of the baseline circuits. Statistical analysis and optimization is performed over the metamodel instead of its SPICE netlist. The use of metamodels for design optimization iterations significantly speeds up the the design-optimization process and analog-level accuracy is maintained by the use of accurate metamodels which are generated from the parasitic-aware netlist.

The overall flow of the design process shown in Fig. 2 highlights the major phases of the design flow. The first phase labeled “A” consists of the baseline logical and physical design. In this phase, the baseline design is drawn both as a circuit schematic and the associated layout. The baseline is simulated for functional verification of the performance objectives. The functional verification also serves to characterize the circuit design objectives. The next phase involves the creation of the process variation aware metamodel of the circuit design. The first step in this phase is the identification and parameterization of the variables used to create the metamodel from the extracted parasitic netlist. Incorporating the process parameters early on in the design phase ensures a process variation aware metamodel. An LHS of the circuit from the parasitic netlist is then used by Kriging techniques to bootstrap the sample data points infusing process variation characteristics. We detail this process in Section V. The Kriging bootstrapped points are used for the NN Training. The final phase is the process aware design optimization. The optimization algorithm is used together with the created metamodel and design objectives as an input to optimize the design. The final design parameters are then used to update the physical design for an optimal design of the circuit. The process aware design optimization phase is discussed in detail in Section VI.

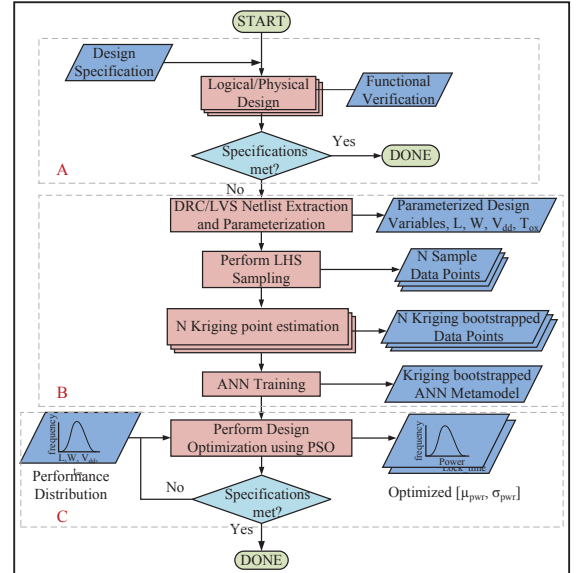


Fig. 2. Proposed design optimization flow.

V. PROCESS-VARIATION AWARE KRIGING BOOTSTRAPPED METAMODELING

Kriging has been successfully used for metamodel generation with high accuracy [7]. The property of Kriging which makes it very appealing and lends to its high accuracy is its ability to take into account the correlation between the input parameters in performance point prediction.

A disadvantage of Kriging is that it uses a set of matrix equations in calculating the unique weights for point predictions. For large circuits and high dimensional designs, the time cost can become expensive. The use of NN on the other hand can generate metamodels which are ultra-fast and robust in accuracy. The NN models however do not efficiently model

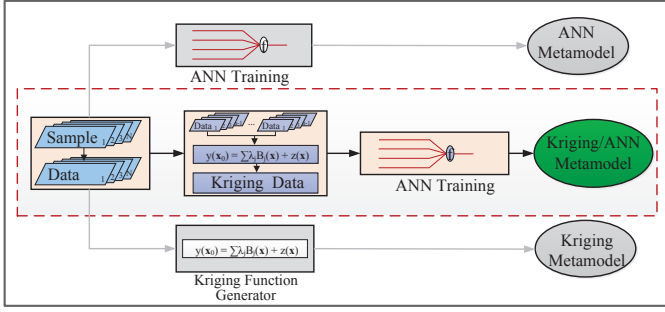


Fig. 3. Proposed Kriging based NN metamodel generation flow.

the effects of process variation. To ensure accuracy and time efficiency as well, we present a Kriging bootstrapped meta-modeling technique that combines the accuracy of Kriging with the speed of NN models, as shown in Fig. 3.

The metamodel generation process takes in sample data from the extracted parasitic netlist. The sample data points are fed into the Kriging metamodel generator for resampling of the data (bootstrapping). We generate N Kriging bootstrapped data points by using $N - 1$ points and the Kriging method to estimate the N th point. N iterations of this process will generate N Kriging bootstrapped data points which are then used for the NN training.

VI. PARTICLE SWARM OPTIMIZATION (PSO) ALGORITHM FOR PROCESS-VARIATION AWARE OPTIMIZATION

PSO is a type of evolutionary swarm intelligence algorithm for numerical optimization problems. Swarm intelligence algorithms are based on the exploitation of social or communal behavior of naturally or artificially occurring agents to collectively search for solutions. While heuristic in nature and based on social behaviors, swarm intelligence algorithms have proved to be very effective in optimization [13], [14], [15], and circuit design [16], [17].

The optimization problem implemented in this flow is to minimize the power consumption of the PLL circuit using the locking time as a design constraint. The process aware optimization of the circuit involves minimizing the mean μ and standard deviation σ of the optimal power consumption. As an example, optimization function can be expressed as:

$$\text{Minimize}[\mu_{pwr} + 3\sigma_{pwr}], \quad (1)$$

while subjected to locking time constraint. The PSO algorithm for the PLL is shown in Algorithm 1. Fig. 4 presents an illustration of the algorithm.

VII. EXPERIMENTAL RESULTS

The physical layout design of a PLL using a 180 nm CMOS technology were performed on the CADENCE Virtuoso platform, as shown in Fig. 5.

The PLL was characterized for power consumption, frequency output, locking time and jitter. The FoMs selected are Power (P_{PLL}), Frequency (F_{PLL}), Locking time (Lck_{PLL}), and Jitter (J_{PLL}). The design objective is the minimization

Algorithm 1: Particle Swarm Optimization of PLL over the Metamodels.

Input: Tuning parameter set X , Bootstrapped Kriging metamodels, Tuning parameter ranges.

Output: $X = (x_1, x_2, \dots, x_n)$ parameter set with optimized statistical performance;

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1 begin
2   SET:  $N$ , number of particles;
3   SET:  $Max_{iteration}$ , counter  $\leftarrow 0$ ;
4   SET: local best  $l_{x_i} \leftarrow$  current position;
5   SET: global best  $g_{x_i} \leftarrow$  current position;
6   Initialize: weight for swarm effect  $\varrho$ ;
7   Initialize: velocity for swarm effect  $w$ ;
8   while counter <  $Max_{iteration}$  do
9     foreach  $N$  do
10      Monte Carlo analysis over metamodels with
11      nominal  $x_i$ ;
12       $v_i = wv_i + \varrho_p\tau_p(l_{x_i} - x_i) + \varrho_g\tau_g(g_{x_i} - x_i)$ ;
13       $x_i \leftarrow x_i + v_i$ ;
14      if  $x_i < l_{x_i}$  then
15         $l_{x_i} \leftarrow x_i$ ;
16        if  $l_{x_i} < g_{x_i}$  then
17           $g_{x_i} \leftarrow l_{x_i}$ ;

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Result: Parameter set X with minimized μ, σ ;

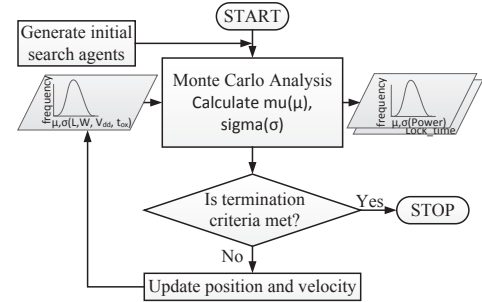


Fig. 4. Flow diagram for the PSO algorithm.

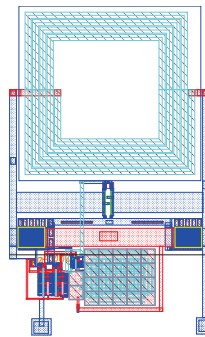


Fig. 5. Physical design of the 180 nm PLL.

of power consumption using the locking time as optimization cost and 21 parameters as design variables.

A total of 21 design parameters were used for the optimization simulation. Further statistical analysis was carried out using MATLAB. The results from the optimization simulation displayed in Table I show an improved statistical variation of

TABLE I
STATISTICAL OPTIMIZATION FOR KRIGING NEURAL NETWORK METAMODEL FOR PLL FOMs

		Kriging-ANN Metamodel				
		SPICE Netlist	Before Optimization		After Optimization	
			Value	Value	Error (%)	Value
Power (P_{PLL})	Mean (μ)	2.48 mW	2.40 mW	3.33	2.35 mW	2.08
	St. Dev. (σ)	0.42 mW	0.34 mW	19.05	0.39 mW	7.14
Frequency (F_{PLL})	Mean (μ)	2.66 GHz	2.51 GHz	5.64	2.78 GHz	4.51
	St. Dev. (σ)	10.95 MHz	41.93 MHz	282.92	16.92 MHz	54.52
Locking Time (Lck_{PLL})	Mean (μ)	5.51 μ s	5.11 μ s	7.26	5.21 μ s	5.44
	St. Dev. (σ)	0.72 μ s	0.44 μ s	38.88	0.42 μ s	41.67
Jitter (J_{PLL})	Mean (μ)	16.80 ns	14.69ns	10.25	17.72ns	5.47
	St. Dev. (σ)	1.32 ps	4.50 ps	240.91	0.33ps	75

the design simulation.

From the results it is observed that the standard deviation for P_{PLL} , Lck_{PLL} , and jitter (J_{PLL}) are all minimized with the frequency (F_{PLL}) having an increased deviation. The mean power consumption was also reduced while the other FoMs were increased. This is expected since the statistical optimization started off with the design parameters for optimal performance.

VIII. CONCLUSION AND FUTURE RESEARCH

This paper presented a statistical optimization design flow technique that incorporates into different levels of the design process statistical awareness through the combination of Kriging and Neural Network based metamodeling with a Particle Swarm Optimization (PSO) based algorithm. The design technique was illustrated through an 180 nm Phase Locked Loop circuit. Experimental simulation results show improved standard deviations of most of the Figures-of-Merits (FoMs) considered. This demonstrates promising results in increasing performance yield in the presence of strong and correlated process variation. The research will be expanded for design optimization of a variety of analog blocks in future.

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