Power Minimization of a Memristor-Based Wien Bridge Oscillator through a Simscape Framework

Prasun Ghosal
Indian Institute of Engineering Science and Technology, Shibpur, India
Email: p_ghosal@it.iiests.ac.in

Saraju P. Mohanty
University of North Texas, Denton, TX, USA
Email: saraju.mohanty@unt.edu

***Abstract*—Power consumption and thereby the power minimization strategies in differetn steps of design of nanoelectronic circuits is a raising concern today. Memristors with its inherent low power consumption have inspired the researchers to think in a different way. Proper modeling and intelligent use of memristors in hybrid mode with CMOS can show a bright direction for tomorrows design. This paper tried to shed the light on this issue by inspecting the problem with a specific case study of Wien-bridge oscillator circuit with different configurations of circuit replacement for heterogeneity and thereby to identify proper and judicious use of memristors for power optimization. Simulation results are quite encouraging to properly predict the appropriate configuration for power reduction.**

***Index Terms*—Memristor, Wien bridge oscillator, Power Minimization**

I. Introduction

Increasing power dissipation and thermal issues are becoming very important in todays and tomorrows nanoelectronic systems design. Bottleneck with CMOS technology scaling threshold and subsequent issues are inspiring researchers to find out some other technological alternative to mitigate the problem. CMOS technology is suffered by several issues like *(a)* parasitic effects *(b)* notable power dissipation *(c)* process variation effects etc today. Memristors have shown a new ray of hope from this perspective both for digital as well as analog nanoscale circuits for its features like *(a)* less power hunger *(b)* more computing capability *(c)* compatibility with neuromorphic computing etc.

A. Memristor: Fourth Fundamental Passive Element

In 2008, a new fabricated device, called *memristor* got its physical form in HP Labs [2], [3] though theoretically it was first reported in 1971 [1]. For exhibiting the properties of both memory as well as resistor, *memristor* name was given. Resistance of this device is affected by magnitude, direction, and duration of the applied voltage. It can remember its resistance value at the moment voltage is off when it is turned on again. It can find several important applications in nanoelectronic design [4] due to its pinched hysteresis and dynamic -ve resistance. It can directly relate magnetic flux and charge and so it is considered as fourth fundamental passive circuit element besides resistor, inductor, and capacitor (see Figure 1).

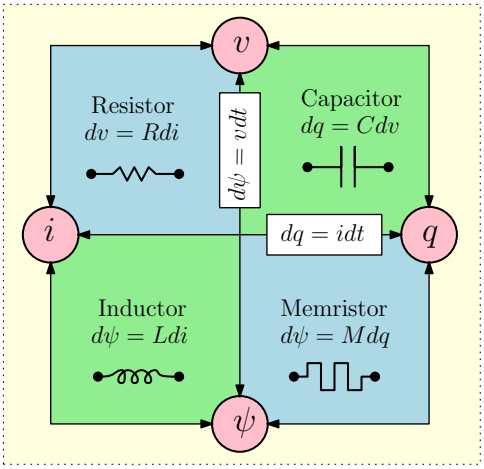

Fig. 1. Relationship between Basic Circuit Elements

B. Some Promising Contextual Role of Memristors

The reemergence of the non-volatile resistive memristor as a basic electric circuit element has boosted new ideas in multiple frontiers ranging from the recondite chaos theory to nanoscale technology products. This 'missing memristor' is expected to bring a technological raft in nonlinear dynamics of memimpedance circuitry, programmable boolean circuits, neuromorphic system design, transistorless multilevel nonvolatile digital memories, and so on [4]. In the memristor application field of study, prominent classification may be done by 1) design of nonvolatile memristor memory system; 2) digital and analog systems; and 3) neuromorphic systems. Taxonomy of various types of memristor applications is depicted in Fig. 2.

Rest of the paper is organized as follows. Novel contributions of the proposed work has been detailed in Section II. Section III provides some background information and motivation for this approach in concise manner. Section IV exhibits introduction to memristors and different existing modeling approaches. The proposed study of power minimization using memristors in Wien bridge oscillator circuit is presented in section V. Experimental results like power reduction factor determination and analysis of experimented models are also inscribed in the previous mentioned section. Lastly section VI concludes the paper by giving important extensions and

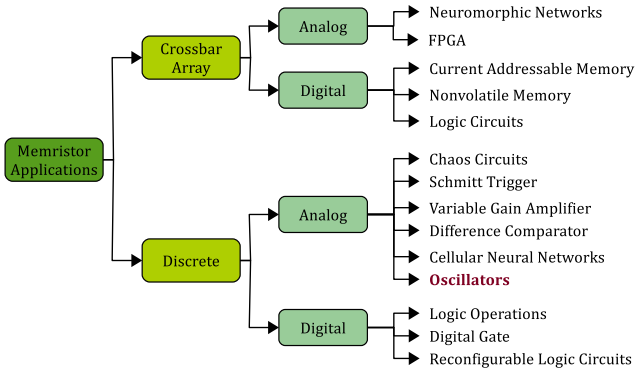

Fig. 2. Different Types of Memristor Applications

directions of our initiative.

II. Novel Contributions

The novel contributions of the proposed work may be summarized as follows.

- The work justifies its use in getting advantage in low power system design by using it in traditional analog circuits.
- Provides a case study by replacing resistors in Wien bridge oscillator with memristors in different configuration modes for proper analysis.
- Analysis of different power reduction factor in different configurations to identify a dynamic property for implementing memristors in analog circuits.

III. Related Research and Motivation

Now, high performance computing tends to support huge parallel processors and costs more power. Visualization of a 3D integrated circuit with low power and high performance may lead as a hypothetical concept with CMOS technology. Another thought have come of memristor [1] or hybrid architecture to make this possible. Memristor was first realized in HP lab, 2008 [3], giving a hope to further scale down nanoscale system designing and feasibility of neuromorphic computing. The first memristor was fabricated with TiO_2 and TiO_{2-x} sandwiched between two platinum (Pt) electrodes. Some approaches towards FPGA [5] [6] and 3D architecture [7] has already been initiated with memristor or hybrid CMOS technology. A CMOS/Memristor hybrid implementation is proposed in [8] in machine learning field. A thermal management scheme for 3D IC by enabling RRAM switching technology was presented in [9]. So, current challenge is going on to provide a neuromemristive solution for 3D architecture with CMOS Memristor coupled hierarchical structure. Neuromemristive networks have already giving inspiring result in emulating human brain, and our motivation is to apply it in a different direction, i.e 3D IC technology.

Neuromorphic computing [10] [11] validates the use of very-large-scale integration (VLSI) systems containing electronic analog circuits to mimic neuro-biological architectures present in the nervous system. In recent times the term neuromorphic has been used to describe analog, digital, and mixed-mode analog/digital VLSI and software systems that implement models of neural systems (for perception, motor control, or multisensory integration).

The thermal aware schemes in CMOS technology was experimented on various aspect of integrated circuits like [12], [13]. Temperature aware [14] and thermal driven [15] solutions are also well researched area for physical design steps for 3 dimensional integrated circuits. As power and thermal concern plays a important role in the integrated circuits, the CMOS-memristor hybrid architecture can provide low power solutions for that.

This paper has portrayed some important and interesting characteristics of memristor based simulation. Main concern of this paper is to manifest the 'less power hungry' property of memristors for analog circuits taking a case study with a simulation modeling tool. A detailed analysis on memristor and it's modeling in Simscape was presented in [16] and [17] respectively. This paper replicates the same Simscape model with deployment of different configurations in Simulink for Wien bridge oscillator circuits for studying the varied power minimization issues. Simscape is actually abstraction level of Simulink for electrical and magnetic field. Each experimental pace is described in the following sections.

IV. Power Minimization: Proposed Solution with Memristor

A. Introducing Memristors

Memristor(memory resistor), a 3nm technology, has a 'freezing property' of storing previous resistance and working as a non-volatile memory. Within a decade, memristor would help us to emulate human brain in a integrated circuits. Aiming at future trends of VLSI, my proposal is based on designing of such a post-CMOS architecture for 3D IC technology.

B. Memeristor Modeling Approaches

Memristor is fourth passive fundamental circuit element forming a non-linear relationship between electric charge and magnetic flux linkage. Memeristor have a non-linear voltage and current relationship that makes it a non-linear electrical model. Various memristor models are already simulated and published for academic purpose in MATLAB, Verlog-A/AMS, Spice, Simulink or Simscape. Known physical and electrical properties were used to create the model. An overview of different languages and a framework for memristor modelling are presented in Fig. 3.

V. Modeling and Simulation

A. Simscape/Simulink based Memristor Model

The mentioned Simscape/Simulink based memristor model was used from [18]. The simulation of memritor linear model in Simscape/Simulink is shown in Figure 4. Simulation procedure exhibits one fundamental property of pinched hysteresis loop for voltage-current plot, as shown in Figure 5.

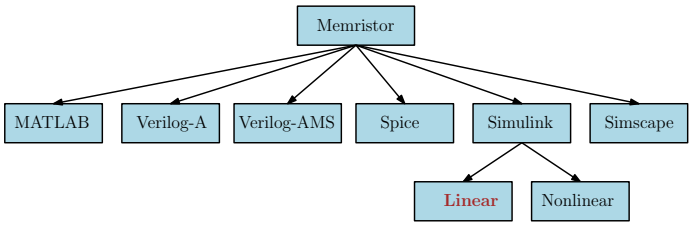

Fig. 3. Different Memristor Models

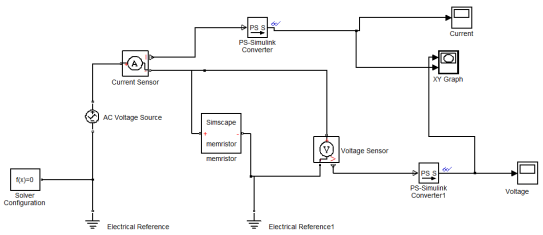

Fig. 4. The Configuration of Simscape/Simulink Memristor

B. Power Minimization in Wien-bridge Oscillator with Memristors

Here Wien bridge oscillator is used as a specific case study circuit. The schematic representation is shown in Fig. 6. A Wien bridge oscillator tank circuit consists of two capacitors and four resistors. Sustained oscillation (range 20 Hz - 20 KHz)is achieved by the instability occurred by combination of +ve and -ve feedback without any external source. The condition for sustained oscillation is presented in equation1 and frequency expression in equation 2.

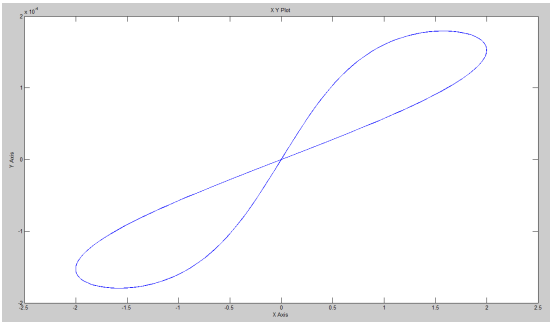

Fig. 5. Current vs. Voltage: Simscape/Simulink Simulation Result

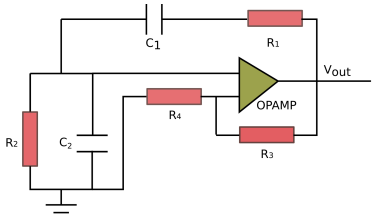

Fig. 6. Schematic of Wien Bridge Oscillator

$$\frac{C_2}{C_1} + \frac{R_1}{R_1} = \frac{R_3}{R_4} \tag{1}$$

$$f = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}} \tag{2}$$

The Simscape/Simulink simulation model of Wien bridge oscillator is shown in Fig. 7, exhibiting voltage oscillation property in Fig. 8.

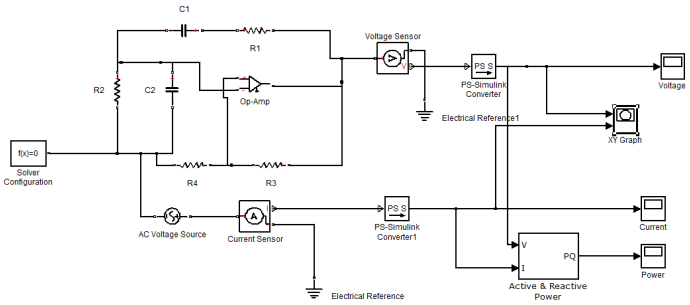

Fig. 7. Configuration of Simscape/Simulink Wien Bridge Oscillator Simulation

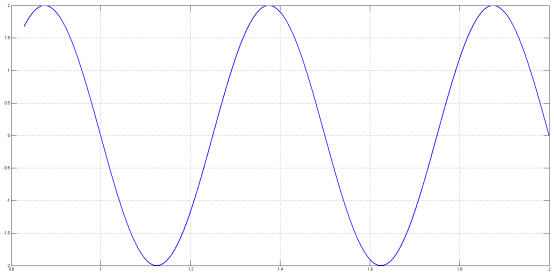

Fig. 8. Voltage Oscillating Property in Simscape/Simulink based Wien Bridge Oscillator Simulation

By controlling memristance during replacing resistors by memristors oscillation frequency can be changed to desired value (see equation 2). Five different configurations are studied (see Table I [18]).

In configuration 1, R_1 is replaced with memristor M_1 whose resistance is labeled as R_{m1}. In configuration 2, R_2 is replaced with memristor M_2 whose resistance is labeled as R_{m2}, and so on (as per Table I).

1) One Resistor Replaced with Memristor: When only one resistor (R_1/R_2) is replaced with memristor (M_1/M_2), then the required balancing property is according to equation 8. Here both configuration 1 and 2 are exhibiting this example. In configuration 1, R_3 needs to be changed to achieve sustained oscillation. So here, R_3 is designed to be $(R_4(1+\frac{R_{m1}}{R_2}))$. The Simscape / Simulink based simulation model of configuration 1 is presented in Figure 9. The power variation during the simulation procedure is depicted in Fig. 11 and Fig. 12.

Similarly, for configuration 2 (Fig. 10), R_2 was replaced a with memristor to achieve oscillation. R_3 is wired to be $R_4(1+\frac{R_1}{R_{m2}})$.

TABLE I
VARIATIONS OF WIEN OSCILLATORS

Configuration	Independent Modifications	Dependent Modifications
Configuration 1	$R_1 \Rightarrow M_1$	$R_3 \Rightarrow R_4(1+\frac{R_{m1}}{R_2})$
Configuration 2	$R_2 \Rightarrow M_2$	$R_3 \Rightarrow R_4(1+\frac{R_1}{R_{m2}})$
Configuration 3	$R_3 \Rightarrow M_3$, $R_4 \Rightarrow M_4$	$R_3 \Rightarrow 2R_{m4}$, $R_1 = R_2$
Configuration 4	$R_2 \Rightarrow M_2$, $R_4 \Rightarrow M_4$	$R_3 \Rightarrow R_{m2} + R_1$
Configuration 5	$Resistors \Rightarrow Memristors$	$R_3 \Rightarrow 2R_{m4}$, Given that $R_{m1} \Rightarrow R_{m2}$

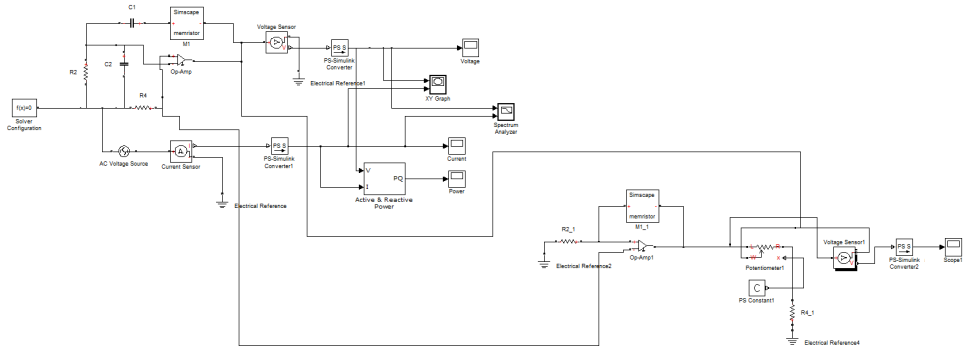

Fig. 9. Configuration 1: Simscape/Simulink Model Replacing one Resistor with Memristor

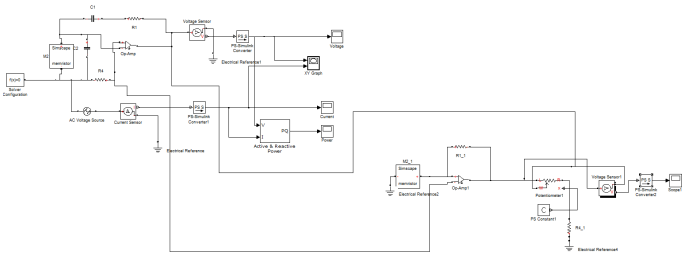

Fig. 10. Configuration 2: Simscape/Simulink Model Replacing one Resistor with Memristor

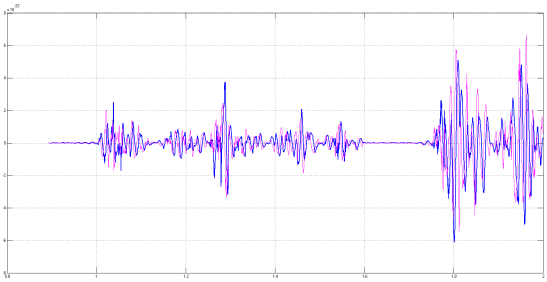

Fig. 12. Study of Power for Configuration 2

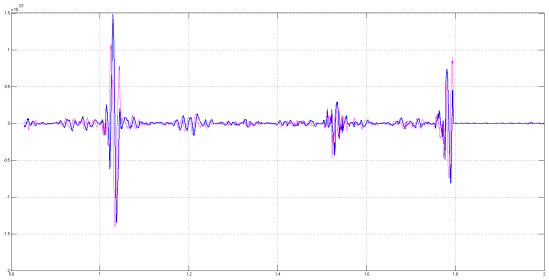

Fig. 11. Study of Power for Configuration 1

2) Two Resistors Replaced with Memristors: Two different configurations are studied with two resistors replacement. In configuration 3 (Figure 13), R_3 and R_4 are replaced with memristors. Again, to fulfil the condition of oscillation, different rating memristors were used. Given that $R_4 = R_{m4}$ and $R_1 = R_2$, R_3 is calculated to be $2 \times R_{m4}$. The power variation during the simulation procedure of configuration 3 and 4, is depicted in Figure 15 and Figure 16 respectively. In configuration 4 (Figure 14), R_2 and R_4 are replaced with memristors . Given that $R_{m2} = R_{m4}$, R_3 is replaced with memristor-resistor combination expressed as $R_{m2} + R_1$.

3) All Resistors Replaced with Memristors: Lastly, all four resistors are replaced with memristors in configuration 5 as shown in Fig. 17. To perceive the sustained oscillation condition R_3 was replaced with $2 \times R_{m4}$. Power variation of the simulated circuit is shown in Fig. 18.

4) Power Variation Analysis: The peak power variation, from all configurations, is shown in Table. II. The following comments are obvious from the table information.

- In configuration 5, where all resistors are replaced with memristors, the consumed power is lowest.
- Consumed power is greater in configuration 2 and 3 than

TABLE II
VARIATIONS OF POWER IN WIEN OSCILLATORS

Configuration	Maximum Linear Power(L_{pow}) [L_{pow} = $V_m \times I_m$]	Maximum Resulting Power (R_{pow}) [W]	Reduction Factor(R_f) [$R_f = \frac{R_{pow}}{L_{pow}}$]
Configuration 1	8×10^{-22}	8×10^{-24}	$\frac{1}{100} = 10^{-2}$
Configuration 2	3×10^{-18}	3×10^{-22}	$\frac{1}{10000} = 10^{-4}$
Configuration 3	3×10^{-21}	4×10^{-22}	$\frac{2}{15}$
Configuration 4	2.4×10^{-17}	1.5×10^{-19}	$\frac{1}{160}$
Configuration 5	2×10^{-24}	2×10^{-25}	$\frac{1}{10} = 10^{-1}$

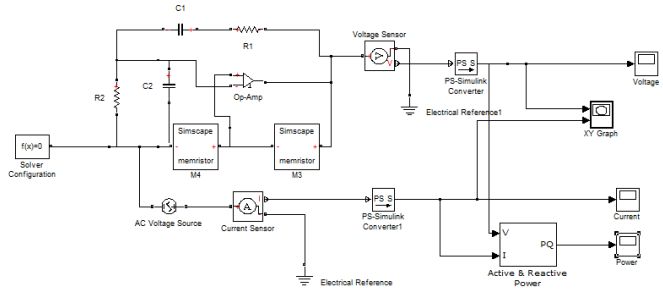

Fig. 13. Configuration 3: Simscape/Simulink Model Replacing two Resistors with Memristors

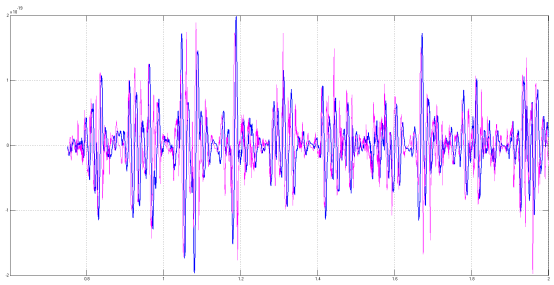

Fig. 16. Study of Power for Configuration 4

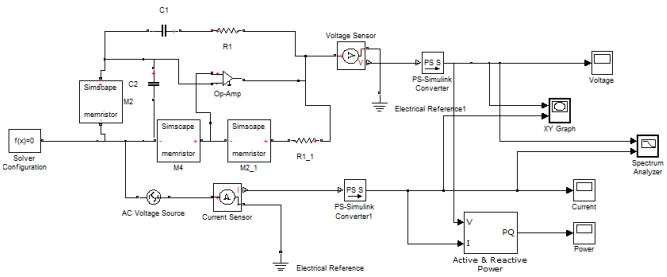

Fig. 14. Configuration 4: Simscape/Simulink Model Replacing two Resistors with Memristors

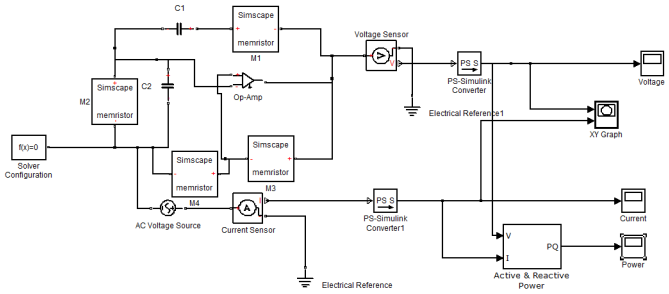

Fig. 17. Configuration 5: Simscape/Simulink Model Replacing all Resistor with Memristor

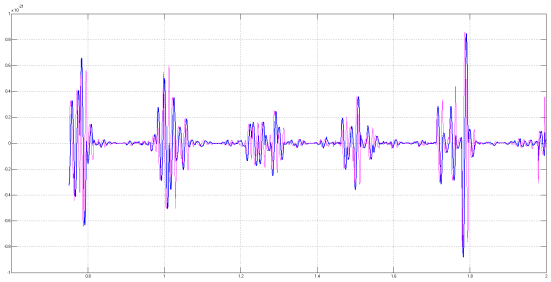

Fig. 15. Study of Power for Configuration 3

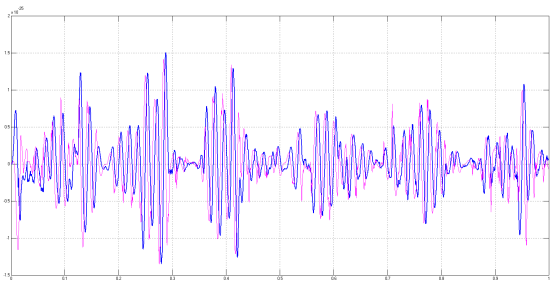

Fig. 18. Study of Power for Configuration 5

configuration 1, where more number of resistors are being replaced with memristors.

- In configuration 2, reduction of power is maximum than any other configuration.
- The power reduction is not dependent on number of resistors to be replaced, the configuration of the circuit has a great impact on it.

So, it's obvious that power reduction can be achieved for maximum cases by replacing resistors with memristors. On the other hand, it is also observed that, power reduction cannot be got only by replacing more and more resistors with memristor. Design and configuration of the circuit play an important role in this case.

Observation 1: Power reduction by replacing resistors with memristors does not solely dependent on number of resistors replaced. It also depends on the configuration of the designed circuit.

In Observation 1, an analogy between variable power reduction factor for different configuration is drawn. Lastly, the main aspect of studying memristor based Wien bridge oscillator is to buttress the concept of nominal power consumption property of memristors for ultra fast modeling and simulation of memristor-based analog circuits.

VI. Conclusion

The simscape/simulink based memristor model is minimizing the power in Wien-bridge oscillator by $\frac{2}{15}$ to $\frac{1}{10^4}$ factors. Simulation results clearly justify that power reduction by using memristors is feasible. Considering the importance of power consumption in the performance of a circuit it can help during the phase of modeling of nanoelectronic circuits to find the optimum configuration for that particular circuit. Future work may be extended to include non-linear models too to improve the accuracy of prediction during simulation.

References

[1] L. Chua, "Memristor-the missing circuit element," *IEEE Transactions on Circuit Theory*, vol. 18, pp. 507–519, Sep 1971.

[2] R. S. Williams, "How we found the missing memristor," *Spectrum, IEEE*, vol. 45, pp. 28–35, Dec 2008.

[3] D. B. S., G. S. S., D. R. S., and W. R. S., "The missing memristor found," *Nature*, vol. 453, pp. 80–83, 2008.

[4] S. P. Mohanty, *Nanoelectronic Mixed-Signal System Design*. McGraw-Hill Education, 2015.

[5] J. Cong and B. X., "mrfpga: A novel fpga architecture with memristor-based reconfiguration," in *2011 IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)*, pp. 1–8, June 2011.

[6] P.-E. Gaillardon, M. Ben-Jamaa, G. Beneventi, F. Clermidy, and L. Perniola, "Emerging memory technologies for reconfigurable routing in fpga architecture," in *17th IEEE International Conference on Electronics, Circuits, and Systems (ICECS), 2010*, pp. 62–65, 2010.

[7] K. T. Cheng and D. B. Strukov, "3d cmos-memristor hybrid circuits: Devices, integration, architecture, and applications," in *Proceedings of the 2012 ACM International Symposium on International Symposium on Physical Design*, ISPD '12, pp. 33–40, 2012.

[8] C. Merkel and D. Kudithipudi, "A current-mode cmos/memristor hybrid implementation of an extreme learning machine," in *Proceedings of the 24th Edition of the Great Lakes Symposium on VLSI*, GLSVLSI '14, pp. 241–242, ACM, 2014.

[9] C. Merkel and D. Kudithipudi, "Temperature sensing rram architecture for 3-d ics," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 22, pp. 878–887, April 2014.

[10] D. Monroe, "Neuromorphic computing gets ready for the (really) big time," *Commun. ACM*, vol. 57, pp. 13–15, June 2014.

[11] Z. W. S., A. G., D. V., F. A., B. J. P., and G. C., "Nanotube devices based crossbar architecture: toward neuromorphic computing," *Nanotechnology*, vol. 21, no. 17, p. 175202, 2010.

[12] P. Ghosal, H. Rahaman, and P. Dasgupta, "Minimizing thermal disparities during placement in 3d ics," in *Computational Science and Engineering (CSE), 2010 IEEE 13th International Conference on*, pp. 160–167, 2010.

[13] P. Ghosal, H. Rahaman, and P. Dasgupta, "Thermal Aware Placement in 3D ICs," in *Proceedings of 2nd International Conference on Advances in Recent Technologies in Communication and Computing (ARTCom 2010)*, pp. 66–70, 2010.

[14] T. Zhang, Y. Zhan, and S. S. Sapatnekar, "Temperature-aware routing in 3D ICs," in *Proceedings of the Asia-South Pacific Design Automation Conference*, pp. 309–314, 2006.

[15] T. Zhang, Y. Zhan, S. S. Sapatnekar, J. Cong, and Y. Zhang, "Thermal-driven multilevel routing for 3-D ICs," in *Proceedings of the Asia-South Pacific Design Automation Conference*, pp. 121–126, 2005.

[16] S. P. Mohanty, "Memristor: From basics to deployment," *IEEE Potentials*, vol. 32, no. 3, 2013.

[17] M. Gautam, "Exploring memristor based analog design in simscape," Master's thesis, University of North Texas, 2013.

[18] E. Agu, S. Mohanty, E. Kougianos, and M. Gautam, "Simscape design flow for memristor based programmable oscillators," in *Proceedings of the 24th Edition of the Great Lakes Symposium on VLSI*, GLSVLSI '14, pp. 223–224, 2014.