FuzzRoute: A Method For Thermally Efficient Congestion Free Global Routing in 3D ICs

Debashri Roy †, Prasun Ghosal †‡, Saraju P. Mohanty ‡
† Indian Institute of Engineering Science and Technology, Shibpur, Howrah 711103, WB, India
‡ University of North Texas, Denton, TX, USA
Email: debashri.roy.08@gmail.com, prasun@ieee.org, saraju.mohanty@unt.edu

***Abstract*—The high integration density interconnects, closer proximity of modules, and the routing phase are pivotal during the layout of 3D ICs. Heuristic based approaches are typically used to handle such NP complete problems of global routing in 3D ICs. To overcome the inherent limitations of deterministic approaches a novel methodology for multi-objective global routing based on fuzzy logic has been proposed in this paper. The guiding information generated after the placement phase is used during routing with the help of a Fuzzy Expert System to achieve thermal efficient and congestion free routing. A complete global routing solution is designed based on the proposed algorithms and the results are compared with selected fully-established global routers viz. Labyrinth, FastRoute3.0, NTHU-R, BoxRouter 2.0, and FGR. Experiments are performed over ISPD benchmarks. The proposed router called *FuzzRoute* achieves balanced superiority in terms of routability, runtime, and wirelength over others. The improvements on routing time for Labyrinth, BoxRouter 2.0, and FGR are 91.81%, 86.87%, and 32.16%, respectively. It may be noted that though FastRoute3.0 achieves fastest runtime, it fails to generate congestion free solutions for all benchmarks, which is overcome by the proposed FuzzRoute of the current paper. FuzzRoute also shows wirelength improvements of 17.35%, 2.88%, 2.44%, 2.83%, and 2.10% respectively over others.**

I. Introduction and Motivation

Layout design phase plays a pivotal role in chip design cycle in modern CMOS technology paradigm and is more complex in three dimensional integrated circuits (3D IC) than it's 2D counterpart due to closer proximity of modules. Global routing problem faces new challenges due to this. Recent works in global routing are aimed at different multi objective optimization techniques dealing with parameters for performance and congestion, thermal, proper insertion of thermal vias [1], sensitivity, minimization of wire length and number of critical paths, crosstalk [2] etc. But, all these approaches suffer from inherent limitations of deterministic approaches.

Fuzzy logic is a powerful soft computing technique that tries to find optimal solution using approximate reasoning unlike deterministic approaches. A pioneering work on this area [3] and later introduction of *fuzzy logic control* (FLC) [4] has boosted this area.

Increase in on chip power density with higher integration density induces localised thermal hot spots. Some earlier works reported in [5]–[10] dealing with thermal aware placement, and routing (2D and 3D) show the concern. 3D Steiner routing approach [11] suffers from very high complexity for multi nets. This encouraged us to search for lesser complexity solution in a non-deterministic way. Besides this another important metric, congestion ratio [defined later in section III], is also taken into consideration.

Rest of the paper is organized as follows. Novel contributions of this paper is summarized in section II. In Section III description of the problem is presented with the required preliminaries. Detailed and overall approach of the entire router (with pre-routing information generation, modified 3D placement, algorithm for fuzzy implementation, and details of main global routing approach with different types of nets) is described in Section IV. Implementation and experimentation details of the proposed fuzzified global router, comparisons with some full proved routers, and several characteristics are given in Section V. Section VI concludes the paper.

II. Contributions of this Paper

A novel multi-objective global routing technique has been proposed offering a thermal aware, congestion free routing solution for global routing of interconnects in 3D ICs. A powerful soft computing technique viz. fuzzy logic has been used to mitigate the effects of deterministic approaches that is able to route all the nets in a netlist. Novelty of this approach lies in many folds including providing the solution within a feasible time, but with a better degree of routability compared to other reported solutions in this category. Standard cell based design style is used for testing with benchmark circuits. However the proposed method can easily be extended to mixed cell design also. An efficient fuzzified expert system has been designed for thermal, and congestion aware global routing in routing space for fully 3D IC structure, as shown in Fig.1. An efficient controller is designed and used for decision making in a FLC by emulating *human like expert experience*. Present work on fuzzified global router generates the global routing path using subregion sequence for all nets. To the best of our knowledge, proposed fuzzified approach for global routing in 3D ICs is the first of it's kind.

Identification of a new metric called thermal sensitivity and it's measurement technique has been reported in one of our earlier work [12] and concept of fuzzification of routing was first reported in [13]. Present work is not only an advancement, but the design of a complete global routing solution for 3D ICs, where, other newly defined terms and metrics, new optimization algorithms, implementation and integration of the entire routing solution has been reported.

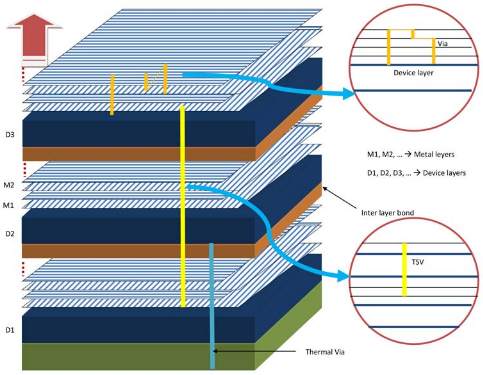


Fig. 1. Routing in 3D ICs.

TABLE I
DERIVED FUZZY SETS FROM LINGUISTIC VARIABLES.

Thermal Sensitivity Ratio	Weakly Sensitive(WS) Moderately Sensitive(MS) Highly Sensitive(HS)
Congestion Ratio	Weakly Congested(WC) Moderately Congested(MC) Highly Congested(HC)

III. PROBLEM DESCRIPTION

A. Definition of Linguistic Variables: Thermal Sensitivity and Congestion Ratio

In fuzzy logic concept each measurable metric used for optimization of the overall objective function in an optimization problem is called a linguistic variable. All these variables vary within [0,1]. Two different linguistic variables used here viz. thermal sensitivity information(s_r), and congestion ratio(o_r) may be defined in the following way.

Definition 1: Entire routing layer is represented by XY grid. Each module may occupy multiple X and Y blocks according to their dimension in a routing layer. Each grid is assigned to its own thermal sensitivity value originating from the power density value (as stated in [7], [8]) and thereby having a direct correlation with the temperature. The cumulative sum of thermal sensitivity values of consisting grid blocks in a localized area may generate a *hot spot* if it crosses a threshold value. A preferable routing region would be a region having less cumulative thermal sensitivity and less congestion. Congestion increases with the increase in number of pre routed nets that eventually increases the challenge during routing later nets. The subregions are selected units of entire routing space for execution of proposed routing algorithm. Routing eligibility is considered as inversely proportional to the thermal sensitivity and congestion ratio of each subregion.

1) Fuzzification: In premise part, the derived six fuzzy sets from two linguistic variables are shown in Table I.

2) Fuzzification of Ineligibility Factor: In the consequent part the linguistic variable is ineligibility criteria (μ_r). Here a number of fuzzy sets may be present. One rule base is used in this approach. For the rule base there are total 9 i.e. all possible fuzzy sets($i^{th} I$, where, $i = 1 \ldots 9$) for this particular linguistic variable, is used.

B. Grade of Membership Function

The membership functions for different fuzzy sets of both premise and consequent part are trapezoidal in nature because a moderately sensitive information with higher grade of membership value may also be considered as a highly sensitive information with a lesser grade of membership value. The nature of a membership function is shown in Fig. 2. The grade of membership values for 3 fuzzy sets(weakly, moderately and highly) corresponding to each linguistic variable of premise are as follows.

$$\begin{array}{lll} \mu_{ch} & =0 & \text{for x} < l_3 \\ & = 1 & \text{for x} \geq l_4 \\ & = (x - l_3)/(l_4 - l_3) & \text{for } l_3 < x < l_4 \end{array}$$

$$\begin{array}{lll} \mu_{cm} & = 0 & \text{for } x < l_1 \ \& \ x > l_4 \\ & = 1 & \text{for } l_2 \leq x \leq l_3 \\ & =(x - l_1)/(l_2 - l_1) & \text{for } l_1 < x < l_2 \\ & = (l_4 - x)/(l_4 - l_3) & \text{for } l_3 < x < l_4 \end{array}$$

$$\begin{array}{lll} \mu_{cw} & = 0 & \text{for } x > l_2 \\ & = 1 & \text{for } x \leq l_1 \\ & = (l_2 - x)/(l_2 - l_1) & \text{for } l_1 < x < l_2 \end{array}$$

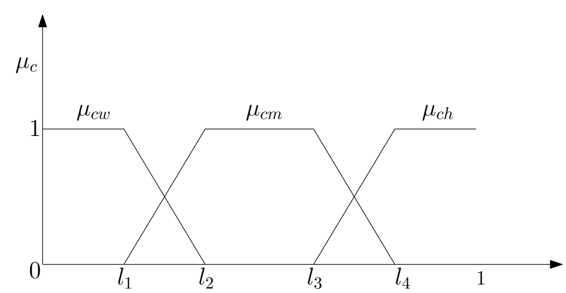


Fig. 2. The graph corresponding to the grade of membership values for thermal sensitivity, and congestion.

In consequent part the nature of membership functions for different fuzzy sets are same as above. Different boundary values l_1, l_2, l_3, l_4 (where $0 < l_1, l_2, l_3, l_4 < 1$) for the fuzzy sets of premise part will be generated in our algorithm. Similarly, for the consequent part the boundary values of different fuzzy sets will be determined according to the boundary values of corresponding fuzzy sets of the premise part mainly depending upon the rule base. the details are omitted due to paucity of space.

C. Problem Statement

Let $P = \{p_1, p_2, p_3, ..., p_k\}$ be a set of pins of k pin net distributed across L layers
$L =$ Number of layers available
Let $M = \{m_1, m_2, m_3, ..., m_r\}$ be a set of modules spread over the routing layer
where, (x_i, y_i) are the bottom left coordinates of module m_i.
Thermal Sensitivity (SI) of a module is in the range of 0 to 1.

Congestion ratio (CR) for each module is in the range of 0 to 1.

α, β are two cost factor coefficients, where $\alpha + \beta = 1$.

Weighted cost factor is generated from the thermal sensitivity and congestion ratio information incorporated with the α and β values.

Objective: *To build a fuzzified global router to determine the routing region with minimum wire-length for the total netlist depending upon the weighted cost function maintaining the two constraints viz. thermal sensitivity and congestion ratio for each net.*

IV. The Proposed Solution

A. Overall Block Diagram

Overall functional block diagram of the entire global router is shown in Fig. 4. It consists of three primary execution blocks viz. (i) Guiding Information Generating Block, (ii) 3D Placement Block, and finally (iii) 3D Routing Block. Detailed functions are discussed in following sections.

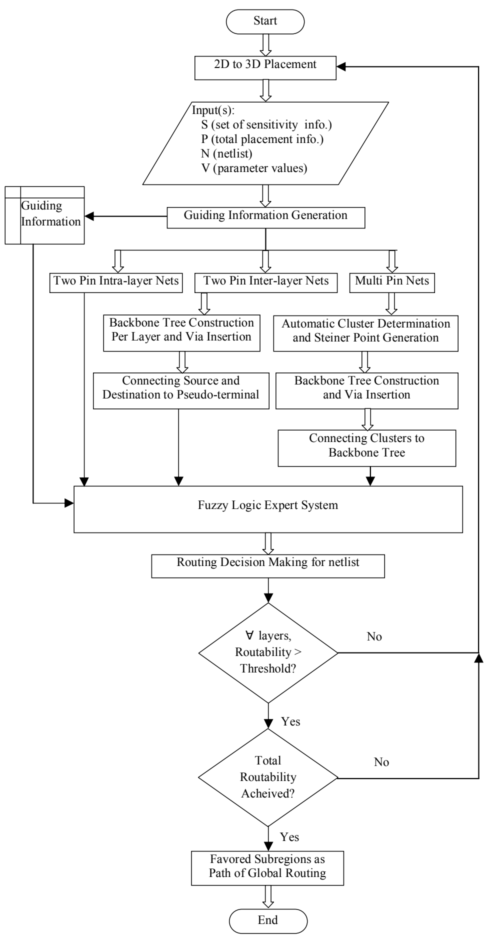


Fig. 3. Overall flow of the proposed fuzzified Global Router for 3D ICs.

B. Modified 3D Placement Technique

Due to unavailability of proper 3D IC benchmarks concepts of thermal aware 3D placement from [7], [8] is used. A modified heuristic has been developed to get 100 % overlap eliminated placement in 3D ICs (see Algorithm 1).

Modified_3D_Placement( )

Input : N= Number of cells to be placed,
L= Number of layers available,
A_r= Aspect ratio of the chip,
S_t= sub-matrix order,
I_t= Maximum iteration limit
Output: Thermally optimized 3D placement

```
begin
    Generate_3D();  /* Generate 3D matrix of minimum dimension satisfying constraints */
    Allocate_3D();  /* Allocate cells with corresponding power density values */
    while optimization_possible = yes do
        for layer_number = 1 to L do
            Layer_therm_opt();  /* Layer wise thermal optimization */
        end
        Inter_layer_therm_opt();  /* Thermal optimization across all the layers */
        if optimized = no then
            find_layers();  /* Determine the layers where 2D optimization is necessary */
        else
            stretch_layers();  /* Stretching routing regions in each layers to eliminate overlapping in cells */
        end
    end
end
```

Algorithm 1: Generation of full 3D placed circuits from standard benchmark circuits.

C. Pre-routing Information Generation

1) Overall Scheme: Overall flow of the proposed fuzzified global routing tool for 3D ICs may be represented as in the flowchart in Fig. 3.

From flowchart, it is clear that the total achieved routability is compared with a predefined threshold value (set by user) after decision making of all the nets for a particular circuit. If routability is greater than threshold, decision is taken and critical nets are passed for manual routing. When lesser, *rip-up* and *re-route* procedure is adopted.

2) Proposed Rule Base: The proposed rule base of fuzzy expert system consists of 9 rules with 9 fuzzy sets corresponding to a linguistic variable of consequent part and 6 fuzzy sets corresponding to two linguistic variables of premise part. The rule base considers all possible rules with all fuzzy sets of premise part. The proposed rule base is stated in Table II.

3) Proposed Fuzzy Expert System: Fuzzy_Expert_System( ) procedure constructs different fuzzy expert systems for different layers with same proposed rule base but different membership functions. This procedure is called from *Generate_Routing_Path()* during processing of generated guiding information.

D. Proposed Fuzzified Approach for Global Routing

The procedure *Generate_Routing_Path( )* generates the total routing path for all nets in terms of sub regions in the second part of the algorithm. It takes the output of modified 2D to 3D placer tool for a circuit as input and produces routing path as output for the netlist of the same circuit.

1) Two-pin Intra-layer Net Routing: The procedure *Generate_Routing_Path( )* first recognises all two-pin intra-layer nets and perform global routing in normal fuzzified way [13]. The *Intra_Layer_Routing( )* procedure generates the favoured subregions for connection between two pins and a boolean

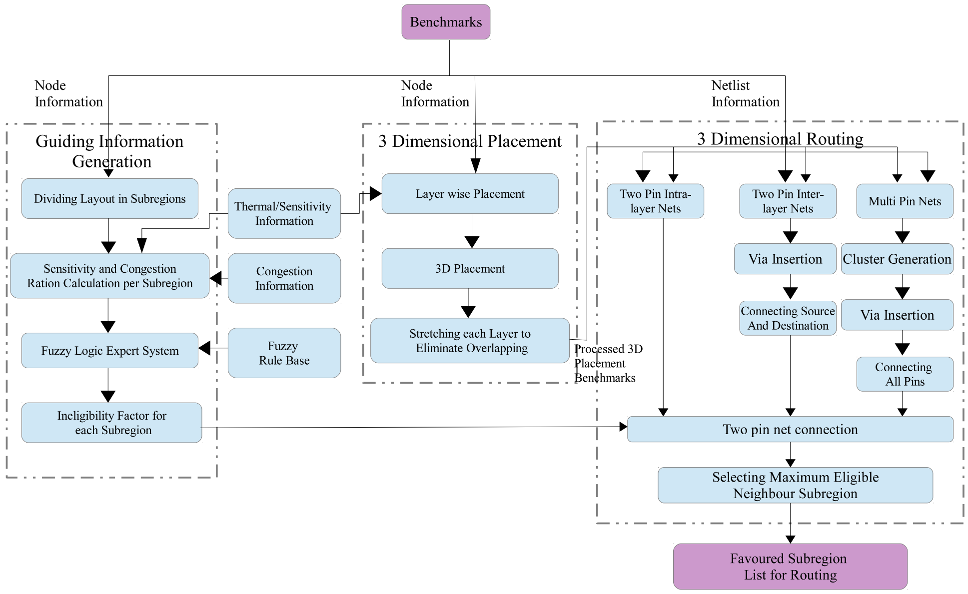


Fig. 4. The Proposed Thermally Efficient Congestion Free Global Routing Approach for 3D ICs.

Generate_Routing_Path( )

Input : SI = Set of thermal sensitivity information for each module,
$PInfo$ = The total placement information,
$NList$ = Netlist,
$ParamInfo$ = Parameter values
Output: Routing path in terms of favoured subregions

begin
  L = No_of_Layers($PInfo$);
  for $layer\_number$ = *1 to L* **do**
    Generate_Guiding_Info(SI, $PInfo$, $ParamInfo$); /* Guiding information generation for all layers */
    Fuzzy_Expert_System(); /* Build distinct fuzzy expert systems for all layers */
  end
  for $net \in NList$ **do**
    if $intra\_layer\_two\_pin\_net$ **then**
      Intra_Layer_Routing(); /* Generate routing path from source to destination */
    else if $inter\_layer\_two\_pin\_net$ **then**
      Backbone_Tree(); /* Determine pseudo terminal positions by constructing backbone tree */
      Pseudo_Terminal_Insertion(); /* Insertion of pseudo terminals and via */
      Connect_All_Pins(); /* Connecting source and destination pins to the pseudo terminal points */
    else
      /* For multi-pin intra and inter layer nets */

      Automatic_Cluster_Generation(); /*Generate Automatic number of clusters with multiple pins for all layers */
      Backbone_Tree(); /* Determine pseudo terminal positions by constructing backbone tree */
      Pseudo_Terminal_Insertion(); /* Insertion of pseudo terminals and via */
      Connect_All_Pins(); /* Connecting all pins of a net to the pseudo terminal points */
    end
  end
end

Algorithm 2: Generation of routing path for a netlist

TABLE II
THE PROPOSED ORIGINAL RULE BASE FOR INTER-LAYER NET ROUTING.

1.	If s_r is WS and o_r is WC then μ_r is $1^{st}I$
2.	If s_r is WS and o_r is MC then μ_r is $2^{nd}I$
3.	If s_r is WS and o_r is HC then μ_r is $3^{rd}I$
4.	If s_r is MS and o_r is WC then μ_r is $4^{th}I$
5.	If s_r is MS and o_r is MC then μ_r is $5^{th}I$
6.	If s_r is MS and o_r is HC then μ_r is $6^{th}I$
7.	If s_r is HS and o_r is WC then μ_r is $7^{th}I$
8.	If s_r is HS and o_r is MC then μ_r is $8^{th}I$
9.	If s_r is HS and o_r is HC then μ_r is $9^{th}I$

value that tells whether the destination is reachable or not. Decision making is done using the generated fuzzy expert systems depending upon different layers.

2) Two-pin Inter-layer Net Routing: Routing of two-pin inter-layer nets are done by via insertion and pseudo-terminal insertion followed by a backbone tree construction. Eventually the actual routing is performed by connecting the pseudo-terminals with source and destination by *Intra_Layer_Routing( )* procedure.

3) Multi-pin Net Routing: Next, All the multi-pin nets are recognised. For better degree of reliability the automatic number of fuzzy cluster determination technique using Simulated Annealing proposed in [14], is being used here with customization. An intelligent technique is used for Backbone Tree generation and determination of Pseudo Terminals for inter-layer connection. Finally clusters are connected to the Backbone Tree.

E. Time Complexity

If l is the total number of layers, m is the number of subregions in x direction and n is the number of subregions in y direction of the layout then time complexity for generating the guiding information is $O(l \times m \times n)$. The total global routing procedure for connecting two-pin, multi-pin, and critical nets requires this time in addition with the time required to process fuzzy expert system for each layer.

V. Experimental Results

A. Implementation and Results

The proposed algorithms have been implemented in C, Java and MATLAB 7.14.0, MCR, and MATLAB Builder JA. The GUI is designed in GUIDE and the fuzzy expert system is implemented using MATLAB fuzzy toolbox. The experiments were performed on a standard desktop environment of 4GB memory with an Intel chip running at 2.30 GHz. ISPD'98 (IBM-PLACE 2.0) benchmark suites (for Fixed-die Placement) were used in the experiments [15] .

Fig. 5 shows a snapshot of the implemented fuzzy expert system using fuzzy toolbox in MATLAB. From snap shots of Fig. 6 it is clear that using rule base the expert system is producing quite accurate output as changing of ineligibility factor is quite smooth here. The α, and β values can actually be user specified, though we have taken α=0.6, and β=0.4 in presented experimental results.

Experimental results for different IBM benchmarks are reported in Table III and variations of guiding information generation time as well as routing time are plotted in Fig. 8. Variation of routing time with different layer number for a fixed benchmark suite (IBM 10) has been studied [see table IV] and plotted in Fig. 7. Results show routing time is significantly less. Moreover, it is even decreasing with increase in device layers for more availability of routing space in 3D ICs. Some important observations from different plots may be noted in following Observations 1, and 2.

Observation 1: Better routing time may be achieved with more number of layers in 3D ICs.

Observation 2: Rate of increase in routing time is much less than the rate of increase in guiding information generation time with increasing numbers of nets.

B. Comparison for ISPD benchmarks

Table V shows performance of FuzzRoute for ISPD '98 benchmarks. Comparisons are made with selected widely used global routers viz. Labyrinth [16], FastRoute 3.0 [17], NTHU-R [18], BoxRouter 2.0 [19], and FGR [20].

First, the result shows that FuzzRoute is able to route through all the benchmarks. Second, it achieves good runtime. It can finish routing all benchmarks within reasonable time on our platform. The improvements on routing time over Labyrinth, FastRoute3.0, NTHU-R, BoxRouter 2.0, FGR are 91.81%, -10.29%, -34.91%, 86.87%, and 32.16% respectively. Though among all quoted global routers FastRoute3.0 achieves fastest runtime, it fails to generate congestion free solutions for all benchmarks e.g. ibm01, ibm04, and ibm09. Whereas, FuzzRoute can achieve 100% congestion free routability for all the circuits in much lesser time than other specified routers. Third, in terms of total wirelength FuzzRoute is not only comparable to others but it is much better with improvements of 17.35%, 2.88%, 2.44%, 2.83%, and 2.10% over Labyrinth, FastRoute3.0, NTHU-R, BoxRouter 2.0, FGR respectively.

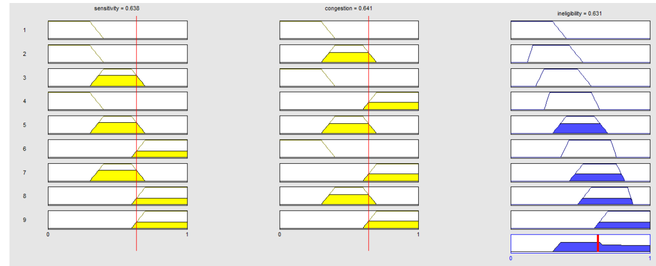
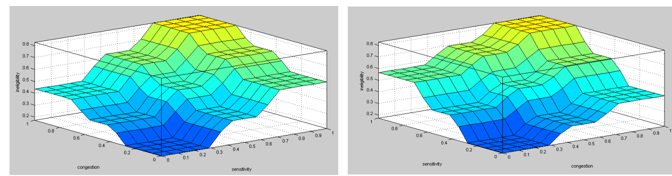


Fig. 5. Fuzzification and defuzzification with respect to rule base.



(a) Ineligibility factor with congestion and sensitivity (b) Ineligibility factor with sensitivity and congestion

Fig. 6. Change of ineligibility factor with sensitivity, congestion for proposed rule base.

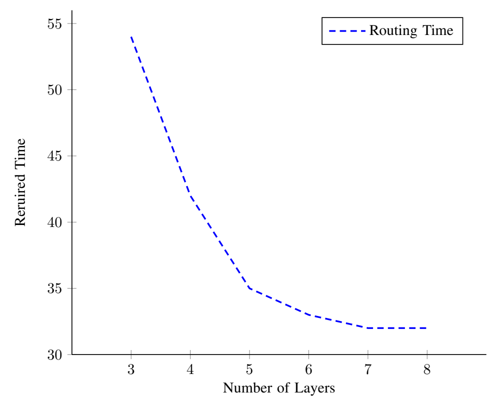


Fig. 7. Variation of Routing time with available number of layers for IBM 10 benchmark circuit [see table IV].

VI. Conclusion

This paper highlights the paramount aspect of global routing problem in 3D ICs by achieving a prominent degree of

TABLE III
Experimental Benchmark Statistics.

Benchmark	# Net	# Layer	Guiding Info Gen Time(s)	Routing Time(s)
ibm01	11507	4	85.0	3.0
		6	36.0	3.0
ibm02	18429	4	121.0	6.0
		6	85.0	4.0
ibm07	44394	6	247.0	22.0
		8	220.0	20.0
ibm08	47944	6	307.0	26.0
		8	297.0	21.0
ibm09	50393	6	294.0	28.0
		8	278.0	22.0
ibm10	64227	6	485.0	33.0
		8	472.0	32.0
ibm11	67016	6	372.0	74.0
		8	367.0	57.0
ibm12	67739	6	605.0	120.0
		8	582.0	96.0

TABLE V
COMPARISON BETWEEN PUBLISHED GLOBAL ROUTERS AND FUZZROUTE ON ISPD '98 BENCHMARK.

Benchmark	Labyrinth [16]		FastRoute3.0 [17]		NTHU-R [18]		BoxRoute 2.0 [19]		FGR [20]		FuzzRoute (**This Paper**)	
	wlen	cpu(s)	wlen	cpu(s)	wlen	cpu(s)	wlen	cpu(s)	wlen	cpu(s)	wlen	cpu(s)
ibm01	77K	21.2	64221	0.64	63321	4.17	62659	33	63332	10	46276	3.0
ibm02	205K	34.5	172223	0.85	170531	7.44	171110	36	168918	13	166922	4.0
ibm07	449K	228.1	369023	1.68	366288	15.89	365790	86	366180	18	357121	22.0
ibm08	470K	238.7	405935	1.82	405169	13.17	405634	90	404714	18	382855	26.0
ibm09	481K	505	414913	1.67	415464	11.59	413862	273	413053	20	403647	28.0
ibm10	680K	588	582838	3.61	580793	33.72	590141	352	578795	92	595465	33.0
Total	2362K	1615.5	2010K	10.27	2001K	85.98	2009K	870	1993K	171	1952K	116.0
Norm	1.21	13.92	1.03	0.088	1.03	.74	1.03	7.5	1.02	1.474	1	1

TABLE IV
LAYER WISE STATISTICS FOR IBM10 BENCHMARK CIRCUIT

#Layers	Guiding Info Gen Time(s)	Routing Time(s)
3	547.0	54.0
4	519.0	42.0
5	489.0	35.0
6	485.0	33.0
7	480.0	32.0
8	472.0	32.0

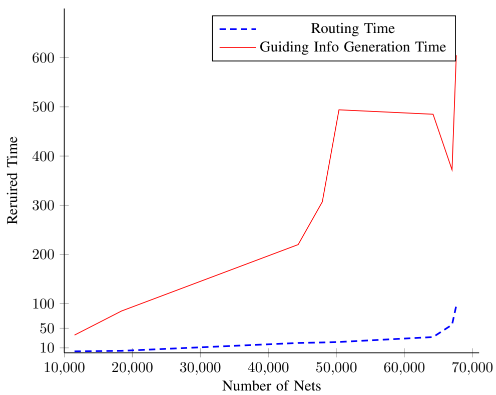


Fig. 8. Variation of Guiding information generation time and Routing time for different ISPD '98 benchmark circuits [see table III] with layer number = 6.

reliability and routability with a reasonable time complexity. The total methodology of the designed multi objective global router has been verified successfully for two-pin, multi-pin and critical intra, and inter-layer nets for 3D ICs. It may also be considered as a new type of guided global routing approach (using Fuzzy logic) for standard cells. The procedure is tested on ISPD'98 benchmark suites (for Fixed-die Placement) and compared with some well known global routers. Design of a foolproof global routing solution for 3D ICs considering other metrics as well, further comparison with other state of the art tools in real 3D IC benchmark suites, extension to mixed sized cell placements may be considered as some possible future extensions of the present work.

REFERENCES

[1] B. Goplen and S. S. Sapatnekar, "Thermal via placement in 3D ICs," in *Proceedings of the International Symposium on Physical Design*, pp. 167–174, 2005.

[2] J. Minz, E. Wong, and S. K. Lim, "Thermal and Crosstalk-Aware Physical Design For 3D System-On-Package," in *Proceedings of Electronic Components and Technology Conference*, pp. 824–831, 2005.

[3] E. H. Mamdani and S. Assilian, "An experiment in linguistic synthesis with a fuzzy logic controller," 1974.

[4] L. A. Zadeh, "Outline of a new approach to the analysis of complex systems and decision processes," vol. 3, pp. 28– 44, 1973.

[5] T. Zhang, Y. Zhan, and S. S. Sapatnekar, "Temperature-aware routing in 3D ICs," in *Proceedings of the Asia-South Pacific Design Automation Conference*, pp. 309–314, 2006.

[6] P. Ghosal, H. Rahaman, and P. Dasgupta, "Uniform Thermal Distributions in Placement of Standard Cells and Gate Arrays: Algorithms and Results," in *Proceedings of the 13th IEEE/VSI VLSI Design and Test Symposium (VDAT 2009)*, pp. 69–78, 2009.

[7] P. Ghosal, H. Rahaman, and P. Dasgupta, "Minimizing thermal disparities during placement in 3d ics," in *Computational Science and Engineering (CSE), 2010 IEEE 13th International Conference on*, pp. 160–167, 2010.

[8] P. Ghosal, H. Rahaman, and P. Dasgupta, "Cell level thermal placement in 3d ics," in *India Conference (INDICON), 2010 Annual IEEE*, pp. 1–4, 2010.

[9] P. Ghosal, H. Rahaman, and P. Dasgupta, "An Experimental Study of Interconnection Length in 3D and 2D VLSI," in *Proceedings of IEEE Latin American Symposium on Circuits and Systems*, 2010.

[10] P. Ghosal, H. Rahaman, and P. Dasgupta, "Thermal Aware Placement in 3D ICs," in *Proceedings of 2nd International Conference on Advances in Recent Technologies in Communication and Computing (ARTCom 2010)*, pp. 66–70, 2010.

[11] M. Pathak and S. K. Lim, "Performance and Thermal-Aware Steiner Routing for 3-D Stacked ICs," in *Proceedings of Computer-Aided Design of Integrated Circuits and Systems*, pp. 1373–1386, 2009.

[12] "[omitted for blind review]," in *Symposium on VLSI, 2008. ISVLSI '08. IEEE Computer Society Annual*, Apr 2008.

[13] "[omitted for blind review]," in *Fuzzy Systems (FUZZ), 2013 IEEE International Conference on*, 2013.

[14] S. Bandyopadhyay, "Automatic Determination of the Number of Fuzzy Clusters Using Simulated Annealing with Variable Representation," in *Proceedings of ISMIS 2005*, pp. 549–602, 2005.

[15] C. J. Alpert, "The ISPD98 circuit benchmark suite," in *ACM International Symposium on Physical Design*, pp. 80–85, 1998.

[16] R. Kastner, E. Bozorgzadeh, and M. Sarrafzadeh, "Pattern routing: use and theory for increasing predictability and avoiding coupling," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 21, no. 7, pp. 777–790, 2002.

[17] Y. Zhang, Y. Xu, and C. Chu, "FastRoute3.0: A Fast and High Quality Global Router Based on Virtual Capacity," in *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design*, pp. 344–349, 2008.

[18] J.-R. Gao, P.-C. Wu, and T.-C. Wang, "A new global router for modern designs," in *Proceedings of the 2008 Asia and South Pacific Design Automation Conference*, ASP-DAC '08, (Los Alamitos, CA, USA), pp. 232–237, IEEE Computer Society Press, 2008.

[19] M. Cho, K. Lu, K. Yuan, and D. Pan, "Boxrouter 2.0: architecture and implementation of a hybrid and robust global router," in *Computer-Aided Design, 2007. ICCAD 2007. IEEE/ACM International Conference on*, pp. 503–508, 2007.

[20] J. Roy and I. Markov, "High-performance routing at the nanometer scale," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 27, no. 6, pp. 1066–1077, 2008.