

# Statistical Process Variation Analysis of a Graphene FET based $LC$ -VCO for WLAN Applications

Md Abir Khan\*, Saraju P. Mohanty<sup>†</sup> and Elias Kougianos<sup>‡</sup>

NanoSystem Design Laboratory (NSDL, <http://nsdl.cse.unt.edu>)

Dept. of Computer Science and Engineering, University of North Texas, Denton, TX 76203, USA.

Email: Md.AbirKhan@my.unt.edu\*, saraju.mohanty@unt.edu<sup>†</sup>, and elias.kougianos@unt.edu<sup>‡</sup>

**Abstract**—Graphene which is a single atom layer of carbon film with the interesting properties of high carrier mobility, high carrier concentration, high thermal conductivity, high velocity saturation, and reduced short channel effects, is emerging as a replacement of the ubiquitous silicon. This is particularly true for high-speed analog and radio-frequency electronics due to low  $I_{on}/I_{off}$  ratio. In this paper, design exploration of a graphene FET (GFET) based  $LC$ -VCO is performed with wireless (WLAN) as the target application. Verilog-A based GFET modeling is performed. The model is used in design simulation, characterization, and sensitivity analysis of a cross-coupled version of an  $LC$ -VCO. In order to analyze the effects of nanoscale process variations, statistical process variation analysis of the GFET based  $LC$ -VCO is performed for selected figures of merit through exhaustive Monte Carlo simulations. Power dissipation and quality factor are also analyzed and their characteristic data are illustrated to obtain a comprehensive description of the circuit. Frequency and phase noise are observed to be within the nominal design range having standard deviation 0.06 GHz and 7.78 dBc/Hz corresponding to 2.35% and 9.03% of the mean, respectively, for the total statistical variation of the parameters.

## I. INTRODUCTION

Graphene is being considered as a promising material for next generation nanoelectronic device fabrication. Graphene does not have implicit bandgap and its low on/off current ratio ( $I_{on}/I_{off}$ ) is not suitable for design in the digital domain. On the other hand, the high carrier mobility of Graphene FETs is useful for the design of RF devices [1]. Graphene exhibits ambipolar property which has been exploited towards the design of multipliers [2], ambipolar RF mixers [3] and other devices. This ambipolar property is also utilized in the design of a polarity controllable graphene inverter [4].

As new technology, graphene based devices need extensive performance analysis. To analyze process variation effects on a Graphene based oscillator circuit, the circuit is designed at schematic level for WLAN frequency ranges. A sensitivity analysis provides information on how the GFET  $LC$ -VCO behaves for different GFET parameters. Monte Carlo simulations are performed to analyze the effects of parameter variation for frequency, phase noise, power dissipation and quality factor.

The rest of the paper is organized as follows. The novel contributions of this paper are discussed in Section II. The design and characterization of the GFET-based  $LC$ -VCO is discussed in Section III. Sensitivity analysis is presented in Section IV. Statistical process variation analysis is performed in Section V. Conclusions are presented in Section VI.

## II. NOVEL CONTRIBUTIONS OF THIS PAPER

The contributions of this paper can be summarized in the following:

- 1) Verilog-A based modeling of the graphene FET (GFET) is performed.
- 2) A GFET based  $LC$ -VCO is designed and characterized.
- 3) A sensitivity analysis of the  $LC$ -VCO for selected GFET parameters is performed.
- 4) Statistical process variation analysis of the  $LC$ -VCO for selected GFET parameters is also presented.

Device models in Verilog-A are compatible with analog circuit simulators and hence provide new exploration tools for the design and analysis of GFET based circuits in SPICE. The VCO designed in this work follows a cross coupled topology where saturation and the second linear region of GFET  $I - V$  characteristics are utilized.

## III. GRAPHENE BASED $LC$ -TANK OSCILLATOR

Graphene based field effect transistors (GFETs) are being explored for applications in high performance electronic devices [5], [6]. Graphene has very high carrier mobility and can be used for high frequency applications [7]. Hence GFET based RF devices such as mixers, a voltage amplifier [8], and a frequency multiplier/doubler [9], [10] are explored currently and are under fabrication. In this paper, graphene oscillator design issues are explored with a design of a cross coupled  $LC$  VCO having center frequency of 2.64 GHz. This frequency is selected to design a fully integrated synchronous oscillator for WLAN applications [11].

The frequency of oscillation ( $f_0$ ) of an  $LC$  tank is given by the following expression [12]:

$$f_0 = \frac{1}{2\pi\sqrt{LC}}, \quad (1)$$

where the capacitance  $C$  is given by:

$$C = C_{GS} + C_{GD} + C_{\text{varactor}}. \quad (2)$$

$C_{GS} + C_{DG}$  are the parasitic capacitance of the GFET, while the varactor capacitance provides the tuning mechanism for the oscillation. For self-sustained oscillation, the following criterion must be fulfilled:

$$g_{\text{active}} > \frac{RC}{L}, \quad (3)$$

where  $g_{active}$  is the transconductance of the active device that compensates the losses in the  $LC$  tank. To keep power dissipation within reasonable limits, the bias current must be limited within a specified range:

$$I_{bias} \geq I_{max} \quad (4)$$

The oscillator voltage swing is defined by:

$$v_{tank} = \frac{I_{bias}}{g_{tank}} \quad (5)$$

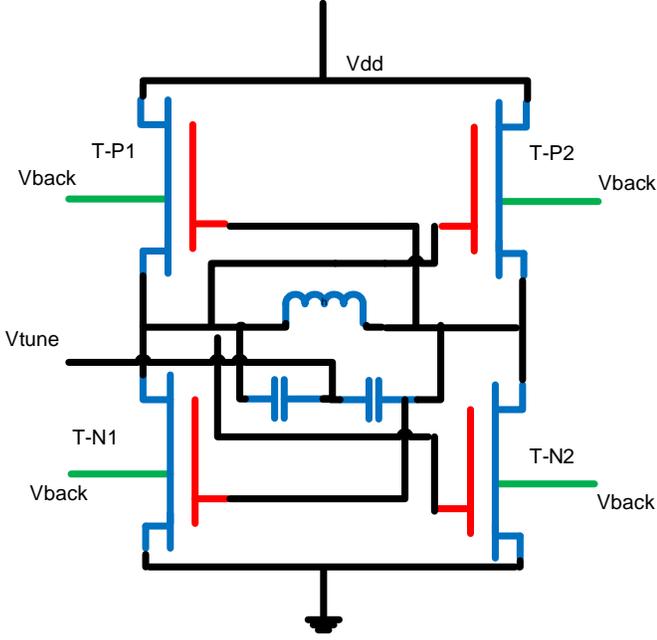
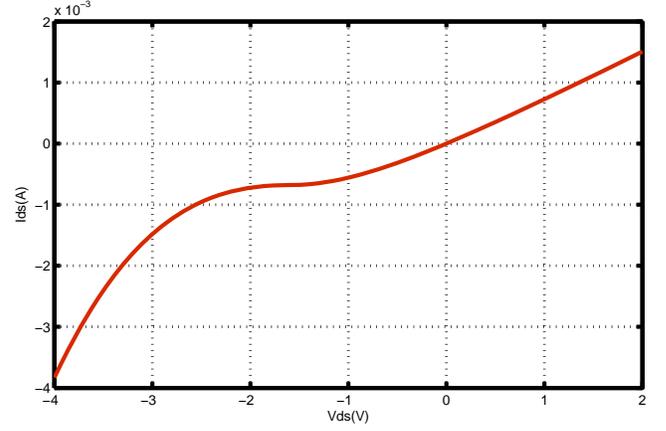


Fig. 1. Graphene  $LC$  VCO Topology

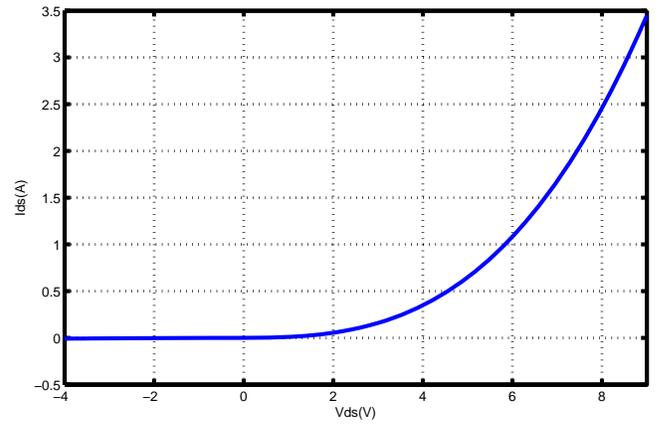
The topology considered for this design is a cross coupled  $LC$  oscillator shown in figure(1) where the GFETs are active devices to compensate for the losses in the  $LC$  tank. Varactors are used as variable tuning capacitors under control of  $v_{tune}$ . A proper operating point of the GFET needs to be selected to satisfy equations (3) and (4). The inductance is then determined. The inner radius, inductor width, spacing and number of turns are design variable affecting  $L$ . Keeping everything else fixed, we can consider the inner radius of a spiral inductor as a design variable. After the required optimization, the proper inductance can be found with reasonable  $g_{tank}$  that provides desired  $LC$  tank voltage swing based on equation (5).

TABLE I  
P-CHANNEL GFET PARAMETERS

| Device Parameter | Value                        |
|------------------|------------------------------|
| $\mu$            | $0.3 \text{ m}^2/\text{s/V}$ |
| $W_P$            | $1.6 \text{ }\mu\text{m}$    |
| $l$              | $1.6 \text{ }\mu\text{m}$    |
| $R_s$            | $600 \text{ }\Omega$         |
| $t_{ox}$         | $10 \text{ nm}$              |



(a)  $I_{ds}$  vs  $V_{ds}$  for P-Type GFET



(b)  $I_{ds}$  vs  $V_{ds}$  for N-Type GFET

Fig. 2.  $I - V$  Characteristics of the GFETs.

TABLE II  
N-CHANNEL GFET PARAMETERS

| Device Parameters | Values                       |
|-------------------|------------------------------|
| $\mu$             | $0.3 \text{ m}^2/\text{s/V}$ |
| $W_N$             | $1.6 \text{ }\mu\text{m}$    |
| $l$               | $1.6 \text{ }\mu\text{m}$    |
| $R_s$             | $4000 \text{ }\Omega$        |
| $t_{ox}$          | $10 \text{ nm}$              |

Tables I and II list the GFET parameters. Figures 2(a) and 2(b) show the  $I - V$  characteristics the GFETs near the operating point. In the case of the PFET there is a small saturation region evident at the operating point. This saturation point is modeled in both charge control model [13] utilized in this paper and also in the model based on velocity saturation [14]. When the top gate voltage becomes more negative, the operating point enters the kink region where the displacement current is modeled by a second linear region [15]. In this operating region, graphene illustrates ambipolar characteristics which are utilized in [2]–[4]. In the case of the NFET, the device is operated in the second linear region which is above the kink.

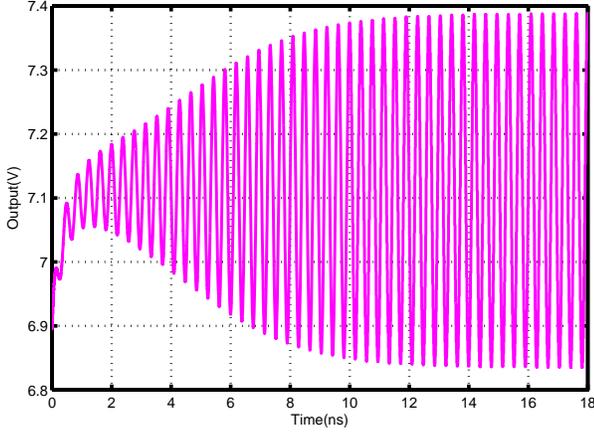


Fig. 3. Output voltage of the GFET based VCO.

The chosen application for this design is as a synchronous oscillator for WLAN having center frequency  $f_0 = 2.64$  GHz. Figures 4(a) and 4(b) illustrate phase noise performance and available tuning range at current operating condition, respectively. Phase noise at  $f_0$  frequency is  $-92.66$  dBc/Hz. The output voltage swing remains almost stable for the entire frequency range at  $0.55 V_{p-p}$ . Table III summarizes the characteristics of the oscillator.

TABLE III  
CHARACTERIZATION OF THE GFET VCO.

| No. | Parameter                     | Value           |
|-----|-------------------------------|-----------------|
| 1   | $f_0$                         | 2.64 GHz        |
| 2   | $V_{tank_{p-p}}$              | 0.55 V          |
| 3   | $V_{supply}$                  | 9 V             |
| 4   | $I_{bias}$                    | 0.88 mA         |
| 5   | Tuning Range                  | 4.2%            |
| 6   | Phase noise (at 1 MHz offset) | $-92.66$ dBc/Hz |

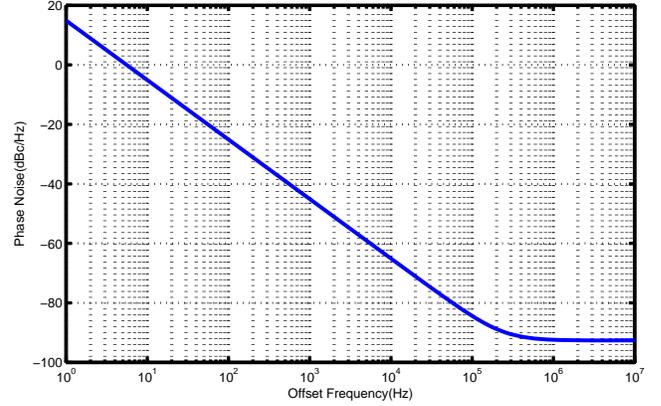
For comparative purposes, a CMOS version of the VCO is designed using 180 nm technology. The same topology is considered as above. Table IV illustrates the characteristics of this design.

TABLE IV  
CHARACTERIZATION OF CMOS  $LC$ -VCO.

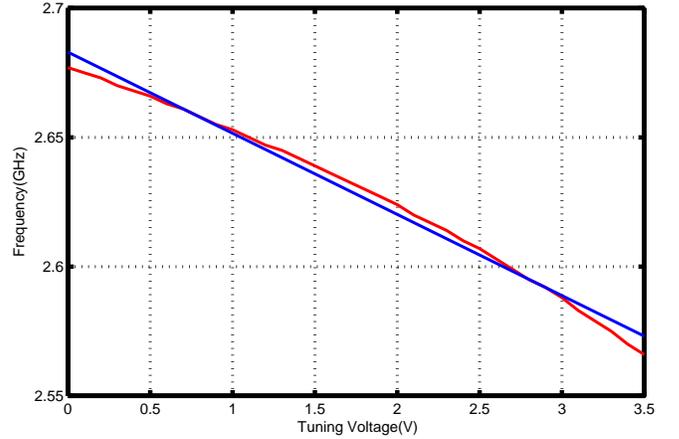
| No. | Parameter                     | Value            |
|-----|-------------------------------|------------------|
| 1   | $f_0$                         | 2.64 GHz         |
| 2   | $V_{tank_{p-p}}$              | 1.9 V            |
| 3   | $V_{supply}$                  | 2.5 V            |
| 4   | $I_{bias}$                    | 1.1 mA           |
| 5   | Tuning Range                  | 15.53 %          |
| 6   | Phase noise (at 1 MHz offset) | $-161.1$ dBc/Hz  |
| 7   | $W_N$                         | $5 \mu\text{m}$  |
| 8   | $W_P$                         | $10 \mu\text{m}$ |

#### IV. SENSITIVITY ANALYSIS

A sensitivity analysis has been performed on the major characteristic of the VCO due to variation of GFET parameters.



(a) Phase noise vs Frequency



(b) Frequency vs  $V_{tune}$ . The linear fit has  $R^2=0.9953$ .

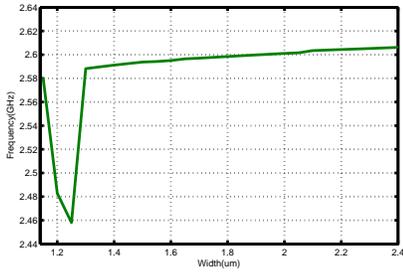
Fig. 4. GFET-based  $LC$ -VCO characterization.

Four major characteristic parameters of a VCO are selected: (i) Frequency, (ii) Phase noise, (iii) Power dissipation, and (iv) Quality Factor ( $Q$ ). Figures 5, 6, 7 and 8 illustrate the dependency of these four characteristics on selected GFET parameters. One parameter is varied at a time while the other parameters maintain their nominal values, as indicated in Tables I and Table II. The parameters varied were (i) width, (ii) length, (iii) mobility, (iv) drain to source resistance, and (v) top gate oxide thickness. However, due to space limitations, only the variation due to the first three parameters is shown in figures 5, 6, 7 and 8.

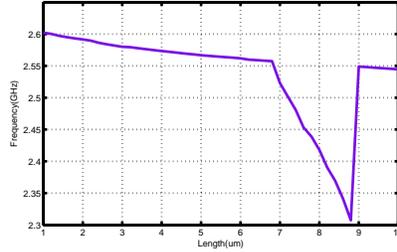
The  $Q$  factor of this circuit has been calculated utilizing short circuit admittance or  $Y$  parameters for a two port circuit having differential configuration. For the differential circuit,  $Q$  can be calculated from the following expression:

$$Q = \frac{\Im(Y_{11} + Y_{22} - Y_{12} - Y_{21})}{\Re(Y_{11} + Y_{22} - Y_{12} - Y_{21})}, \quad (6)$$

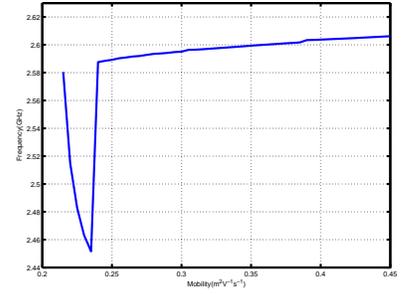
where  $\Im$  indicates the imaginary part of an expression and  $\Re$  its real part. For a symmetric configuration of the differential



(a) Frequency vs. Width

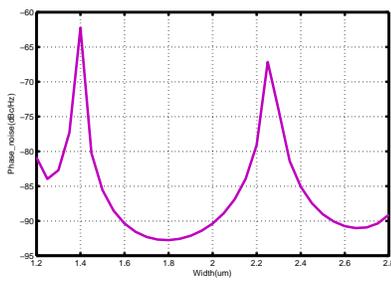


(b) Frequency vs. Length

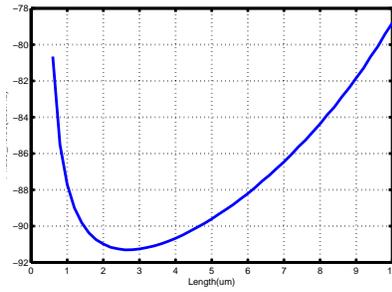


(c) Frequency vs. Mobility

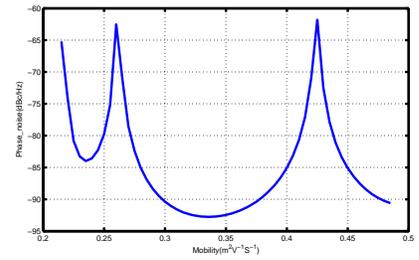
Fig. 5. Dependence of VCO center frequency on selected GFET parameters.



(a) Phase Noise vs. Width

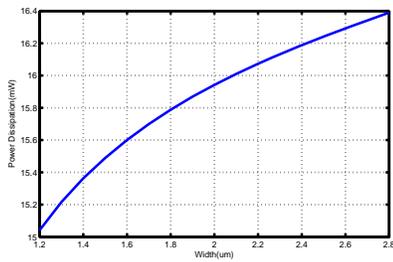


(b) Phase Noise vs. Length

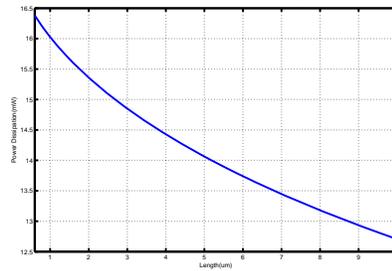


(c) Phase Noise vs. Monility

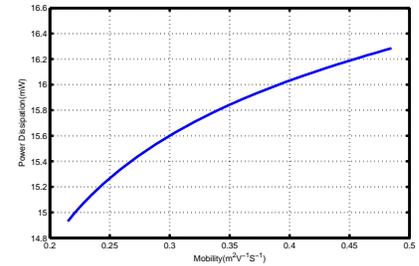
Fig. 6. Dependence of VCO phase noise on selected GFET parameters.



(a) Power dissipation vs. Width

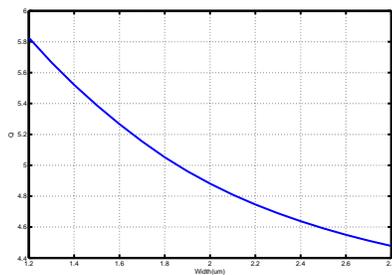


(b) Power dissipation vs. Length

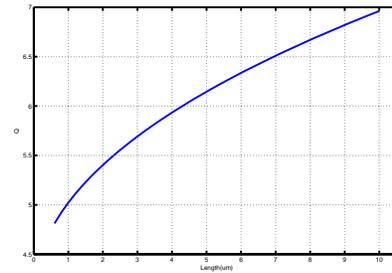


(c) Power dissipation vs. Mobility

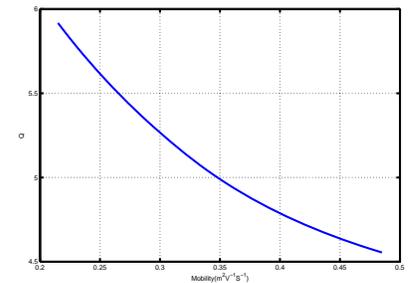
Fig. 7. Dependence of VCO power dissipation on selected GFET parameters.



(a)  $Q$  vs. Width



(b)  $Q$  vs. Length



(c)  $Q$  vs. Mobility

Fig. 8. Dependence of oscillator quality factor ( $Q$ ) on selected GFET parameters.

circuit, equation 6 reduces to the following expression:

$$Q = \frac{\Im(Y_{11} - Y_{12})}{\Re(Y_{11} - Y_{12})} \quad (7)$$

There are sharp decreases in figure 5(a), 5(b) and 5(c) around the resonance point.

Figure 6 illustrates the phase noise performance due to variation of different parameters. In figures 6(a) and 6(c), multiple peaks are observed. This can be explained from the relationship of  $Q$  and signal power to the device parameters considered here. As it is evident from figure 8,  $Q$  decreases with width, mobility and increases with other parameters while signal power exhibits opposite behavior. But both characteristics contribute to reduce phase noise performance while they increase. So due to parametric variation, when their multiplication becomes maximum, minimum phase noise can be found. Peaks are observed at those points when their combined contribution is in minimum value and from figure 7 and 8 this is evident that this situation should occur eventually.

From these plots the minimum phase noise point within the design space can be located. The phase noise shown in Table III is at 1 MHz offset from the 2.6 GHz oscillating frequency. This offset is selected considering the WLAN application of this designed VCO [11].

Figure 7 illustrates the relationship of power dissipation with different parameters. Figures 7(a) and 7(c) show increase in power dissipation as both cause transistor current to increase.

Figure 8 provides detailed sensitivity of the  $Q$  factor of the oscillator on various GFET parameters.  $Q$  varies within 4.5 to 8 in the design space and a suitable point can be located that provides the desired  $Q$ .

## V. STATISTICAL ANALYSIS OF GFET LC-VCO

Monte Carlo simulations were performed by varying the GFET length  $L$ , width  $W$ , drain to source resistance of NFET  $R_{ds}$ , top gate oxide thickness  $t_{ox}$  and mobility  $\mu$ . Though interrelated, these parameters can be adjusted within the feasible range to achieve desired characteristic that may provide desired VCO performance/figures of merit [14], [16]. Also these parameters contribute to the change of VCO characteristic as observed in figure 9. To design a synchronous oscillator for a WLAN application, the VCO needs to have good tuning characteristics with acceptable phase noise performance [11]. Power dissipation should also be minimized.

The Monte Carlo runs consisted of  $N=1000$  samples. Figure 9(a) illustrates the center frequency distribution in histogram form. From this figure, it is seen that most of the samples fall within the range of 2.5 to 2.62 GHz which is nominal for the circuit. A few samples can be found at around 2.2 to 2.4 GHz due to the creation of resonance, as observed earlier. The statistical characterization of the phase noise is shown in figure 9(b). It is observed that most values fall within the range of -80 dBc/Hz to -93 dBc/Hz. Figures 9(c) and 9(d) show the power and  $Q$  factor distributions.

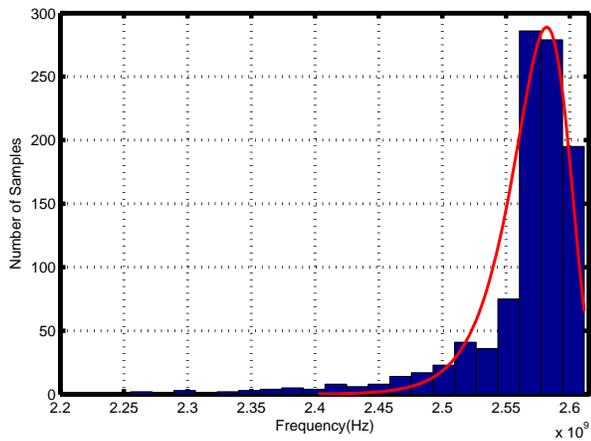
In figure 9, an extreme value distribution curve of type I is fitted over the histograms of the frequency and phase noise data [17], [18]. The fitting curve for power dissipation is lognormal distribution and for the  $Q$  factor is a normal distribution. Table V summarizes the characteristics of the Monte Carlo statistical data for each VCO property. The fitted distribution match the statistical data closely.

## VI. CONCLUSIONS

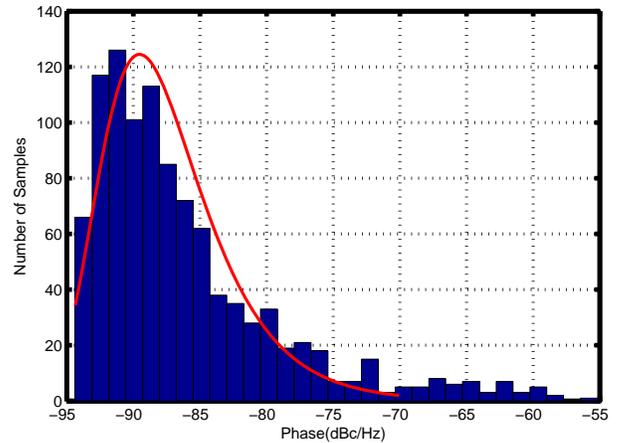
In this paper a verilog-A GFET model was developed and used to design, simulate and characterize a cross-coupled LC-VCO using an industry-standard analog circuit simulator (Cadence's SPECTRE). The GFET model is verified through  $I - V$  characterization. The LC-VCO is designed to be compatible with oscillators used in WLAN applications. Its tuning sensitivity is presented and the linearity of the VCO is confirmed. A standard 180 nm CMOS version of design is also presented for comparison. Monte Carlo simulation was performed for statistical process variation analysis. The Verilog-A model of GFET implemented in this work can be utilized to explore further other circuits such as mixers, voltage doubler etc. Moreover, the work performed in this paper can be extended to physical level design where circuit parasitics can be included. The simulation results presented in this paper will be useful for future works that entail GFET based LC-VCO design and optimization.

## REFERENCES

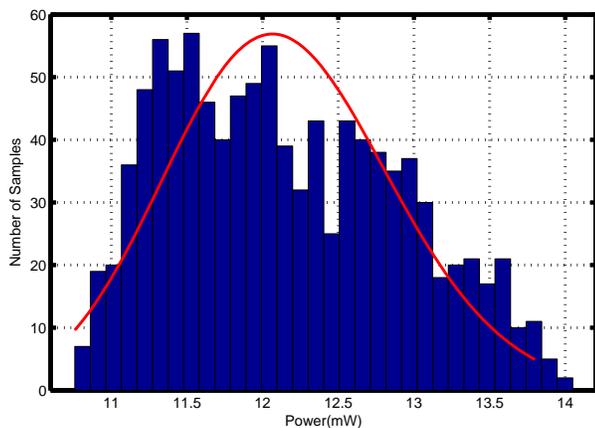
- [1] J. S. Moon and D. K. Gaskill, "Graphene: Its fundamentals to future applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 59, no. 10, pp. 2702–2708, Oct. 2011.
- [2] H. Wang, A. Hsu, K. K. Kim, J. Kong, and T. Palacios, "Gigahertz ambipolar frequency multiplier based on CVD graphene," in *Proceedings of the 2010 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2010, pp. 23.6.1–23.6.4.
- [3] H. Wang, A. Hsu, J. Wu, J. Kong, and T. Palacios, "Graphene-based ambipolar RF mixers," *IEEE Electron Device Letters*, vol. 31, no. 9, pp. 906–908, Sept. 2010.
- [4] N. Harada, K. Yagi, S. Sato, and N. Yokoyama, "A polarity-controllable graphene inverter," *Applied Physics Letters*, vol. 96, no. 1, pp. 012102–012102, 2010.
- [5] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, "Electric field effect in atomically thin carbon films," *Science*, vol. 306, no. 5696, pp. 666–669, 2004.
- [6] M. I. Katnelson, "Graphene: Carbon in two dimensions," *Materials Today*, vol. 10, pp. 20–27, 2007.
- [7] S. V. Morozov, K. S. Novoselov, M. I. Katsnelson, F. Schedin, D. C. Elias, J. A. Jaszczak, and A. K. Geim, "Giant intrinsic carrier mobilities in graphene and its bilayer," *Physical Review Letters*, vol. 100, no. 1, p. 16602, Jan. 2008.
- [8] S. J. Han, K. A. Jenkins, A. Valdes Garcia, A. D. Franklin, A. A. Bol, and W. Haensch, "High-frequency graphene voltage amplifier," *Nano Letters*, vol. 11, no. 9, pp. 3690–3693, 2011.
- [9] M. E. Ramon, K. N. Parrish, S. F. Chowdhury, C. W. Magnuson, H. C. P. Movva, R. S. Ruoff, S. K. Banerjee, and D. Akinwande, "Three-gigahertz graphene frequency doubler on quartz operating beyond the transit frequency," *IEEE Transactions on Nanotechnology*, vol. 11, no. 5, pp. 877–883, Sept. 2012.
- [10] H. Wang, D. Nezich, J. Kong, and T. Palacios, "Graphene frequency multipliers," *IEEE Electron Device Letters*, vol. 30, no. 5, pp. 547–549, May 2009.
- [11] Y. Deval, J.-B. Begueret, A. Spataro, P. Fouillat, and F. Badets, "A 2.7 V, 2.64 GHz fully integrated synchronous oscillator for WLAN applications," in *Proceedings of the 25th European Solid-State Circuits Conference (ESSCIRC)*, 1999, pp. 210–213.



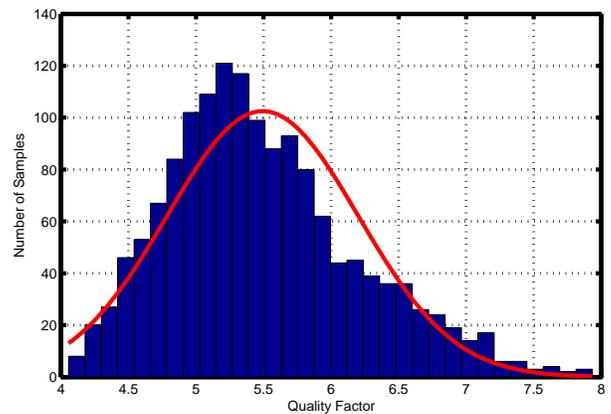
(a) Frequency histogram



(b) Phase noise histogram.



(c) Power dissipation histogram



(d)  $Q$  factor histogram.

Fig. 9. Statistical analysis of the GFET  $LC$ -VCO: Monte Carlo derived histograms for  $N=1000$  samples. The solid lines correspond to fitted probability density functions.

TABLE V  
STATISTICAL CHARACTERIZATION OF GRAPHENE FET BASED  $LC$ -VCO.

| Parameters           | Mean ( $\mu$ ) | Mean (Fitted) | St. Dev. ( $\sigma$ ) | St. Dev. (Fitted) |
|----------------------|----------------|---------------|-----------------------|-------------------|
| Frequency            | 2.56 GHz       | 2.57 GHz      | 60 MHz                | 28 MHz            |
| Phase Noise (dBc/Hz) | -86.01         | -87.34        | 7.78                  | 4.87              |
| Power Dissipation    | 12.15 mW       | 12.13 mW      | 758 $\mu$ W           | 738 $\mu$ W       |
| $Q$ Factor           | 5.49           | 5.49          | 0.84                  | 0.71              |

- [12] O. Garitselov, S. P. Mohanty, and E. Kougiianos, "Accurate Polynomial Metamodeling-Based Ultra-Fast Bee Colony Optimization of a Nano-CMOS Phase-Locked Loop," *Journal of Low Power Electronics*, vol. 8, no. 3, pp. 317–328, June 2012.
- [13] B. Scott and J. Leburton, "Modeling of the output and transfer characteristics of graphene field-effect transistors," *IEEE Transactions on Nanotechnology*, vol. 10, no. 5, pp. 1113–1119, Sept. 2011.
- [14] I. Meric, M. Y. Han, A. F. Young, B. Ozyilmaz, P. Kim, and K. L. Shepard, "Current saturation in zero-bandgap, top-gated graphene field effect transistors," *Nature Nanotechnology*, vol. 3, pp. 654–659, November 2008.
- [15] I. J. Umoh and T. J. Kazmierski, "VHDL-AMS model of a dual gate graphene FET," in *Proceedings of the 2011 Forum on Specification and Design Languages (FDL), 2011*, Sept. 2011, pp. 1–5.
- [16] H. Xu, Z. Zhang, H. Xu, Z. Wang, S. Wang, and L.-M. Peng, "Top-gated graphene field-effect transistors with high normalized transconductance and designable dirac point voltage," *ACS Nano*, vol. 5, no. 6, pp. 5031–5037, Apr. 2011.
- [17] D. Ghai, S. P. Mohanty, and E. Kougiianos, "Design of Parasitic and Process-Variation Aware Nano-CMOS RF Circuits: A VCO Case Study," *IEEE Trans. VLSI Syst.*, vol. 17, no. 9, pp. 1339–1342, September 2009.
- [18] S. Coles, *An Introduction to Statistical Modeling of Extreme Values*. Springer-Verlag, 2001.