Variability-Aware Design of Double Gate FinFET-based Current Mirrors

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ABSTRACT

With the technology trend moving towards smaller geometries and improved circuit performances, multigate transistors are expected to replace the traditional bulk devices. The double-gate FinFET lends itself to a rich design space using various configurations of the two gates. Accurate current mirroring is a critical analog design requirement in many applications. Current mirror is an essential component in analog design for biasing and constant current generation. This paper presents the exploration of different configurations of a double gate fully depleted SOI based FinFETs for efficient design of current mirror designs. In particular, comparison among the important Figures-of-Merit (FoMs) current mirror designs including mismatch, variability, output resistance (r_0), compliance voltage (V_{CV}) is presented for: (1) shorted-gate (SG), (2) independent-gate (IG), and (3) low-power (LP) configurations. Based on the results obtained, guidelines are presented for the designer for current mirror design using FinFET.

Keywords

Analog design; current mirrors; FinFET; mismatch; independent-gate

1. INTRODUCTION

The current mirrors are essential building blocks in analog integrated circuits which affect the qualitative performance of the system. The current mirrors are used as active loads as they offer high impedance. They are also used as biasing structures as they provide better tolerance to the variations in power supply and temperature [2]. An ideal current mirror, which may not be practically realized, has the following:

- Infinite output resistance ($r_0 = \infty$).
- Provide the same current regardless of voltage across it, in other words, there are no compliance range requirements (V_{CV}= 0).
- No sensitivity to real-world effects like mismatch (mismatch = 0) and process variations.

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The major drawbacks of conventional bulk CMOS current mirrors in analog design tend to be the following: mismatch, output resistance degradation and compliance voltage increase, which is due to aggressive technology scaling. One of the candidates to replace planar bulk CMOS technology is the double gate FinFET (DG-FinFET) technology [3, 4]. FinFETs are particularly appealing because they allow suppression of short channel effects (SCE), high transconductance and optimal subthreshold voltage. In DG-FinFETs, there is reduced mismatch from random dopant fluctuations due to undoped or lightly doped body and reduced carrier mobility degradation. DG-FinFETs also provide design flexibility at circuit level with two gates as the threshold voltage can be adjusted using bias applied on the back-gate [22]. This feature offers the following advantages: versatile functionality from the same set of devices, and reduction of layout area and a higher speed/lower power consumption over equivalent conventional circuits [12]. The current mirror circuit is implemented using the FinFET technology to explore these advantages.

The following modes of DG-FinFET configurations are considered for circuit design: (1) the shorted-gate (SG) mode with transistor gates tied together, (2) the low-power (LP) mode where the back-gate is tied to a reverse-bias voltage to reduce leakage power, and (3) the independent gate (IG) mode where independent signals are used to drive the two device gates [3, 4]. In the current paper we consider these configurations for current mirror designs to study their impact on current mirror design. The objective is the comparative analysis of the various DG-FinFET configurations and trends of the FoMs of the current mirrors to evaluate the advantages of FinFETs on analog designs.

The remainder of this paper is organized as follows: Section 2 summarizes the contributions of this paper. Section 3 presents the related research. A discussion of the FinFET models and FinFET configuration-based current mirrors is presented in Section 4. Section 5 presents discussions on variability and mismatch for the various DG-FinFET configuration-based current mirrors. A performance analysis for FoMs under consideration is presented in Section 6. Section 7 discusses the design guidelines for FinFET based current mirrors. This is followed by conclusions and directions for future research in Section 8.

2. CONTRIBUTIONS OF THIS PAPER

The *novel contributions* of this paper include the following:

1. A comparative study is presented among the SG, IG and LP configurations of the double gate FinFET device for current mirror design. A 32nm n-type FinFET current mirror has been used for this comparison.

2. Study of mismatch, variability, output resistance (r_0), compliance voltage (V_{CV}) is presented for SG, IG and LP mode double gate FinFET current mirrors.
3. A novel algorithm is presented for measuring mismatch in the configurations of double gate FinFET current mirrors using Design of Experiments (DOE) and polynomial modeling. Mismatch models are developed for each configuration.
4. A novel algorithm is presented for measuring variability in the various double gate FinFET configuration-based current mirrors. The coefficient of variation (c_v) is presented for each configuration.
5. Guidelines are formed for current mirror design using double gate FinFET current mirrors.

3. RELATED PRIOR RESEARCH

The feasibility of FinFET based digital and analog circuits has been well established in [11, 17, 4, 3, 7]. In [6], a back-gate voltage tuning based statistical optimization is performed in a FinFET-based SRAM array. In analog design, the exploration has also been done at the device level [16, 15]. The impact of fin width on FinFET characteristics is analyzed in [13]. The analog performance of Double Gate, Tri-Gate FinFET and single-gate (SG) SOI MOSFETs are compared in [20]. The performances of FinFET are studied for analog/RF circuits in [21, 8, 18]. The various configurations of the FinFET device for analog applications are presented in [12, 9]. However, the main focus is on forward bias configurations and not reverse bias configurations, which are becoming increasingly popular for digital applications and are covered in the current paper.

The research presented in this paper is the advancement of research in [5], in which a comparison of the SG, IG and LP FinFET modes is presented for analog design using FoMs like open circuit gain, transition frequency, and variability. The current paper deals with current mirror design focusing more on the relevant FoMs like compliance voltage and output resistance. Apart from variability, current mismatch is measured which is crucial for current mirror design.

4. DOUBLE GATE FINFET-BASED CURRENT MIRRORS

Current mirrors work on the principle that if the gate-source potentials of two identical FinFET devices are equal, the channel current is equal. For a good current source, the devices must operate in the saturation region. In case of the reference transistor (REF) of the mirror, the drain current $I_D = I_{REF}$. Reference current I_{REF} is a known current (I_{REF}=35μA), provided by the current source ensuring that it is constant and independent of voltage supply variations [2]. Using $V_{DG-REF} = 0$ for transistor REF, I_{REF} sets the value of V_{GS-REF}. The circuit in figure 1 forces the same V_{GS-REF} to apply to the output transistor OUT. If OUT is also biased with V_{DG-OUT}=0 and provided REF transistors and OUT have good matching, we have $I_{OUT} = I_{REF}$, i.e. the output current is same as the reference current when V_{DG-OUT}=0 for the output transistor, given both transistors are matched.

Fig. 1 shows shorted-gate (SG), independent-gate (IG), and Low-Power (LP) n-type FinFET current mirrors, where V_{gf} denotes the voltage applied at the front gate, and V_{gb} denotes the voltage applied at the back gate. In the SG mode, the front and back gates are tied together, while in the independent-gate (IG) mode, the top part of the gate is etched out giving rise to two independent gates and the back-gate voltage (V_{gb}) is set to 0 V [15]. The low-power (LP)-mode applies a reverse-bias voltage of -0.2V to the back-gate.

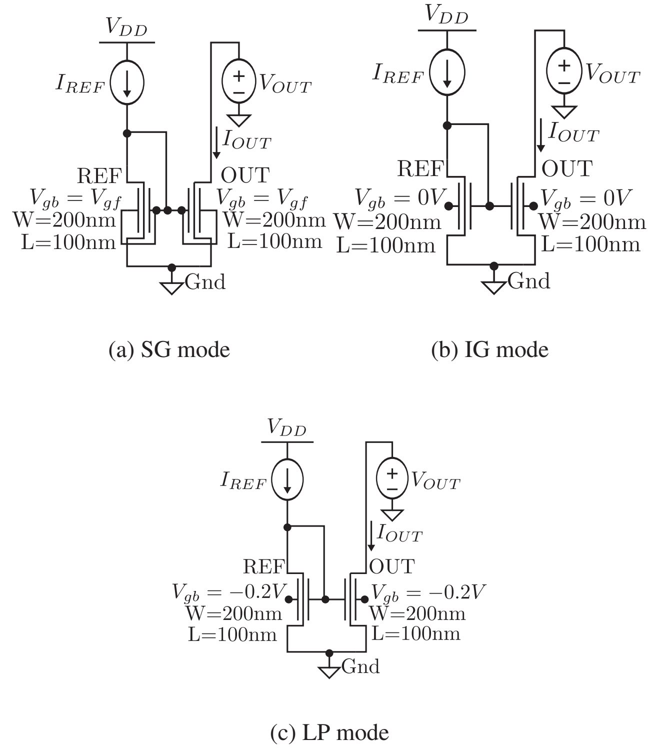


Figure 1: Circuit diagram and simulation setup for (a) SG mode, (b) IG mode and (c) LP mode DG-FinFET based current mirrors.

We use an equivalent sub-circuit model for a FinFET device instead of TCAD simulators as the existing compact models are accurate and simple to use [1]. The FinFET is inherently an SOI transistor as the bottom of a FinFET structure sits on top of a layer of SiO_2. The SOI thickness (T_{si}) is very thin in a typical FinFET process making the silicon body fully depleted. The fully depleted SOI model of BSIM (BSIM FD SOI) is used as the model basis for each sub-transistor. Two fully depleted SOI devices have been used as the front and back transistors, respectively. To make this sub-circuit compatible with standard circuit simulators (SPICE), BSIM SOI has been used as the model for each device. The current conduction controlled by the front and back gate in a FinFET [22] is captured by using two single-gate transistors. Each sub-transistor has its own definitions of gate voltage (V_g), threshold voltage (V_{Th}), and gate-oxide thickness (T_{ox}). The key parameter values for the FinFET models at 32nm node are shown in Table 1. The body thickness (T_{Si}) of a single fin is equal to the silicon channel thickness.

Table 1: 32nm n-type FinFET Device Nominal Values.

Parameter	Value
Oxide Thickness T_{ox}(nm)	1.4 nm
Threshold voltage V_{Thn}	0.28 V
Channel doping $N_{ch}(cm^{-3})$	2×10^{16}
Fin-Height H_{fin}(nm)	50 nm
Body Thickness T_{Si}(nm)	8.6 nm

5. VARIABILITY ANALYSIS OF FINFET CURRENT MIRRORS

This section presents the mismatch and process variation study for the various configuration-based current mirrors.

5.1 Mismatch

We use a Design of Experiments (DOE)-based setup to understand the effect of mismatch on the FinFET-configuration current mirrors. A detailed discussion of DOE assisted method for process variation analysis is presented in [19]. A $\pm 30\%$ gate oxide thickness mismatch between the REF transistor (nominal value: T_{ox-REF} = 1.4 nm) and OUT (nominal value: T_{ox-OUT} = 1.4 nm) devices of the current mirror has been considered, with T_{ox-REF_L}= 1nm and T_{ox-OUT_L}= 1 nm as the low values, and T_{ox-REF_H} = 1.8 nm and T_{ox-OUT_H} = 1.8 nm as the high values. A 3 level-2 factors leads to 3^2=9 states in the design matrix (shown in Table 2). Algorithm 1 shows the detailed steps. The proposed algorithm affords designers an efficient process to understand the effects device and process parameters mismatch on device performance.

Algorithm 1 Mismatch in FinFET configuration current mirrors

Objective: Mismatch in SG, IG and LP configuration-based FinFET current mirrors.
Input Factors: T_{ox-REF}, T_{ox-OUT}.
Output Responses: Transfer ratio=$\frac{I_{OUT}}{I_{REF}}$, mismatch=$\frac{I_{OUT}-I_{REF}}{I_{REF}} \times 100\%$.
Setup experiment using 3 level-2 factors (3^2=9 states).
for each FinFET configuration **do**
    for each 1:9 state of experiment **do**
        Run simulation.
        Record $\frac{I_{OUT}}{I_{REF}}$, mismatch.
    end for
end for
Form regression-based mismatch models.

The mismatch is calculated as $\frac{I_{OUT}-I_{REF}}{I_{REF}} \times 100\%$. Table 2 presents the current transfer ratio=$\frac{I_{OUT}}{I_{REF}}$ and mismatch values for each of the configurations. Nominally, the point where V_{OUT}= V_{DS-REF}= V_{GS-REF} is where the transfer ratio $\frac{I_{OUT}}{I_{REF}}$=1, leading to a mismatch of 0%. We have not taken into consideration the mismatch between front (T_{oxf}) and back (T_{oxb}) gate oxide thicknesses within each device in this study and assume they are identical (T_{oxf}= T_{oxb}= T_{ox}) as the theme of this section is to study inter-device mismatch, and not intra-device mismatch.

To understand the behavior of configurations, we present the threshold voltage as a function of the back-gate voltage (V_{gb}) [10]:

$$\frac{\partial V_{Thn}}{\partial V_{gb}} = -\frac{\epsilon_{si} \times T_{ox}}{\epsilon_{si} \times T_{ox} + \epsilon_{ox} \times T_{si}}, \quad (1)$$

where $\frac{\partial V_{Thn}}{\partial V_{gb}}$ is called the back-gate effect. The negative sign in equation 1 implies that the direction of the threshold voltage change is opposite to that of the back-gate change. So, a negative back gate bias results in a threshold voltage shift towards a positive direction. We can also see that the back-gate effect becomes dominant as the gate oxide thickness increases. If the oxide thickness is reduced, the front surface potential is more dominantly controlled by the front gate than the back gate, and the back-gate effect becomes weaker. We can see from Table 2, that the mismatch is lowest when the oxide thicknesses are low, and the back-gate effect is minimized. Also, LP mode has highest mismatch, followed by IG and SG mode, where the back-gate effect is not present. Also, in the case of SG mode, the gate work function and the bias applied are the same for both gates. However, in the IG and LP modes, the gate work function is different for the 2 gates, giving rise to a flat-band voltage difference (ΔV_{fb}) [10]. This leads to the prediction that LP mode will suffer the highest mismatch followed by IG and SG mode.

Using the data in Table 2, we develop mismatch models for each configuration. Fig. 2(a), 2(b) and 2(c) show the surface fit for the data points in SG, IG and LP mode, respectively. Polynomials of the order 2 are developed for each configuration of the form: Mismatch (in %) = $p_{00} + p_{10} \times T_{ox-REF} + p_{01} \times T_{ox-OUT} + p_{20} \times T^2_{ox-REF} + p_{11} \times T_{ox-REF} \times T_{ox-OUT} + p_{02} \times T^2_{ox-OUT}$. The mismatch models are accurate with low values of RMSE $\approx$ 0.0614 and R^2 $\approx$ 0.999. The coefficient matrices for each DG-FinFET configurations are presented in the following equations:

$$p_{ij}(Mismatch_{SG}) = \begin{bmatrix} 0.01144 & -4.173 & -1.787 \\ 3.256 & -0.1163 & 0 \\ 1.488 & 0 & 0 \end{bmatrix} \quad (2)$$

$$p_{ij}(Mismatch_{IG}) = \begin{bmatrix} 0.011 & -5.328 & -1.203 \\ 4.385 & 0.004158 & 0 \\ 0.988 & 0 & 0 \end{bmatrix} \quad (3)$$

$$p_{ij}(Mismatch_{LP}) = \begin{bmatrix} 0.005834 & -11.4 & -0.7874 \\ 9.573 & 0.128 & 0 \\ 0.5752 & 0 & 0 \end{bmatrix} \quad (4)$$

Algorithm 2 Process variation in FinFET configuration current mirrors.

Objective: Coefficient of variation (c_v) in SG, IG and LP configuration-based FinFET current mirrors.
Input Factors: $\mathcal{N}(\mu_{T_{ox-REF}}, \sigma_{T_{ox-REF}})$, $\mathcal{N}(\mu_{T_{ox-OUT}}, \sigma_{T_{ox-OUT}})$.
Output Responses: $\mathcal{N}(\mu_{\frac{I_{OUT}}{I_{REF}}}, \sigma_{\frac{I_{OUT}}{I_{REF}}})$.
Setup Monte-Carlo experiment.
for each FinFET configuration **do**
    for each 1:1000 Monte-Carlo run **do**
        Run simulation.
        Record $\frac{I_{OUT}}{I_{REF}}$.
    end for
end for
Report $\mu_{\frac{I_{OUT}}{I_{REF}}}$, $\sigma_{\frac{I_{OUT}}{I_{REF}}}$ and $c_{v\frac{I_{OUT}}{I_{REF}}}$

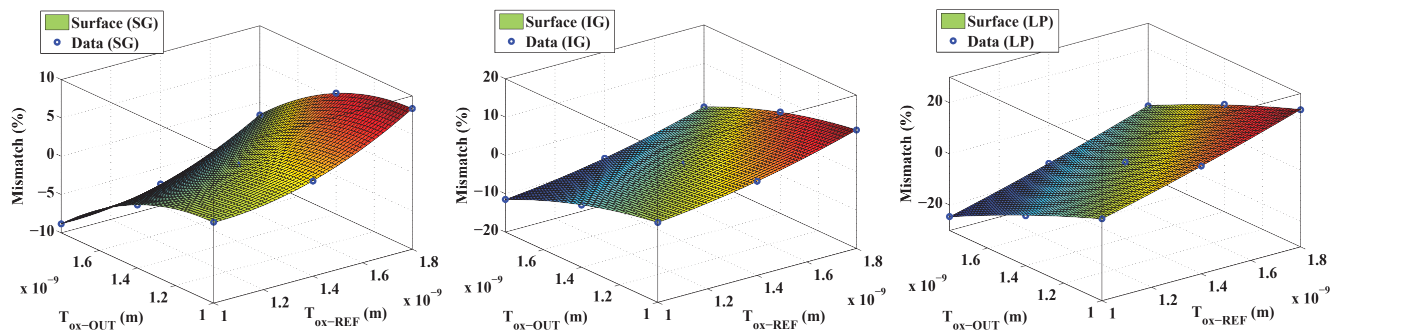
5.2 Process Variation

For process variation, we consider T_{ox-REF} and T_{ox-OUT} variations having a Gaussian (normal) distribution with mean (μ) values as specified in Table 1 and standard deviation (σ) as 10% of the mean. 1000 Monte Carlo simulations are performed. Algorithm 2 shows the steps.

Fig. 3(a), 3(b), 3(c) show the probability distribution function (PDFs) with Gaussian fit of the transfer ratio ($\frac{I_{OUT}}{I_{REF}}$) for SG, IG and LP modes, respectively. Table 3 shows the mean (μ), standard deviation (σ) and the coefficient of variation (c_v=$\frac{\sigma}{\mu} \times 100\%$) values for the configurations. We use the c_v value to compare the variability of the configurations as it shows the extent of variability in relation to mean of the population. Overall, it is observed that the LP mode shows the highest variability, followed by the IG mode and the SG mode. This trend is due to discrepancy of the work function between the two gates in the IG and LP modes of

Table 2: T_{ox} Mismatch effect on FinFET Configuration-based Current Mirrors

REF	OUT	$\frac{I_{OUT}}{I_{REF}}$(SG)	Mismatch(SG)	$\frac{I_{OUT}}{I_{REF}}$(IG)	Mismatch(IG)	$\frac{I_{OUT}}{I_{REF}}$(LP)	Mismatch(LP)
T_{ox-R_L}	T_{ox-OUT_L}	1.00555	+0.555%	1.00845	+0.845%	1.0208	+2.080%
T_{ox-REF}	T_{ox-OUT_L}	1.02402	+2.402%	1.04573	+4.573%	1.12182	+12.182%
T_{ox-REF_H}	T_{ox-OUT_L}	1.08352	+8.352%	1.10897	+10.897%	1.23643	+23.643%
T_{ox-REF_L}	T_{ox-OUT}	0.982087	-1.791%	0.962083	-3.792%	0.89517	-10.483%
T_{ox-REF}	T_{ox-OUT}	1	0%	1	0%	1	0%
T_{ox-REF_H}	T_{ox-OUT}	1.05793	+5.793%	1.06459	+6.459%	1.12034	+12.034%
T_{ox-REF_L}	T_{ox-OUT_H}	0.911764	-8.824%	0.88536	-11.464%	0.75459	-24.541%
T_{ox-REF}	T_{ox-OUT_H}	0.928658	-7.134%	0.922524	-7.748%	0.857361	-14.264%
T_{ox-REF_H}	T_{ox-OUT_H}	0.983526	-1.647%	0.986101	-1.390%	0.977039	-2.296%



(a) SG mode (b) IG mode (c) LP mode

Figure 2: Mismatch models for (a) SG mode, (b) IG mode and (c) LP mode FinFET current mirrors.

DG-FinFET, as discussed in Section 5.1. This difference in work function leads to a difference in the threshold voltage as [10]:

$$\Delta V_{Thn} = \frac{\epsilon_{si} \times T_{ox}}{\epsilon_{si} \times T_{ox} + \epsilon_{ox} \times T_{si}} \times \Delta V_{fb}. \quad (5)$$

According to Eqn. 5, the impact of the work function difference on the threshold voltage gets weaker as the gate oxide thickness reduces.

Table 3: Process variation statistical data for DG-FinFET current mirrors.

Mode	μ	σ	c_v(in %)
SG	1	0.0252	2.52
IG	1	0.0309	3.09
LP	1	0.0637	6.37

6. PERFORMANCE ANALYSIS OF DG-FINFET BASED CURRENT MIRRORS

This section discusses the FoMs such as output resistance (r_0) and compliance voltage (V_{CV}). The simulation setup used is the same as shown in Fig. 1, where V_{OUT} is varied from 0 to V_{DD} (1V), and I_{OUT} is recorded.

6.1 Output resistance (r_0)

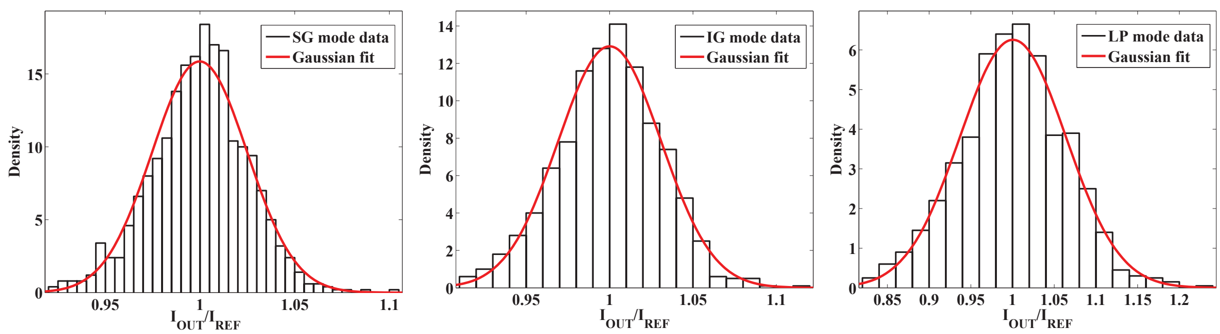
r_0 is measured by taking the reciprocal of the output current's derivative from I_{OUT}-V_{OUT} curves. Using the well known long-channel relationship: $r_0 \propto \frac{1}{I_{OUT}}$[2] (also used for understanding short channel behavior), we can understand the trend observed. As the best drive strength is offered by SG-mode [3], I_{OUT} increases at a faster rate with increasing V_{OUT}, we obtain the lowest r_0 for this configuration, followed by the IG and LP modes, where I_{OUT} reduces [3] compared to SG mode. Figure 4 shows the trend, and Table 4 shows the values of r_0 recorded at a biasing point of V_{OUT} = 0.4 V. As r_0 dominates the open circuit gain: $(g_m \times r_0) \propto \frac{1}{\sqrt{I_{OUT}}}$ [12], we can infer that the open circuit gain also follows the same trend as r_0 for the configuration-based current mirrors.

Table 4: r_0 for FinFET configuration-based current mirrors.

Configuration	r_0
SG mode	20.43 kΩ
IG mode	24.58 kΩ
LP mode	26.33 kΩ

6.2 Compliance Voltage (V_{CV})

The output compliance range for a current mirror is the range of output voltages where the current mirror behaves like a current



(a) SG mode (b) IG mode (c) LP mode

Figure 3: Distribution Functions for $\frac{I_{OUT}}{I_{REF}}$ for (a) SG mode, (b) IG mode and (c) LP mode FinFET current mirrors.

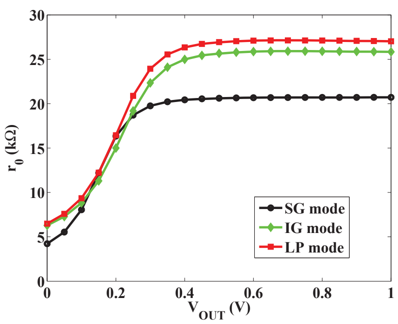


Figure 4: r_0 for FinFET configuration-based current mirrors.

source and not an open or a resistor. To keep the output transistor in saturation, V_{DG-OUT} = 0 V. Hence, the lowest output voltage that results in correct mirror behavior, the compliance voltage, is V_{OUT} = V_{CV} = V_{GS-OUT} = V_{DS-OUT} for the output transistor at the output current level with V_{DG-OUT} = 0 V. A lower value of V_{CV} is recommended as it leads to a higher compliance range. Figure 5 shows the intersection points where I_{OUT} = I_{REF}, and V_{CV} is recorded at these points. Table 5 shows the exact values. We can observe that SG mode offers the best (lowest) compliance voltage followed by IG and LP modes.

Table 5: V_{CV} for FinFET configurations based-current mirrors.

Configuration	V_{CV}
SG mode	0.359
IG mode	0.473
LP mode	0.528

This observation can be explained as follows: In FinFET, the effect of back-gate biasing is that the threshold voltage (V_{Thnf}) of the front-gate increases as the reverse-biasing (V_{gb}) of the back-gate increases [6]. The front-gate threshold voltage (V_{Thnf}) for the IG and LP mode is related to the back-gate voltage (V_{gb}) as [14]:

$$V_{Thnf(IG,LP)} = V_{Thn} - m \times V_{gb}, \tag{6}$$

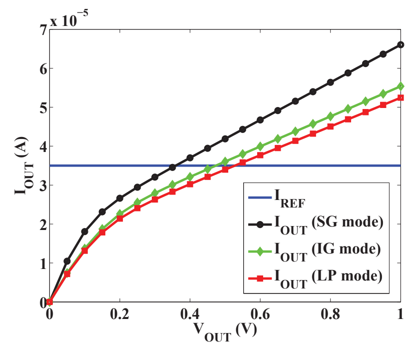


Figure 5: V_{CV} for FinFET configuration-based current mirrors

where m is the gate-to-gate coupling factor given by:

$$m = \frac{3 \times T_{oxf}}{3 \times T_{oxb} + T_{si}}, \tag{7}$$

where T_{oxf} and T_{oxb} are front and back gate oxide thicknesses, respectively. The threshold voltage of IG, LP modes is related to the SG mode configuration as:

$$V_{Thnf(IG,LP)} = (1 + m) \times V_{Thnf(SG)}. \tag{8}$$

It is evident that SG mode has the lowest V_{Thnf}, resulting in the lowest V_{CV} as it turns on faster than the IG and the LP mode and offers the largest compliance range. As the LP mode has the highest reverse bias (V_{gb}=-0.2V), it is the slowest giving rise to the largest V_{CV}, hence offering smallest compliance range.

7. CURRENT MIRROR DESIGN GUIDELINES USING DG FINFET

This section presents the guidelines for current mirror design using DG-FinFET configurations. The experimental results obtained in section 5.1 and Section 6 are used in the realization of the guidelines. Table 6 shows the design trade-offs between the three DG-FinFET configurations under consideration. There is a trade-off between the output resistance and the compliance voltage for current mirrors. The LP mode current mirror offers high gain (high

r_0) making it suitable for application in a common source amplifier. However, it has high variability and high V_{CV}. The SG mode current mirror offers low gain (r_0) making it suitable for use in a common drain amplifier for a voltage buffer. SG mode current mirror also offers the lowest variability and V_{CV}. The IG mode offers a compromise between the LP and SG mode with medium variability, r_0 and V_{CV}.

Table 6: Guidelines for current mirror design using FinFET configurations.

Variability	r_0	V_{CV}	Configuration
High	High	High	LP
Medium	Medium	Medium	IG
Low	Low	Low	SG

8. CONCLUSIONS

In this paper, we have studied current mirrors based on 3 configurations of the double gate FinFET device for analog circuit design. 2 novel algorithms are presented for measuring mismatch (using DOE and polynomial modeling) and variability in the double gate FinFET current mirrors. The future work will involve exploring advanced current mirror architectures such as cascode current mirror, regulated drain current mirror, supply independent biasing circuits using the various configurations studied in this paper. Mixed mode current mirrors may be proposed where certain devices are operated in the LP mode for high output resistance, and other devices in the SG mode for lower mismatch and higher compliance range.

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