Fast Statistical Process Variation Analysis using Universal Kriging Metamodeling: A PLL Example

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***Abstract*—The design of Analog Mixed-Signal Systems-on-Chip (AMS-SoCs) presents difficult challenges given the number of design specifications that must be met. This situation is more aggravating in the presence of process variation effects for nanoscale technologies. Existing statistical techniques heavily rely on Monte-Carlo analysis for design parameters in an effort to mitigate the effects of process variation. Such methods, while accurate are often expensive and require extensive amount of simulations. In this paper we present a geostatistical based metamodeling technique that can accurately take into account process variation and considerably reduces the amount of time for simulation. An illustration of the proposed technique is shown using a 180nm PLL design. The proposed technique achieves an accuracy of 0.7 % and 0.33% for power consumption and locking time, respectively, and improves the run time by about 10 times.**

***Keywords*-Geostatistics, Kriging, Universal Kriging, Analog mixed-signal (AMS), PLL, Nano-CMOS, Process Variations**

I. Introduction

Modern electronic designs have had analog content increasingly integrated with digital components making Analog/Mixed-Signal (AMS) designs ubiquitous. AMS designs however present numerous challenges to design engineers. Including familiar problems like efficient integration, electrical and physical reconciliation (EPR), designers also have to tackle the effects of process variation. As technology scales deep into nanometer dimensions, the effects of process variation have a dominating impact on performance behavior of circuits, with analog circuits being more prone to these effects [1], [2]. Due to systematic and random variations of design parameters, circuit designs rarely meet design specifications and the yield is reduced. It is then important to accommodate the effects of process variation early in the design flow to efficiently mitigate its impact.

Existing techniques for process aware designs heavily rely on Monte Carlo (MC) simulations and other statistical analysis methods to design for worst case scenarios. Research has been presented on such methods using MC and several variants [3], [4]. Monte Carlo analysis generates multiple simulations of the device while varying the design parameters such as transistor width, transistor length, thickness oxide, and threshold voltage with randomly generated parameter samples for analysis. The inherent problem of Monte Carlo analysis is the large number of simulation runs which can be very time consuming for very large circuits. For example, a single simulation of a large analog circuit on a CAD tool for a full blown parasitic netlist could take several days to complete. The ever reducing time-to-market makes this time cost infeasible. Different techniques have been explored to mitigate the time costs for analysis. These methods include hierarchical statistical analysis, symbolic and regression based techniques [5], [3]. Regression based techniques still require multiple simulations of the analog circuit for building the models. The device performance responses using sample points are used to build the model that can be further used for Monte Carlo Analysis. However, for analog designs in the deep nanometer regions, the error due to process variation is significantly correlated between design parameters, and regression based metamodels do not efficiently capture these effects and hence do not provide an accurate fit across the local and global design space [6].

This paper presents a geostatistical based metamodeling technique that uses *universal Kriging prediction* in building AMS design metamodels. Kriging prediction techniques were originally introduced and used in the geostatistics field for modelings [7], [8], [9] and recently in integrated circuit metamodeling [10], [11], [12]. The Kriging based performance prediction techniques use a combination of regression based methods that model the error correlation between design parameters and a stochastic component that aims to neutralize the deterministic nature of computer simulations. We propose Kriging based metamodels since they inherently provide a more statistically accurate analysis for process variation. A 180nm PLL design is also presented to demonstrate the efficiency of Kriging.

The rest of this paper is organized as follows: The universal Kriging metamodeling of the PLL is presented in Section II while the process variation aware analysis is presented in Section III. Experimental results are presented in Section IV and Section V contains conclusions and future research.

II. Geostatics Based Metamodeling of a PLL

In this section we present geostatistical based metamodeling that uses "Universal Kriging" for performance prediction. A brief overview of Kriging based metamodeling is given.

A. PLL:Case Study Circuit

The phase locked loop (PLL) which is a closed feedback loop circuit system is an ideal circuit for this study and is an excellent example of mixed-signal design. It is widely used in

many AMS-SoCs including processors, Field-Programmable Gate Arrays (FPGAs) and in telecommunication applications. The major components of the PLL are the phase detector, charge pump, voltage controlled oscillator (VCO) and frequency divider. A system diagram is shown in Fig. 1.

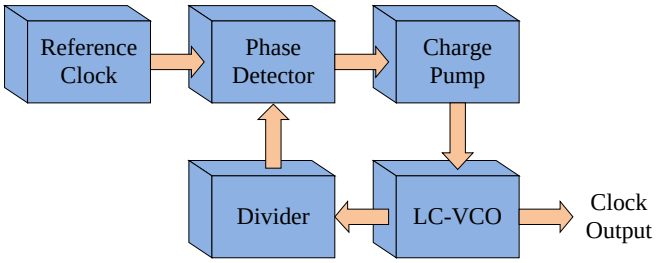


Fig. 1. High level system diagram of a PLL.

In a PLL, the phase detector detects the phase difference of the signals from the reference clock and closed loop. A difference in phase causes the charge pump to supply charge with proportion to error detected. The signal is filtered and used to control the VCO which produces the output phase to lock in with the reference clock. The divider is used to make the output signal a multiple of the reference clock where desired. The physical layout design of the baseline 180nm design is shown in Fig. 2.

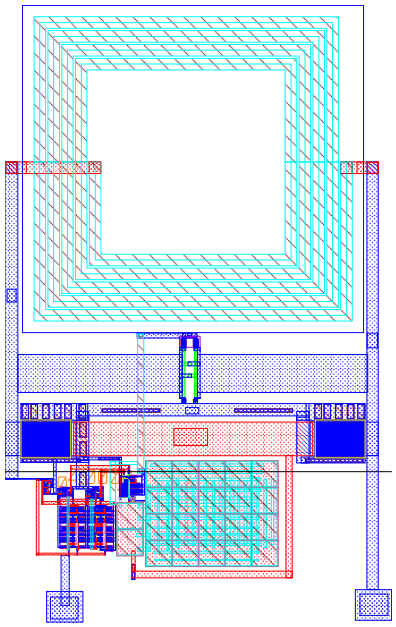


Fig. 2. Physical layout design of the 180nm PLL.

The PLL was characterized for power consumption, frequency output and locking time. The design objective is the minimization of power consumption using the locking time as optimization cost and 21 design parameters as variables.

B. Universal Kriging Based Metamodeling

Kriging techniques were originally used for geostatistical research and have been extended to other fields [7], [8], [9] and even VLSI design [10], [11], [12]. The application of Kriging for metamodeling was proposed in [13] as a combination of polynomial regression with a stochastic approach to mitigate the deterministic nature of computer experiments. The basic expression of Kriging is of the form:

$$y(\mathbf{x_0}) = \sum_{j=1}^{L} \lambda_j B_j(\mathbf{x}) + z(\mathbf{x}), \tag{1}$$

where $y(\mathbf{x_0})$ is a stochastic function which predicts the response at the design point $(\mathbf{x_0})$. $\{B_j(\mathbf{x}), j = 1, \cdots, L\}$ is a specific set of basic functions over the design domain D_N, λ_j are fitting coefficients (also known as weights) to be determined based on the Kriging method applied. $z(\mathbf{x})$ is a stochastic process with zero mean and based on a spatial correlation function. The weights, λ_j used in Kriging are a function of the correlation between the set of sampled data points to be used for prediction and the response points to be predicted. This feature ensures the weighting average of each predicted performance point is unique.

Kriging takes into account the autocorrelation between design parameters and is characterized by the covariance function [14]. The correlation function, usually called the *variogram*, is expressed as follows:

$$r(\mathbf{s}, \mathbf{t}) = \mathrm{Corr}(z(\mathbf{s}), z(\mathbf{t})). \tag{2}$$

The weights are chosen so that the Kriging variance is minimized [15], [7]. The weight selection technique can be varied to fine tune the result. Popular Kriging methods include the simple, ordinary and universal methods. Simple and ordinary Kriging assume a constant mean in the local domain of the predicted point, whereas universal Kriging method assumes the mean as a deterministic function. This work explores universal Kriging for the metamodeling of the PLL circuit.

Assuming there are n sampled points the of variable x, to predict a new point $y(x_0)$, the weights λ are estimated by the following:

$$\begin{pmatrix} \lambda_1 \\ \vdots \\ \lambda_n \\ \mu \end{pmatrix} = \Gamma^{-1} \begin{pmatrix} \gamma(x_1, x_0) \\ \vdots \\ \gamma(x_n, x_0) \\ 1 \end{pmatrix}, \tag{3}$$

Γ is the covariance matrix of the observed points and is given by the following expression:

$$\Gamma = \begin{pmatrix} \gamma(x_1, x_1) & \cdots & \gamma(x_1, x_n) & 1 \\ \vdots & \ddots & \vdots & 1 \\ \gamma(x_n, x_1) & \cdots & \gamma(x_n, x_n) & 1 \\ 1 & 1 & 1 & 0 \end{pmatrix}, \tag{4}$$

where the variogram is calculated as follows:

$$\gamma(x_1, x_2) = E\left(|z(x_1) - z(x_2)|^2\right). \tag{5}$$

The estimation of the variogram is obtained by fitting to some empirical autocorrelation functions. A few examples that are commonly used include the linear, exponential, Gaussian

and spherical models [13]. The Gaussian model is expressed as follows:

$$\gamma(h) = C_0 \left(1 - exp\left(-\frac{h^2}{r^2 a}\right)\right), \tag{6}$$

where C_0, C and a are shape parameters.

For the performance output of the power consumption of the PLL, which is analyzed in this work, the generated metamodel will be of the form:

$$\widehat{Z}(\mathbf{wn_0}) = \sum_{j=1}^{L} \lambda_j B_j(\mathbf{wn}) + z(\mathbf{wn}), \tag{7}$$

where $\widehat{P_{PLL}}(\mathbf{Wn_0})$ is the predicted power consumption at design point $\mathbf{Wn_0}$. The Kriging metamodel functions are generated using the MATLAB toolbox mGstat [16]. The sample points are generated using the Latin Hypercube Sampling (LHS) technique. LHS is more effective in capturing the entire design space thus improving the variance over Monte Carlo distributions [17]. A comparison of sampling techniques shows that metamodels generated using LHS techniques are more accurate than random sampling techniques.

III. Process Variation Aware Statistical Metamodel Generation

Conventional methods for process variation aware design analysis involve Monte Carlo simulations on the circuit design netlist for process variation verification. This process expends considerable time costs. The statistical method proposed involves running the statistical analysis on the Kriging metamodels instead. The Kriging metamodels have an advantage over similar methods using metamodels as they are more accurate and have a better efficiency of capturing the error correlation between design parameters thus making them more suitable for modeling the effects of process variation. The stochastic component of Kriging based techniques also compensates for the stochastic nature of computer simulations on which most design analysis are run on.

In creating the Kriging metamodel, the design parameters that are most sensitive to the performance outputs are used to ensure a robust model. The design parameters used were the transistor width and channel length of each component of the PLL. As technology scales deeper into the nanometer region, the transistor length also contributes to the threshold voltage variation. The transistor oxide thickness T_{ox} for both NMOS and PMOS transistors as well as the threshold voltage (V_{th}) are also included. In total, 21 design and process parameters were used for the device sampling. The parasitic netlist is parameterized to enable multiple simulations controlled by a scripting language.

For each performance output a different Kriging metamodel is generated. These process variation aware metamodels are then further used for statistical yield analysis. A comparison of the statistical analysis from the proposed model is compared to analysis from the extracted circuit netlist.

IV. Experimental Results

The 180nm PLL circuit described in section II-A was used for the experimental analysis of this work. The full blown RLCK parasitic netlist was extracted from the physical design layout and used for device sampling and simulation for silicon aware accuracy. A Monte Carlo analysis of 1000 simulation runs was performed for comparison to the statistical model proposed in this work. The Monte Carlo simulations were configured for process and mismatch variations. The physical design and Monte Carlo simulations were performed using the CADENCE Virtuoso environment. The performance outputs characterized are the power consumption (P_{PLL}), and the locking time ($Lock_{PLL}$). The process variation analysis is performed on the universal Kriging metamodel using MATLAB.

The results of the proposed statistical model are characterized by the histogram plots shown in Figure 3. The plots show the PDF for both the power consumption of the PLL and the locking time. The x-axis for Figure 3(a) shows the power and the y-axis shows the frequency of outputs. Similarly, Figure 3(b) shows the locking time and frequency of outputs respectively. The distribution for both plots is Gaussian as expected from the nature of random process variation modeled.

Table I shows the tabulated statistical analysis for the mean (μ) and standard deviation (σ) of the power consumption and locking time of the PLL in comparison to the values from the actual netlist. The mean value of the predicted power output is 0.871 mW compared to 0.877 from the actual netlist Monte Carlo analysis with a 0.7 % error. The predicted locking time is 3.23 μs compared to 3.24 μs with a 0.31 % error. The accuracy of these results validates the proposed statistical model which can be used for analysis while reducing the amount of time required for the conventional Monte Carlo analysis. This is a significant improvement of time costs for analysis. The simulation time for the Monte Carlo analysis on the actual netlist is about 5 days while the Kriging metamodel generation and analysis takes only a few hours.

To demonstrate the improvement of Kriging over behavioral modeling used for analysis, the results from selected works are compared to this work in Table II.

V. Conclusion

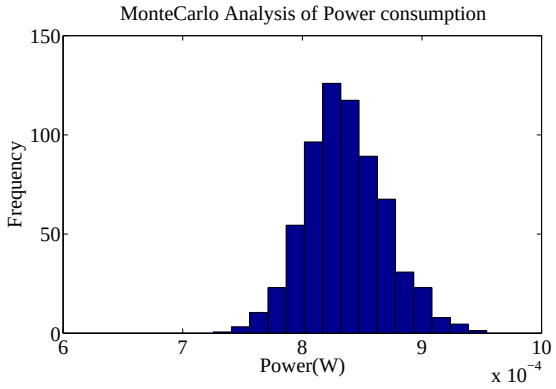
This paper presented a Kriging based statistical model for process variation aware analysis of analog mixed signal circuit designs. The proposed model with the inherent characteristic of Kriging prediction techniques takes into account the correlation between design parameters in process variation. Simulation and analysis results shows that the model compares well to conventional but time exhausting Monte Carlo methods. It achieves a mean error of 0.7 % and 0.33 % for the statistical analysis of the power consumption and locking time compared to the Monte Carlo control but speeds up the simulation process by approximately 10 times. This proves that the proposed method minimizes the statistical error while improving the simulation time considerably.

TABLE I
STATISTICAL ANALYSIS FOR ACCURACY OF KRIGING GENERATED METAMODEL FOR PLL POWER CONSUMPTION

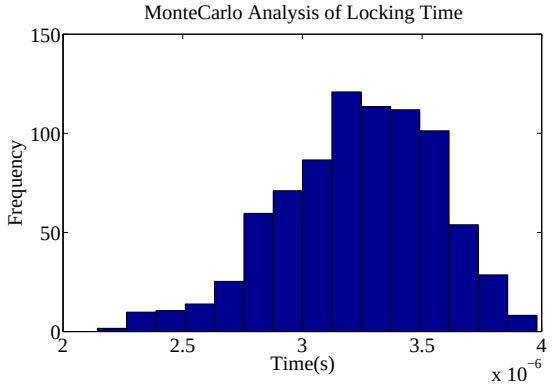
	Mean (μ)			Standard Deviation (σ)		
	Circuit	Kriging	Error	Circuit	Kriging	Error
P_{PLL}	0.877 mW	0.871 mW	0.7 %	0.073 mW	0.072 mW	1.4 %
$Lock_{PLL}$	3.24 μs	3.23 μs	0.31 %	1.07 μs	0.33 μs	69.16 %

TABLE II
STATISTICAL ANALYSIS FOR ACCURACY OF KRIGING GENERATED METAMODEL FOR PLL POWER CONSUMPTION

Research	Technique	Power		Locking Time	
		Mean	Error	Mean	Error
[3]	Quasi-SA	-	-	3.45	2.2 %
[18]	ANN	0.90 mW	0.14 %	3.22 μs	0.7 %
[This Paper]	Kriging	0.87 mW	0.7 %	3.23 μs	0.33 %



(a) Power dissipation



(b) Locking time

Fig. 3. Statistical analysis of the performance output for the 180nm PLL using Kriging metamodels.

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