Double Gate FinFET based Mixed-Signal Design: A VCO Case Study

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***Abstract*— This paper investigates mixed-signal design for double-gate (DG) FinFET technology using a current-starved voltage controlled oscillator (VCO) as a case study. Design issues of the DG FinFET-based VCO is presented in a comparative perspective with a classical CMOS VCO. The DG FinFET VCO is analyzed for the figures-of-merit like center frequency, frequency-voltage (f-v) characteristics. Statistical process variation analysis is presented to study the variability in DG FinFET VCO. Models are investigated for the f-v characteristics and width quantization-aware modeling has been presented for the FinFET-based VCO. The models can be used for fast design optimization. To the best of the authors' knowledge, this is the first paper that examines DG FinFET technology with for circuit-level mixed signal design while presenting a comparative between classical CMOS and DG FinFET technologies.**

I. Introduction

Aggressive scaling of CMOS technology continues to meet the power, speed and packaging density requirements of state of art integrated circuits. The use of conventional planar single gate MOSFETs is becoming extremely difficult due to enhanced Short-Channel Effects (SCEs) [1]. In addition to SCEs, planar MOSFETs suffer from random dopant fluctuations (RDF) in the channel area, which is believed to be the main source of threshold voltage mismatch among the devices, fabricated on the same wafer [2]. Process variation in FinFETS due to Random dopant fluctuations (RDF) are reduced due to undoped or lightly doped body and reduced carrier mobility degradation [3]. Various structures of the DG-FinFETs are the promising candidates for the replacement of conventional single gate planar MOSFETs due to their higher immunity to SCEs [4]. In 2012, Intel has started using FinFETs for its future commercial devices [5].

Fabrication of FinFETs is compatible with that of conventional CMOS, thus making possible very rapid deployment to manufacturing. The major advantages of FinFET include the following: (1) Nearly ideal subthreshold slope. (2) Small intrinsic gate capacitance. (3) Smaller junction capacitances. (4) Better immunity to SCEs. (5) Higher $\left(\frac{I_{ON}}{I_{OFF}}\right)$ ratio. (6) Design flexibility at circuit level with shorted gate (SG) and independent gate (IG) options.

Memory design and digital design with FinFETs has been explored quite exhaustively [4], [6], [7]. Use of FinFET for analog design has been relatively less explored. In analog design, the FinFET has also been used at the device level [8]. Research is required at the circuit level as well, for example, the width-quantization property in FinFETs causes the gate sizing in FinFETs to be treated as a discrete variable [2]. This paper presents study at circuit level. In order to study the impact of FinFETs on mixed-signal circuit design, we have chosen a VCO for this study.

The *novel contributions* of this paper are as follows:

1) A FinFET-based VCO design is performed and simulated for 45nm technology node.
2) Models of frequency-voltage characteristics are developed for nano-CMOS VCO and FinFET-based VCO.
3) A fast surface model for width quantization-aware optimization using design of experiments (DOE) is presented for the FinFET VCO which can be used optimization.
4) The VCO is characterized for center frequency, frequency-voltage characteristics, and process variation. Qualitative and quantitative discussions are presented.

II. Design of Current-Starved DG FinFET VCO

The shorted-gate (SG) n-type FinFET structure is shown in Fig. 1. The FinFET device has been configured in the SG mode where the front and back gates are tied together. The body thickness (T_{Si}) of a single fin equals to silicon channel thickness. The current flows from the source to drain along the wafer plan. Each fin provides $2 \times H_{fin}$ of device width, where H_{fin} is the height of the each fin. For the FinFET devices, widths are quantized into units of the fins. Large width of device can be obtained by using multiple fins [9].

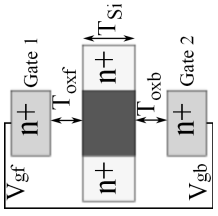


Fig. 1. Shorted Gate (SG) Double-Gate n-type FinFET.

The bottom of a FinFET structure sits on top of a layer of SiO_2 and the FinFET is inherently an silicon-on-insulator (SOI) transistor. Furthermore, in the typical FinFET process range, the SOI thickness (T_{si}) is so thin that the silicon body is fully depleted. Hence, the fully depleted SOI model of BSIM (BSIM FD SOI) is used as the model basis for each sub-transistor. An equivalent sub-circuit approach is adopted

in this paper for the DG FinFET device modeling [10]. The model consists of two fully depleted SOI devices for the front and back transistors, respectively. BSIM SOI is used as the model for each device making this sub-circuit compatible with standard circuit simulators, like SPICE. Two single-gate transistors have been used to capture the current conduction controlled by the front and back gate in a FinFET transistor [3]. Each sub-transistor has its own definitions of gate voltage (V_g), threshold voltage (V_{Th}), and gate-oxide thickness (T_{ox}). The key parameter values for bulk CMOS and DG FinFET models at 45nm node are shown in Table I.

TABLE I
45NM BULK CMOS AND FINFET DEVICE PARAMETER VALUES.

Parameter	Bulk CMOS	DG FinFET
Oxide Thickness T_{ox}(nm)	1.4nm	1.5nm
Threshold voltage V_{Th}	V_{Thn} = 0.22V, V_{Thp}= -0.22V	V_{Thn}=0.31V, V_{Thp}=-0.25V
Channel doping $N_{ch}(cm^{-3})$	2.8 $\times$ 10^{18}	2 $\times$ 10^{16}
Fin-Height H_{fin}(nm)	–	50nm
Body Thickness T_{Si}(nm)	–	8.4nm

The circuit diagram of a DG FinFET based current-starved VCO using is shown in Fig. 2. The nominal sizes are shown for a 45nm technology node. The supply voltage (V_{DD}) is kept at 1 V. An inverter is formed by the devices PM1 (FP1) and NM1 (FN1). The current sources are formed by PM2 (FP2) and N2 (FN2), which limit the current available to the inverter, hence starving the inverter for current. The tuning voltage (V_{tune}) sets the drain currents in the devices PM11 (FP11) and NM11 (FN11), which form the input stage. The currents in PM11 (FP11) and NM11 (FN11) are mirrored in each inverter or current source stage.

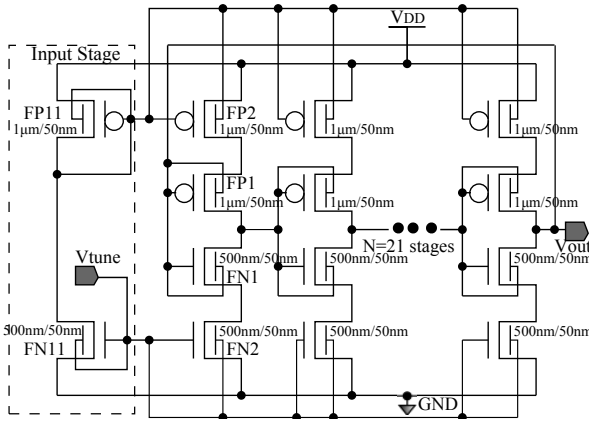


Fig. 2. A 45 nm Shorted Doubled Gate FinFET based VCO design.

The oscillation frequency (aka center frequency) of a current-starved VCO when V_{tune}=$\frac{V_{DD}}{2}$ is expressed by:

$$\text{Freq}_{VCO} = I_D / \left(n \times C_t \times V_{DD}\right). \quad (1)$$

Where I_D is drain current, n is number of stages, C_t is total capacitance on the drains of PM1 and NM1, and V_{DD} is supply voltage. We have designed 21-stage oscillator; thus n = 21, I_D=10μA and C_t=4.7 fF for a target frequency of 100 MHz. We have C_t=C_{tot} times the area of the device. For a CMOS device, C_{tot}=C_{ox} (gate-oxide capacitance of the device). For a DG FinFET based device, C_{tot} is calculated as the series combination of three terms as follows:

$$\frac{1}{C_{tot}} = \frac{1}{C_{Si}} + \frac{1}{C_{gate}} + \frac{1}{C_{ox}}. \quad (2)$$

Where C_{Si} is the capacitance to the carriers in the channel, C_{gate} is the depletion capacitance of the gate electrode. This leads to smaller intrinsic gate capacitance in FinFET, resulting in higher oscillation frequency. A center frequency of 775.6 MHz has been observed for the FinFET VCO. The overall characterization is presented in Table II. Where pwr_{FinFET} is the power consumption, k_v is the vco gain, $freq_{FinFET}$-minimum and $freq_{FinFET}$-maximum are the minimum and maximum frequencies.

TABLE II
DG FINFET VCO CHARACTERIZATION.

Parameter	Value
$freq_{FinFET}$	775.6 MHz
pwr_{FinFET}	65.4μW
k_v	2.331 GHz/V
$freq_{FinFET}$-minimum	363.2 MHz
$freq_{FinFET}$-maximum	1.165 GHz
V_{tune}	0 to 1V

III. MODELING F-V CHARACTERISTICS OF VCO

The f-v characteristics are plotted for both bulk CMOS and DG FinFET VCO. Fig. 3 shows the tuning curves. We now present models for f-v characteristics which can be used for VCO optimization or optimization of larger systems such as phase-locked loop (PLL) which uses such a VCO.

For the nano-CMOS VCO, the characteristic is shown in Fig. 3. The best-fit curve is obtained of the following form:

$$freq_{CMOS}(V_{tune}) = a_0 e^{-\left(\frac{V_{tune}-b_0}{c_0}\right)^2} + a_1 e^{-\left(\frac{V_{tune}-b_1}{c_1}\right)^2} \quad (3)$$

Where a_0= 4.126 $\times$ 10^8, b_0= 1.368, c_0= 1.351, a_1= 2.059 $\times$ 10^8, b_1= -0.1483, c_1= 0.8269. The goodness-of-fit of the model is evaluated using Root of Mean Square Error (RMSE) and coefficient of determination (R^2).

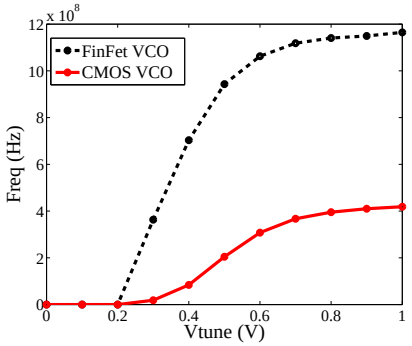


Fig. 3. The f-v Characteristics of DG FinFET and Bulk MOSFET VCOs.

The RMSE estimates the error between the simulation data and propose model which is of the following form:

$$RMSE = \sqrt{\frac{1}{N}\sum_{i=0}^{N}(freq(V_{tune}^i) - \widehat{freq(V_{tune}^i)})^2}. \quad (4)$$

Where N is the number of measurements. $freq(V_{tune}^i)$ and $\widehat{freq(V_{tune}^i)}$ are the frequency responses at point V_{tune}^i of

the tuning voltage (V_{tune}) data observations and the proposed model, respectively. A smaller RMSE value indicates an accurate model. We report an RMSE of 8.369 MHz for the nano-CMOS f-v characteristics model. R^2 measures the proportion of the variation of the tuning voltage data observations around the mean that is explained by the fitted regression model. Advantage of using R^2 is that its scale is intuitive, and an improvement in the model results in proportional increase in R^2. The closer R^2 is to 1, the greater the degree of association between variables V_{tune} and the response. The following expression is used for measuring R^2:

$$R^2 = 1 - \frac{\sum_{i=0}^{N}(freq(V_{tune}^i) - \widehat{freq(V_{tune}^i)})^2}{\sum_{i=0}^{N}(freq(V_{tune}^i) - \overline{freq(V_{tune}^i)})^2}. \quad (5)$$

Where $\overline{freq(V_{tune}^i)}$ is the mean of the response at point (V_{tune}^i) of the tuning voltage data observations. We report an R^2 value of 0.9992 for the CMOS f-v characteristics model.

For the FinFET VCO, a cubic (3rd order) polynomial is chosen as best-fit which is of the following form:

$$freq_{FinFET}(V_{tune}) = p_0 + p_1 V_{tune} + p_2 V_{tune}^2 + p_3 V_{tune}^3. \quad (6)$$

Where p_0= 1.1 $\times$ 10^9, p_1= 1.426 $\times$ 10^8, p_2= -1.646 $\times$ 10^8 , p_3 = 6.802 $\times$ 10^7. The fitness of the model is evaluated using RMSE and R^2 using the formula provided in Eqn. 4 and 5. An RMSE=6.098 MHz and R^2=0.9997 is observed for the DG FinFET based VCO f-v characteristics model.

IV. Width Quantization-Aware Modeling of DG FinFET based VCO

For a DG FinFET, each fin provides device width of 2 $\times$ H_{fin} of device width. The size of each fin determines the increments in device widths available to the circuit designer and multiple fins are required to obtain large widths in a device. In this paper, for the DG FinFET, each fin provides a width of 100nm. So, the FinFET VCO has N_{fin}=10 fins (W = 2 $\times$ H_{fin} $\times$ N_{fin}=1μm). In classical CMOS, the transistor widths are treated as continuous variables which are subjected to continuous optimization techniques [3]. However, in FinFETs the width can only be increased in increments of N_{fin} making it a discrete optimization problem.

We present a width quantization-aware model relating the device geometry to the center frequency $freq_{FinFET}$ of the DG FinFET VCO. This model can be used for DG FinFET based fast optimization of VCO and PLL. We use a Design of Experiments (DOE) based full-factorial run for data sampling. A regression based model of the order 2 has the form:

$$freq_{FinFET} = 2H_{fin} \sum_{i,j=0}^{2} p_{ij} N_{fin-n}^i N_{fin-p}^j. \quad (7)$$

Where p_{ij} is the matrix of coefficients obtained from regression, N_{fin-n} is the number of fins in the n-type FinFET, and N_{fin-p} is the number of fins in the p-type FinFET. As the number of fins can only take an integer value, this becomes a discrete model. Fig. 4 shows the corresponding surface plot. The following coefficient matrix is obtained:

$$p_{ij}(freq_{FinFET}) = \begin{bmatrix} 7.9 \times 10^8 & -2.5 \times 10^7 & -8.9 \times 10^6 \\ 1.3 \times 10^8 & 1.4 \times 10^7 & 0 \\ -4.9 \times 10^7 & 0 & 0 \end{bmatrix} \quad (8)$$

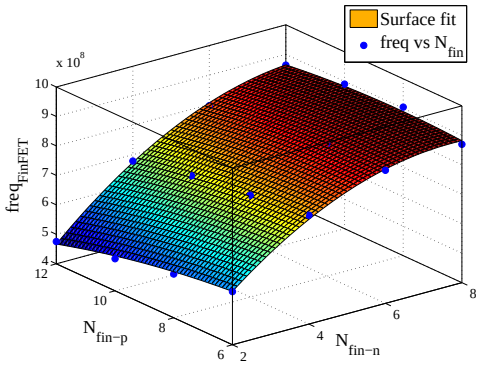


Fig. 4. Surface plot relating oscillation frequency to number of fins.

We again use the RMSE and R^2 to report the goodness-of-fit of the quantization-aware frequency model. For DG FinFET VCO, the RMSE has the following form:

$$RMSE = \sqrt{\frac{1}{M \times N}\sum_{i=0}^{M}\sum_{j=0}^{N}(freq(N_{fin-n}^i, N_{fin-p}^j) - \widehat{freq(N_{fin-n}^i, N_{fin-p}^j)})^2}. \quad (9)$$

Where M $\times$ N are the data points of the N_{fin-n} and N_{fin-p} parameters selected in the design domain. $freq(N_{fin-n}^i, N_{fin-p}^j)$ and $\widehat{freq(N_{fin-n}^i, N_{fin-p}^j)}$ are the frequency responses at points (N_{fin-n}^i, N_{fin-p}^j) of the data point observations and the regression based model, respectively. We report an RMSE of 10.9 MHz for the model. For DG FinFET based VCO, the R^2 is calculated as follows:

$$R^2 = 1 - \frac{\sum_{i=0}^{M}\sum_{j=0}^{N}(freq(N_{fin-n}^i, N_{fin-p}^j) - \widehat{freq(N_{fin-n}^i, N_{fin-p}^j)})^2}{\sum_{i=0}^{M}\sum_{j=0}^{N}(freq(N_{fin-n}^i, N_{fin-p}^j) - \overline{freq(N_{fin-n}^i, N_{fin-p}^j)})^2}. \quad (10)$$

Where $\overline{freq(N_{fin-n}^i, N_{fin-p}^j)}$ is the mean of the response at points (N_{fin-n}^i, N_{fin-p}^j) of the data point observations. We report an R^2 value of 0.9942 for the model.

V. Statistical Process Variation Analysis of VCO

The process variation in nanoscale manufacturing processes has been a main concern for designer as it affects the device parameters and overall affects the yield. The key device parameter, threshold voltage standard deviation (σV_{Th}) is affected by gate oxide thickness (T_{ox}), channel dopant concentration (N_{ch}), and channel length (L) and width (W) [11]:

$$\sigma V_{Th} = \left(\frac{\sqrt[4]{4q^3\epsilon_{Si}\phi_B}}{2}\right)\left(\frac{T_{ox}}{\epsilon_{ox}}\right)\left(\frac{\sqrt[4]{N_{ch}}}{\sqrt{W \times L}}\right). \quad (11)$$

Where ϕ_B = 2 $\times \kappa_B \times T \times \ln(N_{ch}/n_i)$, with κ_B Boltzmann's constant, T the absolute temperature, n_i the intrinsic carrier concentration, q the elementary charge), and ϵ_{ox} and ϵ_{Si} are the permittivity of oxide and silicon, respectively. The above expression is consistent with observations that σV_{Th} is inversely proportional to the square root of the device area. As the variations in device geometry and doping profile parameters can be translated into the effective variation in threshold voltage [12]. The threshold voltage fluctuation is considered as the major source of process variation when the performance impacts of the parameter fluctuations are

investigated. We consider V_{Th} variations having a Gaussian distribution with mean values as specified in Table I and standard deviation (σV_{Th}) as 10% of the mean, assuming the same range of parameter variation for bulk CMOS and FinFET devices. We performed Monte Carlo simulations of 500 run. Fig. 5(a) and 5(c) show the probability distribution function (PDFs) of the center frequency for the VCOs. Fig. 5(b) and 5(d) present the cumulative distribution function (CDFs). It is observed that the distributions follow a Gaussian (normal) trend. The chi-square goodness of fit has also been performed within 5% significance level, which satisfies the *null hypothesis* that the $freq_{CMOS}$ and $freq_{FinFET}$ follow a Gaussian distribution. The chi-square test statistic is given by the following expression:

$$\chi^2 = \sum_{i=1}^{N} \frac{(O(freq)_i - E(freq)_i)^2}{E(freq)_i}. \quad (12)$$

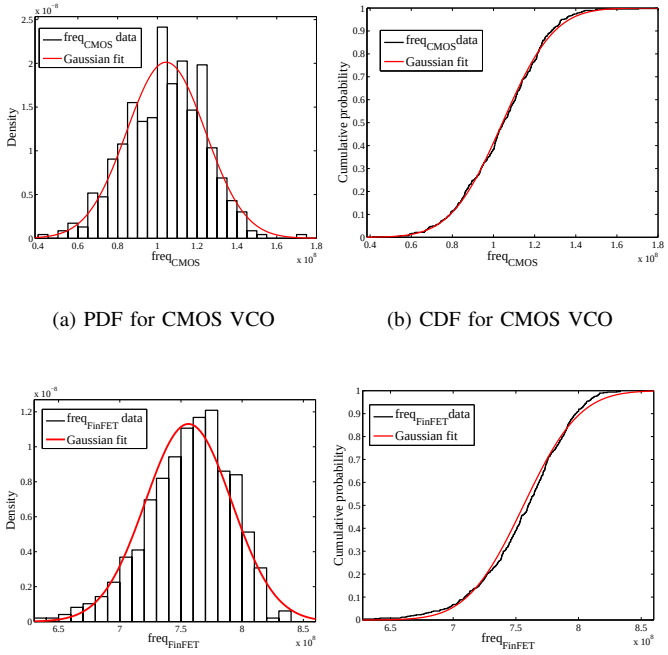
Where $O(freq)_i$ are the observed counts and $E(freq)_i$ are the expected counts. For comparison of CMOS VCO with FinFET VCO in context of process variation, we present the coefficient of variation (c_v). The coefficient of variation c_v is defined as the ratio of the standard deviation σ to the mean μ. c_v shows the extent of variability in relation to mean of the population. Hence, a low c_v indicates a higher process variation tolerance. From the values obtained in Table III, it is observed that the *DG FinFET VCO shows a 4.66% variability, as opposed to 18.98% variability in the classical CMOS VCO*. The Bulk CMOS VCO design is more vulnerable to process variation than the DG FinFET VCO design.

TABLE III
PROCESS VARIATION DATA FOR CMOS AND DG FINFET VCO.

Measurement	μ	σ	$c_v = \left(\frac{\sigma}{\mu}\right)$
$freq_{CMOS}$	104.37 MHz	19.812 MHz	0.1898
$freq_{FinFET}$	756.14 MHz	35.272 MHz	0.0466

VI. CONCLUSIONS

This paper explores DG FinFET based for mixed signal design at with a current-starved VCO as a case study. We have drawn a comparison between classical CMOS and DG FinFET based VCO, for this purpose. The FoMs considered include center frequency, f-v characteristics and nanoscale process variation. The DG FinFET VCO has a 7× higher center frequency due to smaller intrinsic gate capacitance. Fast and accurate models have been presented for f-v characteristics of CMOS and FinFET VCO. It is observed that while a gaussian fit is most suitable for modeling the f-v characteristics of CMOS VCO, a cubic polynomial is well-fitted for the FinFET counterpart. From the process variation analysis, we observe that the FinFET VCO shows 4.66% variability due to V_{Th} fluctuations, as compared to 18.98% variability in the CMOS VCO, making it more process variation tolerant. A width quantization-aware model for a FinFET VCO is also presented. As part of future research, thermal effects will be examined, as FinFETs suffer from self-heating. Width quantization-aware models for power consumption will be developed, and a discrete multiobjective optimization will be performed using FinFET based mixed signal circuits.



(a) PDF for CMOS VCO (b) CDF for CMOS VCO

(c) PDF for FinFET VCO (d) CDF for FinFET VCO

Fig. 5. Statistical Distribution functions for CMOS and FinFET VCO

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