Comparative Analysis of Double Gate FinFET Configurations for Analog Circuit Design

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***Abstract*— FinFETs are being adopted as an alternative to nanoscale classical MOSFET for digital circuits. The double-gate (DG) FinFET gives rise to a rich design space using various configurations of the gates. Existing research study the DG FinFET for digital design. However, the effectiveness of the various DG FinFET configurations for the analog design has not received much attention. In this paper, we compare the DG FinFET parameters including transconductance (g_m), output resistance (r_0), open-circuit gain ($g_m \times r_0$), transition frequency (f_T) including the most important issue, "nanoscale variability", which are important for analog design. The following three configurations for a fully depleted SOI DG FinFET are analyzed: shorted-gate, independent-gate, and low-power, for both strong inversion and subthreshold operations. Using the results obtained, we present guidelines for DG FinFET based analog design.**

I. Introduction and Contributions

Nanoscale bulk CMOS technology suffers from various short channel effects (SCEs), threshold voltage fluctuations, and process variations. One of the new devices being explored is the FinFET technology, due to its higher immunity to SCEs and process variation [2], [3]. FinFETs have advantages like a higher $\left(\frac{I_{ON}}{I_{OFF}}\right)$ ratio (very important for digital circuits) and smaller intrinsic gate capacitances and design flexibility at with multiple gates. For a double-gate FinFET, three configurations are identified: shorted-gate (SG) mode with transistor gates tied together, low-power (LP) mode where the back-gate is tied to a reverse-bias voltage to reduce leakage power, and independent gate (IG) mode where independent signals are used to drive the two device gates. The question is how good is each of the DG FinFET configurations for analog designs.

The digital circuits are the main workhorse in the consumer electronics in which, devices are built for a high $\left(\frac{I_{ON}}{I_{OFF}}\right)$ ratio. The digital chips utilize FinFET devices are in production [1]. However, for analog designs, a high $\left(\frac{I_{ON}}{I_{OFF}}\right)$ ratio, may not lead to best performance. The design trade-offs for analog circuit design are more complicated than those for digital. If instead of bulk CMOS, the FinFET will be used, the device architecture will change, and more interpretation time will be required for optimal circuits to be designed.

The FinFET based digital circuits are being explored [4], [5]. In [6], a FinFET-based SRAM is optimized using back-gate voltage tuning. In [7], FinFET is optimized for low-voltage analog design. In [8], the analog performance of DG and Tri-Gate FinFET are compared. In [9], the analog/RF performance of FinFET are compared with bulk CMOS. However, there is no comparison between the various configurations of the FinFET device for analog applications.

This paper is an effort in the direction of exploring the FinFET technology for analog circuit design. The *novel contributions* of this paper can be summarized as follows:

1) A comparative analysis among the configurations of the FinFET device is presented for analog circuit design.
2) Output resistance, Transconductance, Open-circuit gain, transition frequency are analyzed in both strong inversion and subthreshold regions.
3) Statistical process variation analysis is presented for the above FinFET parameters in both strong inversion and subthreshold regions of DG FinFET operation.
4) Design guidelines are formed for the analog circuit designer working with FinFET configurations.

II. DG FinFET: Model and Configurations

The FinFET is inherently an SOI transistor. The body thickness (T_{Si}) of a fin is analogous to silicon channel thickness. Fig. 1 shows the shorted-gate (SG), independent-gate (IG) and Low-Power (LP) structures of a n-type FinFET. V_{gf} is the potential difference between the front gate and source. V_{gb} denotes the potential difference between the back gate and the source. In the SG mode, the front and back gates are tied together. In the IG mode, the top part of the gate is etched out for two independent gates [7]. The LP-mode applies a reverse-bias voltage to the back-gate in order to reduce subthreshold leakage. SG mode has smallest delay, followed by IG and LP mode [2]. For power consumption, LP mode gives the lowest power consumption, followed by IG and SG mode. Digital design mainly deal with with delay and power.

In the typical FinFET process, the SOI thickness (T_{si}) is so thin that the silicon body is fully depleted. Two single-gate transistors have been used to capture the current conduction controlled by the front and back gate in a DG FinFET transistor [3]. Each sub-transistor has its own definitions of gate voltage (V_g), threshold voltage (V_{Th}), and gate-oxide thickness (T_{ox}). The fully depleted SOI model of BSIM (BSIM FD SOI) is used for each sub-transistor. The key parameters for the FinFET model for 32nm node are shown in Table I. For brevity, results for a n-type DG FinFET device is presented while dual trends are observed for p-type.

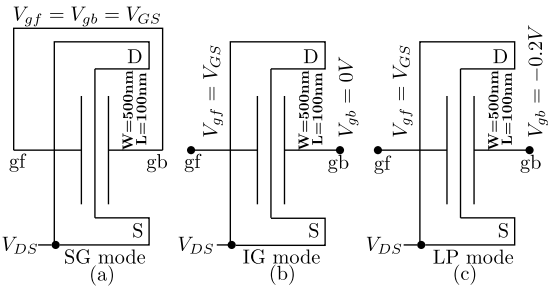


Fig. 1. Configurations for n-type Double Gate FinFET studied in this paper.

TABLE I

PARAMETER VALUES OF A 32NM N-TYPE DG FINFET DEVICE.

Parameter	Value
Oxide Thickness T_{ox}(nm)	1.4nm
Threshold voltage V_{Thn}	0.28V
Channel doping $N_{ch}(cm^{-3})$	2×10^{16}
Fin-Height H_{fin}(nm)	50nm
Body Thickness T_{Si}(nm)	8.6nm

III. DG FINFET PARAMETERS FROM THE ANALOG CIRCUIT DESIGN PERSPECTIVE

A. Analyzing DG FinFET in Strong Inversion Region

For a good matching, a nominal size of L = 100 nm and W = 500 nm is assumed. For strong inversion region, V_{GS} is set to 0.35 V and overdrive voltage V_{ov} = V_{GS}-V_{Thn} = 70 mV.

1) Transconductance (g_m): g_m is plotted against V_{GS} in Fig. 2. Table II shows the g_m values for a V_{GS} of 0.35 V (V_{ov} 70 mV). In FinFET, the effect of back-gate biasing is that the threshold voltage of the front-gate (V_{Thnf}) increases as the reverse-biasing (V_{gb}) of the back-gate increases [6]. V_{Thnf} is related to the V_{gb} as follows for IG and LP [10]:

$$V_{Thnf(IG,LP)} = V_{Thn} - r \times V_{gb}. \quad (1)$$

Where r is gate-to-gate coupling factor: $r = \left(\frac{3 \times T_{oxf}}{3 \times T_{oxb} + T_{si}}\right)$. T_{oxf} and T_{oxb} are front and back gate oxide thicknesses. V_{Th} of IG or LP modes is related to the SG mode as:

$$V_{Thnf(IG,LP)} = (1 + r) \times V_{Thnf(SG)}. \quad (2)$$

It is clear from Eqn. 2, that SG mode has the lowest V_{Thnf}, resulting in the largest g_m as it turns on faster with V_{GS} than the IG and the LP mode. As the LP mode has the highest reverse bias (V_{gb}=-0.2V), it is the slowest with the smallest g_m. g_m changes with V_{GS}, as the saturation velocity does not remain constant, and depends on both V_{GS} and V_{DS}. The trend can also be explained using the behavior: $g_m \propto \sqrt{I_D}$.

2) Output Resistance (r_0): r_0 is measured from the inverse of the slope from I_D-V_{DS} curves. FinFET does not follow square-law and has a much higher $\left(\frac{I_{ON}}{I_{OFF}}\right)$ ratio. As FinFETs offer the best drive strength in SG-mode [2], I_D increases at a faster rate with increasing V_{DS} and we obtain the lowest r_0 for this configuration $\left(r_0 \propto \frac{1}{I_D}\right)$, followed by the IG and LP modes, where I_{ON} reduces by almost 60% compared to SG mode [2]. Fig. 3(a) shows the trend, and Table II shows the values of r_0 recorded at a biasing point of V_{DS}=0.4V.

3) Open-Circuit Gain ($g_m \times r_0$): As $g_m \propto \sqrt{I_D}$, and $r_0 \propto \left(\frac{1}{I_D}\right)$, we can say that $(g_m \times r_0) \propto \left(\frac{1}{\sqrt{I_D}}\right)$. Since the LP mode has the weakest drive current, it offers the highest gain. This is followed by the IG and SG mode (Table II).

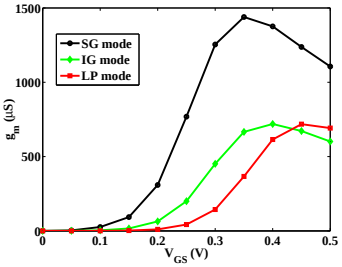
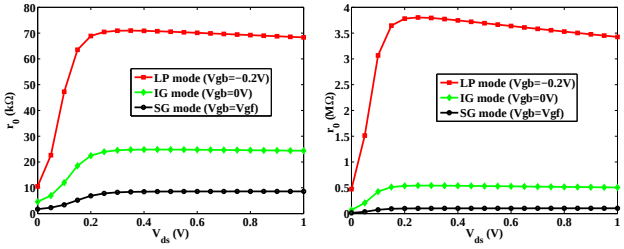


Fig. 2. g_m trend in strong inversion and subthreshold.



(a) Strong inversion (b) Subthreshold

Fig. 3. r_0 trend in strong inversion and subthreshold in DG FinFET.

TABLE II

OPEN CIRCUIT GAIN IN STRONG INVERSION OF DG FINFET.

Configuration	g_m	r_0	$g_m \times r_0$
SG mode	1.4391 mS	8.49 kΩ	12.22
IG mode	666.07 μS	24.83 kΩ	16.54
LP mode	366.5 μS	70.88 kΩ	25.98

4) Transition Frequency (f_T): f_T is the frequency at which the device transitions from an amplifier to an attenuator. A high f_T value indicates a high speed. f_T for short-channel devices is generally expressed as follows:

$$f_T = \frac{g_m}{2 \times \pi \times C_{gs}}. \quad (3)$$

Where C_{gs} is gate to source capacitance. From subsection III-A.1, we can infer that $g_m \propto \left(\frac{1}{V_{Thnf}}\right)$. This, along with Eqn. 3 ($f_T \propto g_m$) helps us understand the trends in Fig. 4(a), and the values presented in Table III. So, SG mode offers highest speed, followed by IG and LP modes, respectively.

TABLE III

f_T IN STRONG INVERSION OF DG FINFET.

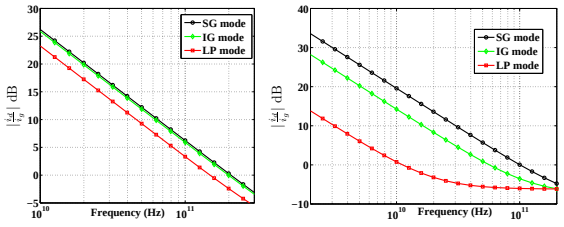
Configuration	f_T
SG mode	208.1 GHz
IG mode	200.6 GHz
LP mode	149.9 GHz

B. Analyzing DG FinFET in Subthreshold Region

For subthreshold region, we set V_{GS}=0.2V (V_{Thn}=0.28V). Following is the subthreshold current in a DG FinFET [13]:

$$I_{sub} = \alpha \times \frac{H}{L} \times e^{\left(\frac{V_{GS} - V_{Thnf}}{\beta}\right)} \times \left(1 - e^{\left(\frac{-q \times V_{DS}}{k \times T}\right)}\right). \quad (4)$$

Where k is Boltzmann constant, T is the temperature in Kelvin, and α and β are fitting parameters. Diffusion is mainly responsible for current transport in the subthreshold region, as opposed to drift in the strong inversion region.



(a) Strong inversion (b) Subthreshold

Fig. 4. f_T trend in strong inversion and subthreshold of DG FinFET.

1) Transconductance (g_m): g_m in the subthreshold region for the various configurations shows the same trend as in the strong inversion region. As shown in Fig. 2 for subthreshold region, only the readings are taken at V_{GS}=0.2V, with SG mode having highest g_m followed by IG and LP modes. However, the relative values of g_m as compared to the strong inversion region are lesser (Table IV). This can be explained using $g_m \propto \sqrt{I_D}$. As the I_D would be close to I_{OFF} in the subthreshold region, a decrease in the g_m value is expected.

2) Output Resistance (r_0): As $r_0 \propto \left(\frac{1}{I_D}\right)$, and I_D begins to fall in the subthreshold region, we see relatively larger r_0 as compared to strong inversion (Table IV). The trend, however, stays the same as in strong inversion (Fig. 3(b)).

3) Open-circuit gain ($g_m \times r_0$): Using $(g_m \times r_0) \propto \left(\frac{1}{\sqrt{I_D}}\right)$, we get relatively larger open-circuit gain in subthreshold region as compared to strong inversion. The trend stays the same, with LP mode having the highest gain, IG mode having medium gain and SG mode having the lowest gain (Table IV).

TABLE IV

OPEN CIRCUIT GAIN IN SUBTHRESHOLD REGION OF DG FINFET.

Configuration	g_m	r_0	$g_m \times r_0$
SG mode	309 μS	101.66 kΩ	31.41
IG mode	63.9 μS	538.78 kΩ	34.43
LP mode	12.4 μS	3.7466 MΩ	46.45

4) Transition Frequency (f_T): As g_m is smaller in subthreshold region, f_T in subthreshold region is smaller than the strong inversion (Table V). Also C_{gs} in the subthreshold region is smaller in strong inversion region. The trend is the same, with LP being the slowest and SG the fastest (Fig. 4(b)).

TABLE V

f_T IN SUBTHRESHOLD REGION OF DG FINFET.

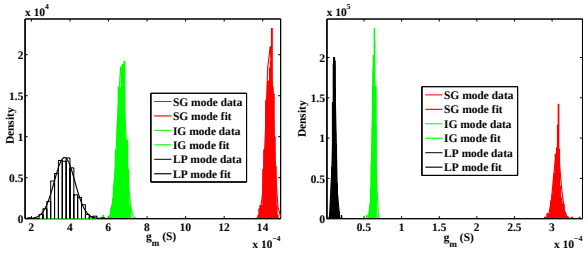
Configuration	f_T
SG mode	100.78 GHz
IG mode	57.65 GHz
LP mode	11.34 GHz

IV. PROCESS VARIATION ANALYSIS OF DG FINFET

A. Process Variation Analysis during Strong Inversion Region

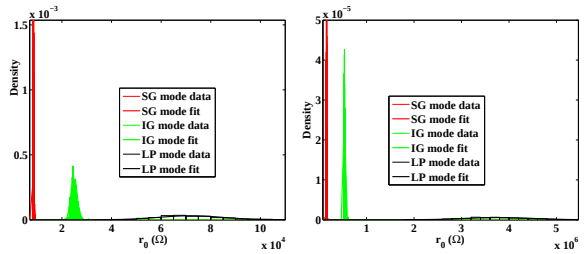
Threshold voltage fluctuations are considered as the major source of process variation when the performance impacts of the parameter fluctuations are investigated. In the IG and LP mode, the threshold voltage can be expressed as a function of the back-gate voltage (V_{gb}) [11]:

$$\frac{\partial V_{Thn}}{\partial V_{gb}} = -\frac{\epsilon_{si} \times T_{ox}}{\epsilon_{si} \times T_{ox} + \epsilon_{ox} \times T_{si}}. \quad (5)$$



(a) Strong inversion (b) Subthreshold

Fig. 5. g_m variability in strong inversion and subthreshold.



(a) Strong inversion (b) Subthreshold

Fig. 6. r_0 variability in strong inversion and subthreshold.

Where $\left(\frac{\partial V_{Thn}}{\partial V_{gb}}\right)$ is called the back-gate effect. The negative sign in Eqn. 5 implies that the direction of the threshold voltage change is opposite to that of the back-gate change. So, a negative back gate bias results in a threshold voltage shift towards a positive direction. We can also observe that the back-gate effect becomes dominant as the body thickness decreases or the gate oxide thickness increases. If the oxide thickness is reduced, the front surface potential is more dominantly controlled by the front gate than the back gate, and the back-gate effect becomes weaker. For process variation, we consider T_{oxf} and T_{oxb} variations having a Gaussian distribution with mean (μ) values as specified in Table I and σ as 10 % of the μ. Monte Carlo simulations are performed for 500 run. Fig. 5(a), 6(a), 7(a) show the statistical distributions with Gaussian fit of the g_m, r_0 and f_T in strong inversion region. Table VI shows μ, σ, and coefficient of variation (c_v) values for the 3 modes. We use the c_v value to compare the variability of the configurations [12]. Overall, it is observed that the LP mode has the highest variability, followed by the IG mode and the SG mode. The f_T variability for all 3 modes is comparable. The reason for this is that in the case of SG mode, the gate work function and the bias applied are the same for both gates. However, in the IG and LP modes, the gate work function is different for the 2 gates, giving rise to a flatband voltage difference (ΔV_{fb}) [11]. Thus *IG, LP modes will be affected more severely by process variations than the SG mode.*

B. Process Variation Analysis during Subthreshold Region

Fig. 5(b), 6(b), 7(b) show the statistical distributions with Gaussian fit of the g_m, r_0 and f_T for the subthreshold region. The monte-carlo setup is the same as for strong inversion, except the n-type DG FinFET is biased at V_{GS}=0.2V. The c_v values in Table VII show that the SG mode has highest process variation tolerance, followed by IG and LP modes. This trend

TABLE VI

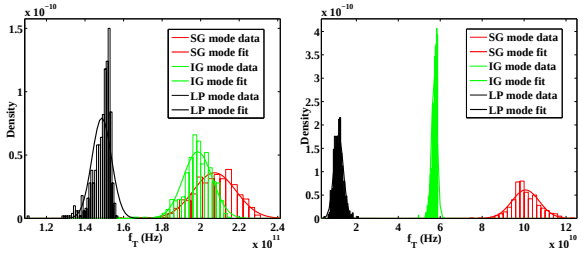
IMPACT OF PROCESS VARIATION DURING STRONG INVERSION REGION OPERATION OF DG FINFET.

Configuration	g_m			r_0			f_T		
	μ	σ	$c_v=\frac{\sigma}{\mu}\%$	μ	σ	$c_v=\frac{\sigma}{\mu}\%$	μ	σ	$c_v=\frac{\sigma}{\mu}\%$
SG mode	1.436 mS	18.71 μS	1.30	8.51 kΩ	177.79Ω	2.08	207.23 GHz	11.06 GHz	5.33
IG mode	666.66 μS	21.14 μS	3.17	24.91 kΩ	1.17kΩ	4.69	198.46 GHz	7.58 GHz	3.82
LP mode	371.96 μS	53.24 μS	14.31	72.08 kΩ	13.54kΩ	18.78	148.68 GHz	5.03 GHz	3.38

TABLE VII

IMPACT OF PROCESS VARIATION DURING SUBTHRESHOLD REGION OPERATION OF DG FINFET.

Configuration	g_m			r_0			f_T		
	μ	σ	$c_v=\frac{\sigma}{\mu}\%$	μ	σ	$c_v=\frac{\sigma}{\mu}\%$	μ	σ	$c_v=\frac{\sigma}{\mu}\%$
SG mode	306.65μS	4.72μS	1.53	105.68 kΩ	1.99 kΩ	1.88	100.68 GHz	6.53 GHz	6.49
IG mode	62.91μS	1.91μS	3.04	541.07 kΩ	11.64 kΩ	2.15	57.21 GHz	1.22 GHz	2.13
LP mode	11.52μS	2.06μS	17.88	3.79 MΩ	736.47 kΩ	19.43	11.51 GHz	2.16 GHz	18.77



(a) Strong inversion (b) Subthreshold

Fig. 7. f_T variability in strong inversion and subthreshold.

originates from the discrepancy of the work function between the two gates in the IG and LP mode. This difference in work function leads to a difference in the threshold voltage, as evident from the following [11]:

$$\Delta V_{Thn} = \frac{\epsilon_{si} \times T_{ox}}{\epsilon_{si} \times T_{ox} + \epsilon_{ox} \times T_{si}} \times \Delta V_{fb}. \quad (6)$$

The impact of the work function difference on the threshold voltage becomes weaker as the gate oxide thickness is reduced.

V. GUIDELINES FOR FINFET BASED ANALOG DESIGN

Based on the results from previous Sections, we develop certain guidelines for the analog designer working with the DG FinFET and efficient utilization of the device. Table VIII shows the design options available. For example, if the designer wishes to obtain a high gain, but can work with lower speeds, he/she may operate all the devices in that particular circuit in a LP configuration in the subthreshold region. This configuration, however comes with a high process variability. The IG mode offers a compromise between the LP and SG mode with medium gain, speed and variability. If the regions of operation are compared, a higher gain is achieved in the subthreshold region as compared to the strong inversion region, but at the cost of a lower speed and higher variability. Moreover, a mixed mode analog circuit may be explored where certain devices are operated in the LP mode to obtain high gain, and the other devices may be operated in the SG mode in order to get high speed and low variability. This will give rise to a much richer design space, and a new class of analog circuits.

VI. CONCLUSIONS AND FUTURE RESEARCH

In this paper, we have studied various configurations of the FinFET device for it use in analog circuit design. The trade-offs have been discussed, and logical explanation provided for the trends observed. Both the strong inversion and subthreshold region of operation have been compared. The future work will involve designing state-of-the-art analog circuits like bandgap references, op-amps and comparators using a blend of the various configurations studied in this paper.

TABLE VIII

GUIDELINES FOR ANALOG DESIGN USING DG FINFET CONFIGURATIONS.

Region	Gain	Speed	Variability	Configuration
Subthreshold	High	Low	High	LP
Subthreshold	Medium	Medium	Medium	IG
Subthreshold	Low	High	Low	SG
Strong inversion	High	Low	High	LP
Strong inversion	Medium	Medium	Medium	IG
Strong inversion	Low	High	Low	SG

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