Fast Analog Design Optimization using Regression based Modeling and Genetic Algorithm: A Nano-CMOS VCO Case Study

Dhruva Ghai[1], Saraju P. Mohanty[2] and Garima Thakral[3].
Department of Electronics and Communication Engineering, Oriental University, Indore.[1]
NanoSystem Design Laboratory, Dept. of Computer Science and Engineering, University of North Texas, USA.[2]
Department of Computer Science, Oriental University, Indore.[3]
Email-ID: dhruvaghai@orientaluniversity.in[1], saraju.mohanty@unt.edu[2],
and garimathakral@oriental.ac.in[3].

***Abstract*— The mature electronic design automation (EDA) tools and well-defined abstraction-levels for digital circuits have almost automated the digital design process. However, analog circuit design and optimization is still not automated. Custom design of analog circuits and slow analog in SPICE has always needed maximum efforts, skills, design cycle time. This paper presents a novel design flow for constrained optimization of nano-CMOS analog circuits. The proposed analog design flow combines polynomial-regression based models and genetic algorithm for fast optimization. For evaluating the effectiveness of the proposed design flow, power minimization in a 50nm CMOS based current-starved voltage-controlled oscillator (VCO) is carried out, while treating oscillation frequency as a performance constraint. Accurate polynomial-regression based models are developed for power and frequency of the VCO. The goodness-of-fit of the models is evaluated using SSE, $RMSE$ and R^2. Using these models, we form a constrained optimization problem which is solved using genetic algorithm. The flow achieved 21.67% power savings, with a constraint of frequency $\geq$ 100 MHz. To the best of the authors' knowledge, this is the first study which approaches a VCO design problem as a mathematical constrained optimization involving the usage of regression based modeling and genetic algorithm.**

I. Introduction and contributions

Digital design exploration and optimization has been largely automated due to availability of large number of electronic design automation (EDA) or computer-aided design (CAD) tools. This is also aided by the availability of well-defined abstractions for digital circuits (such as system, architecture, and logic levels). However, automatic design optimization of analog circuits is still a difficult and time intensive process [1]. For example, the analog simulation time for a nano-CMOS phase-locked loop is a matter of several days. So, debugging such a design is time intensive and costly. This results in high-cost and longer design cycle time. If such analog design are performed at nano-CMOS technology, the issues are further complicated and result in yield loss.

Modern analog integrated circuit (IC) optimization problems are highly complicated and involve minimizing a cost function subject to certain constraints. Multivariant technique is implemented to understand constrained optimization in this research. In most analog design situations, a designer must make trade-offs between conflicting behavioral requirements, dealing with functions that are often non-linear [2], such as power consumption and frequency of a VCO [3]. Circuit designers need novel design/optimization flows [4]. Optimizing two or more design objectives while subjecting design variables or performance metrics to constraints is the aim of multi-objective optimization [5], [6]. The trade-offs and sensitivity analysis between the different objectives can be explored by multi-objective optimization. During optimization, the baseline circuit is iteratively tuned by adjusting a large number of design parameters to vast amounts of different design possibilities of the same circuit to meet the target design functions. This makes it very tedious to do exhaustive design space exploration for complex nano-CMOS circuits. Further, this situation is aggravated by the use of compact SPICE models [7] with hundreds of parameters in nano-CMOS technology. Multiobjective optimization problems [8], [9] can be found wherever optimal decisions need to be taken in the presence of trade-offs between two or more conflicting objectives.

Polynomial regression model is an abstracted model of the netlist which enables a fast design space search [10], [11]. Authors have explored support vector machines (SVM)-based regression modeling in [12]. Polynomial regression models are useful for relative functions to unknown and very complex nonlinear relationship. This model is a mathematical predictive equation which may be used as a substitute for the actual circuit, leading to easier and faster simulations with multiple iterations during optimization. Hence, it can be used as an alternative to the exhaustive search of the actual circuits design space. The model can also be used in a variety of tools, such as MATLAB, and is language independent and can be used in a flexible fashion.

The *novel contributions* of this paper are as follows:

1) A novel fast design flow for multiobjective constrained optimization in nano-CMOS analog circuits is proposed. The speed up in design flow is achieved by the use of polynomial regression models and genetic algorithm based optimization.

2) A method for polynomial regression based modeling has been proposed for analog circuits. The goodness-of-fit of the polynomial regression models is measured using SSE, $RMSE$ and R^2.
3) A genetic algorithm based optimization approach is presented that considers power consumption as objective and frequency as constraint for a VCO design.
4) A 50 nm CMOS based current starved VCO is subjected to the proposed design methodology. We report 21.67% power savings and frequency $\geq$ 100 MHz in the VCO.

The notations and definitions for various terminologies used in this paper are given in Table I. To give an overview, the paper is organized in following manner: Section II discusses the proposed flow. The design of the VCO and regression based models are discussed in section III. Section IV highlights the formation and solution of the constrained optimization step of the flow using genetic algorithm. This is followed by conclusions and future research in section V.

TABLE I
NOTATION AND ACRONYMS USED IN THIS PAPER

V_{DD}	: supply voltage of nano-CMOS circuit
V_{in}	: input voltage to nano-CMOS circuit
V_{out}	: output voltage to nano-CMOS circuit
W_p	: width of the PMOS transistor
W_n	: width of the NMOS transistor
Power$_{VCO}$	: power consumption of VCO
Frequency$_{VCO}$	: frequency of VCO
$g(x)$	: cost function
$h(x)$	: non-linear inequality constraint
SSE	: Sum of squared error
RMSE	: Root of Mean Square Error
R^2	: Coefficient of Determination
GA	: Genetic Algorithm

II. PROPOSED DESIGN OPTIMIZATION FLOW FOR NANO-CMOS VCO

This section presents the proposed flow for constrained optimization in nano-CMOS based analog circuits. Although, a VCO is used as an example circuit in this case study for reducing power consumption, and increasing frequency, the optimization flow can be generalized for other nano-CMOS analog circuits (like operational amplifiers, filters, sense amplifiers, etc.) as well.

The input to the proposed design flow is a baseline design of circuit. This is one time manual design step. At this stage a netlist is sufficient for the design flow. For a schematic design this netlist will have only active devices whereas for a layout design full-blown parasitics (RCLK) is included. In this paper, we have used a 50 nm CMOS based VCO. A baseline design is carried out as per the specifications. The design objectives and constraints are identified and measured for this baseline VCO (power and frequency). In order to collect data for building the regression-based models, exhaustive simulations are performed to obtain the sample data points in the space defined by the bounded design variables. For this study, we consider 2 design variables i.e. W_p: width of the PMOS

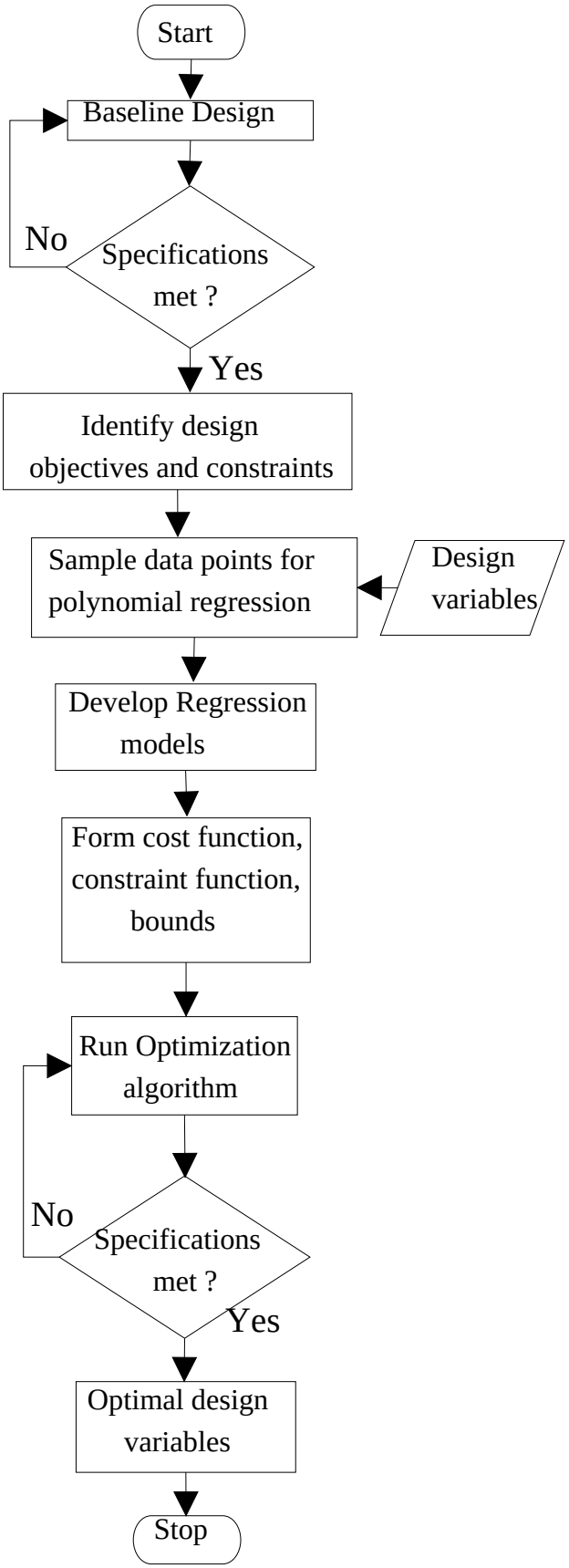

Fig. 1. Proposed optimization flow.

transistors, and W_n: width of the NMOS transistors in the current starved VCO. Thereafter, a polynomial regression based model is developed for each design objective (i.e. power and frequency) using these sample data points. Polynomial regression is efficient, reliable and allows for very fast design exploration [13] in a smaller design space (like 2 design variables in this paper). But it is not efficient for very high dimensional circuits (many parameters) due to the number of coefficients limited by memory space. Other modeling techniques, like pareto surfaces [14] also suffer from the curse of dimensionality. In order to accommodate a larger design space with a higher number of variables, we may use techniques such as neural networks [15], support vector machines based regression [12], kriging [16] in the proposed design flow instead of polynomial regression.

At this stage of the design flow, the analog circuit design problem is formulated as a constrained optimization problem. For an example the following:

$$\begin{aligned} \underset{x}{\text{minimize}} \quad & g(x) \\ \text{subject to} \quad & h(x) \leq 0, \\ & X_L < x < X_H. \end{aligned} \tag{1}$$

Where $g(x)$ is the cost function to be minimized and the vector $h(x)$ is the non-linear inequality constraint. Vector x corresponds to the design variable set (x= $[W_n, W_p]^T$), and X_L and X_H are their lower and upper bounds, respectively. $g(x)$ and $h(x)$ are formed using the models, which are developed in the regression step of the flow. We have considered power of the VCO as the design objective and frequency of the VCO as the design constraint. However, other VCO specifications like phase noise and tuning linearity may also be considered in the set of design objectives: $g(x)$ or design constraints: $h(x)$. Cost function, constraints and bounds are formed for design variables which are the inputs to the optimization algorithm. This constrained optimization formulation is then fed to the optimization algorithm.

A number of global optimization algorithms are available in current literature for optimization of analog circuits, i.e. genetic algorithm [8], simulated annealing [16], particle-swarm optimization [17], bee-colony optimization [18]. These algorithms are particularly effective in finding global optimal or near-optimal solutions, as compared to local optimization techniques like conjugate-gradient [19] and derivative-based methods [13]. Convex Optimization has been explored in [20] where circuit designs are expressed as posynomial models. We have used the genetic algorithm (GA) to solve our optimization problem, as it is easily transferred to existing simulations and models. Also, GA can handle arbitrary constraints and objectives unlike other commonly used optimization methodologies. The output of the algorithm is the optimal values of the design variables. The circuit is then re-simulated using these design variable values for obtaining the design objectives. For example, power and frequency for the VCO.

III. Design and Modeling of $50nm$ current-starved VCO

The circuit diagram for baseline 50nm current-starved VCO is shown in figure 2. The supply voltage (V_{DD}) has been kept at 1 V. An inverter is formed by the devices P1 and N1. The current sources, formed by P2 and N2, limit the current available to the inverter (P1 and N1). So, the inverter is starved for current. The input voltage sets the drain currents in the devices P11 and N11. The currents in P11 and N11 are mirrored in each inverter/current source stage.

The oscillation frequency of the current-starved VCO is given by equation 2 [6].

$$\text{Frequency}_{VCO} = \frac{I_D}{n \times C_{tot} \times V_{DD}}. \tag{2}$$

Where I_D=drain current, n=number of stages, C_{tot}=total capacitance on the drains of P1 and N1, and V_{DD}=supply voltage. We have chosen n=21, I_D=10μA and C_{tot}=4.7 fF for a target frequency of 100 MHz. The average power consumption by the VCO is given by the following expression:

$$\begin{aligned} \text{Power}_{VCO} &= P_{\text{dynamic}} + P_{\text{subthreshold}} + P_{\text{gate-oxide}} \qquad (3) \\ &= nC_{tot}V_{DD}^2\text{Frequency}_{VCO} \\ &\quad + C\exp\left(\frac{V_{gs}-V_{Th}}{Sv_{therm}}\right)\left(1-\exp\left(\frac{-V_{ds}}{v_{therm}}\right)\right) \\ &\quad + \alpha WL\left(\frac{V_{ox}}{T_{ox}}\right)^2 \exp\left(\frac{-\beta\left(1-\left(1-\frac{V_{ox}}{\phi_{ox}}\right)^{\frac{3}{2}}\right)}{\left(\frac{V_{ox}}{T_{ox}}\right)}\right) \qquad (4) \end{aligned}$$

Where $C = \left(\mu_0 \times \left(\frac{\epsilon_{ox}W}{T_{ox}L_{eff}}\right) \times v_{therm}^2 \times e^{1.8}\right)$, T_{ox} is the oxide thickness, ϕ_{ox} is the barrier height for the tunneling particle (hole or electron), and α and β are physical parameters used in modeling.

For developing models for Power$_{VCO}$ and Frequency$_{VCO}$ as function of the design variable set x=$[W_p, W_n]^T$, a quadratic polynomial regression (order=2) is applied. The polynomial regression model is expressed as follows:

$$f(x) = \sum_{i,j=0}^{2} p_{ij} \times x(1)^i \times x(2)^j. \tag{5}$$

Where $x(1)$=W_n, $x(2)$=W_p, $f(x)$ may be $freq$ or pwr and p_{ij} is the matrix of coefficients obtained by polynomial regression.

A. Polynomial Regression Modeling of VCO Power

The design space is explored through parametric simulations for the values of W_n and W_p ranging from the lower bounded constraint (100nm) to upper bounded constraint (1μm) and the data points are used to obtain least squares fit polynomial as in equation (5). The coefficient matrix obtained as in equation 6. Figure 3 shows the corresponding surface plot.

$$p_{ij}(pwr) = \begin{bmatrix} 5.4\times10^{-5} & 6.8\times10^{-6} & -1.3\times10^{-6} \\ 6.6\times10^{-6} & 2.7\times10^{-6} & 0 \\ -1.2\times10^{-6} & 0 & 0 \end{bmatrix} \tag{6}$$

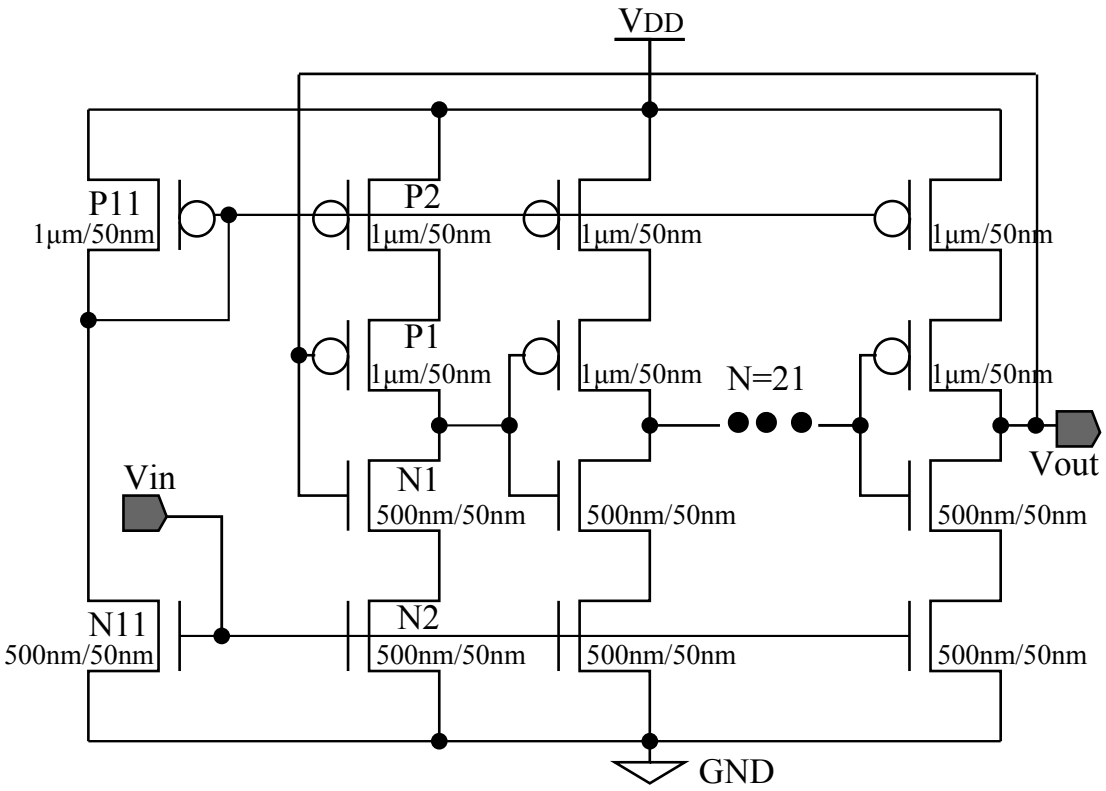

Fig. 2. Logical diagram for VCO with transistor sizes for 50 nm CMOS based baseline design.

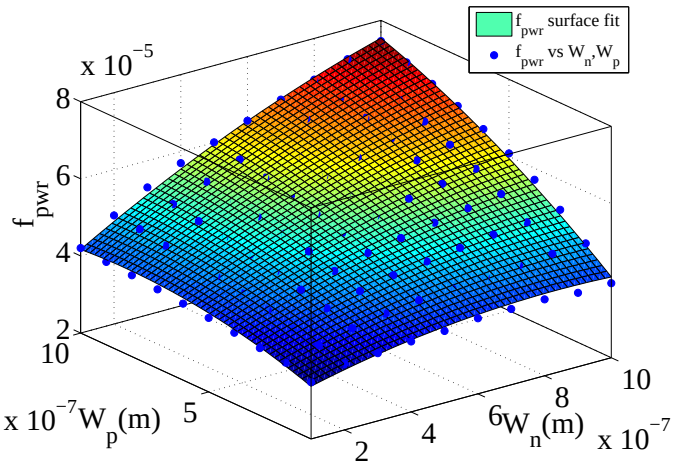

Fig. 3. Surface plot for power consumption of VCO.

We analyze the sum of squared error (SSE), Root of Mean Square Error (RMSE) and coefficient of determination (R^2) [11] as measures of goodness of fit for the polynomial regression model. SSE is a measure of the discrepancy between the data and an estimation model. If the estimation model is well fitted, it results in predictive data values close to observed values. A small SSE indicates a tight fit of the model to the data. Equation 7 shows the formula used for calculating SSE.

$$SSE = \sum_{i=0}^{N} (f(x_i) - \widehat{f(x_i)})^2. \tag{7}$$

Where N=1000 are uniformly distributed points of the parameters selected in the design domain (x). We report an SSE of 56.55pW. $f(x_i)$ and $\widehat{f(x_i)}$ are the responses at point (x_i) of the data point observations and the regression based model, respectively. One way to calculate RMSE is obtained by substituting equation 7 in equation 8. Alternatively, RMSE is shown in equation 9.

$$RMSE = \sqrt{\frac{SSE}{N}} \tag{8}$$

$$= \sqrt{\frac{1}{N} \sum_{i=0}^{N} (f(x_i) - \widehat{f(x_i)})^2}. \tag{9}$$

The RMSE estimates the difference between the observed data points from simulations and the polynomial regression model. A smaller RMSE value indicates an accurate polynomial regression model [11]. We report an RMSE of 0.2378μW for the power model.

The coefficient of determination (R^2) measures the proportion of the variation of the data point observations around the mean that is explained by the fitted regression model. Advantage of using R^2 is that its scale is intuitive, and an

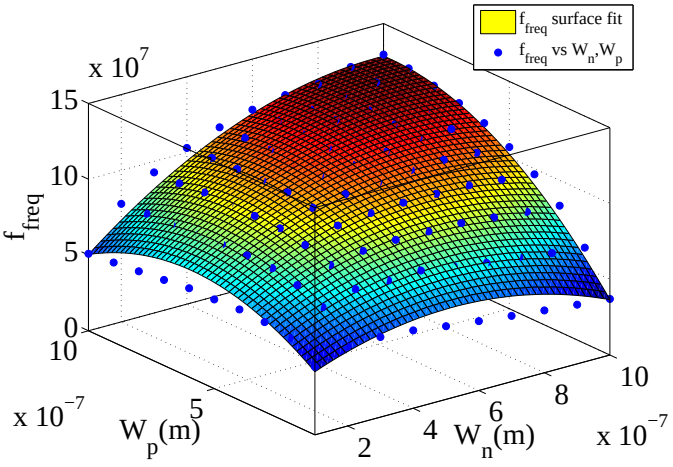

Fig. 4. Surface plot for oscillating frequency of the VCO.

improvement in the regression model results in proportional increase in R^2. The closer R^2 is to 1, the greater the degree of association between variables x and the response. Equation 10 is used for measuring R^2.

$$R^2 = 1 - \frac{\sum_{i=0}^{N}(f(x_i) - \widehat{f(x_i)})^2}{\sum_{i=0}^{N}(f(x_i) - \overline{f(x_i)})^2}. \quad (10)$$

Where $\overline{f(x_i)}$ is the mean of the response at point (x_i) of the data point observations. We report an R^2 value of 0.9943 for the power model.

B. Polynomial Regression Modeling of VCO Frequency

Equation 11 shows the coefficient matrix obtained for the frequency model. The corresponding surface plot for oscillating frequency is shown in figure 4 .

$$p_{ij}(freq) = \begin{bmatrix} 1.10 \times 10^8 & 1.61 \times 10^7 & -1.02 \times 10^7 \\ 1.17 \times 10^7 & 8.57 \times 10^6 & 0 \\ -8.41 \times 10^6 & 0 & 0 \end{bmatrix} \quad (11)$$

The goodness of fit is measured using SSE, RMSE and R^2 described in equations 7, 8 and 10, respectively. SSE of 4.76 $\times 10^{15}$ Hz, RMSE of 2.184 MHz and R^2 of 0.9953 is reported for the frequency model.

IV. Constrained Optimization of VCO using Genetic Algorithm (GA)

This section discusses the development of the cost function, constraint function and Genetic Algorithm (GA) used for optimization. We formulate the optimization problem as follows:

$$\begin{aligned} \text{minimize} \quad & \text{Power}_{VCO} \\ \text{such that} \quad & \text{Frequency}_{VCO} \geq 100MHz, \\ & 100nm \leq [W_p, W_n]^T \leq 1\mu m. \end{aligned} \quad (12)$$

In order to make equation 12 the same format as equation 1, we formulate the optimization problem as follows:

$$\begin{aligned} \text{minimize} \quad & g(x) = \text{Power}_{VCO} \\ \text{such that} \quad & 100 \times 10^6 - \text{Frequency}_{VCO} \leq 0, \\ & 100nm \leq x \leq 1\mu m. \end{aligned} \quad (13)$$

Where cost function is $g(x)$=Power$_{VCO}$ and constraint function is $h(x) = 100 \times 10^6$-Frequency$_{VCO}$. The lower and upper bounds for the design variable set $x = [W_p, W_n]^T$ are 100nm and 1μm respectively. The cost function is minimized through a Genetic Algorithm.

The Genetic Algorithm has an advantage over most of other techniques presented in current literature as it helps in formulating the problem as a nonlinear optimization with equality and inequality constraints [21]. Algorithm 1 shows the pseudocode for GA applied to VCO. The inputs to the algorithm are the cost function $g(x)$, the non-linear inequality constraint function $h(x)$ and the lower (X_L) and upper (X_H) bounds to the design solution set x. New candidates (children) for the design solution set are generated with a mechanism called crossover (rate=0.8) which combines part of the genetic material of each parent x' and then applies a random mutation. If the child x'_{child} inherits good characteristics from its parents x', it will have a higher probability to survive. The values of child x'_{child} are stored in the set of children x''. The fitness of the child $x''$and parent x' population is then evaluated using $g(x)$, $h(x)$ and the survivors can be formed either by the fittest from $x'' \cup$ the fittest from x'.

Genetic Algorithm first accepts a set of design solution set (statements 6 and 7 in algorithm 1), and then constructs a set of child design solution set (statements 9 to 15 in algorithm 1). The stopping criterion is provided by the number of generations (maxgen). Table II shows the final design solution set obtained from proposed Genetic Algorithm based optimization.

TABLE II
Comparison of objectives in baseline and optimized VCO.

Design	W_p	W_n	Power$_{VCO}$	Frequency$_{VCO}$
Baseline	1μm	500nm	60μW	111.4 MHz
Optimized	482nm	434nm	47μW	105.4 MHz

V. Conclusions and Future Research

A polynomial regression model assisted constrained multi-objective optimization has been carried out on a 50nm VCO for simultaneous frequency and power optimization. A model-based approach is beneficial as it is faster than optimizing the actual circuit. The proposed approach leads to 21.67% power reduction and a frequency $\geq$ 100 MHz is maintained. As part of future research, regression based models will be developed, taking into account supply sensitivity, temperature sensitivity and parasitics. VCO performance parameters other than power and frequency, such as phase noise, tuning linearity will also

Algorithm 1 Proposed Genetic Algorithm (GA) for VCO Optimization.

Input: Cost function $g(x)$, constraint function $h(x)$, 100nm $\leq x \leq 1\mu$m and design solution set x.
Output: Optimal design solution x_{opt}.
Generate initial population design variable x.
Initialize the number of iterations, gen=0.
while gen $<$ maxgen-1 **do**
    Select mating pool from the initial population as $x' \subset x$.
    Initialize set of children $x''= \emptyset$.
    for i=0 to populationsize-1 **do**
        Select individuals x'_a at random from x'.
        Apply crossover to x'_a to produce child x'_{child}.
        Randomly mutate produced child x'_{child}.
        x''=$x'' \cup x'_{child}$.
    end for
    x'''=$x'' \cup x'$.
    Evaluate fitness using $g(x''')$, $h(x''')$.
    Increment the counter as gen=gen+1.
end while
The optimal solution is obtained: x_{opt}=x'''.
Assign x_{opt} to transistors in VCO and recreate the design using the new parameters.
Re-simulate VCO to characterize for $freq$ and pwr.

be considered. Also, the constrained optimization problem presented in this paper will solved using other algorithms such as the Lagrange multiplier method and artificial bee colony. The effects of process variation will be incorporated in future statistical design flows.

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