Metamodel-Assisted Fast and Accurate Optimization of an OP-AMP for Biomedical Applications

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***Abstract*—The optimized OP-AMPs resulting out of a traditional flows, although may meet the given specifications after consuming significant design cycle time, do not guarantee an optimal system performance. In this paper, a three-step polynomial metamodel-assisted OP-AMP optimization flow is proposed to address these issues. The flow incorporate polynomial metamodeling, Verilog-AMS integration, and a customized Cuckoo Search optimization. To the best of the authors' knowledge, this paper for the first time presents such a design flow for state-of-the art OP-AMP optimization. Highly accurate and ultra-fast ($\sim$17000$\times$ speedup compared to traditional methods) polynomial metamodels are generated to estimate OP-AMP performance. An OP-AMP meta-macromodel is constructed and is integrated into a Verilog-AMS module (called Verilog-AMS-POM) to facilitate fast time-domain simulations. The core optimization module is a customized Cuckoo Search algorithm which produces promising optimized results. The OP-AMP power dissipation is reduced from 252.8 μW to 65.5μW (3.86$\times$ improvement).**

I. Introduction and Contributions

In order to achieve high performance and high yield, an analog/mixed-signal (AMS) system must be optimized at both system and circuit levels. For a top-down design approach, this starts with designing and optimizing the system with sub-block models at high levels of abstraction. The specifications for each sub-block that lead to the best system performance are then obtained. Each sub-block is then designed and optimized toward these specifications. The issue with this approach is that generating an accurate model, if it is even feasible, takes significant effort. Therefore some characteristics of the sub-blocks are ignored at the high-level simulation. This makes the obtained sub-block specifications less reliable.

To address the aforementioned issues, **a three-step optimization flow is proposed in this paper using an OP-AMP as a case study**. The proposed flow is assisted by POlynomial Metamodels (POMs) to significantly reduce the design optimization cycles. In the first step, based on the specifications from high-level simulations, an optimized OP-AMP design is obtained by ultra-fast POM-assisted optimization. This optimized design serves as the starting point for constructing an OP-AMP meta-macromodel in the second step. The meta-macromodel is then integrated into a Verilog-AMS module-which is used at system-level simulations and can greatly reduce the computation time. The third step performs optimization at the system level. The computation time is greatly reduced due to the use of the **Verilog-AMS PO**lynomial **M**eta-macromodel (which is called **Verilog-AMS-POM** in this paper). The meta-macromodel is the polynomial metamodel generated from the macromodel (i.e. transfer function or SPICE macromodel). Since the optimization is performed at system-level with the circuit-level metamodel based on the OP-AMP design, the resulting final OP-AMP design has a much higher chance of meting the system requirements and attaining much higher performance. For the optimization a customized Cuckoo Search algorithm is used for the first time for OP-AMP optimization through Verilog-AMS-POM.

The rest of this paper is organized as follows: Section II discusses previous research relevant to OP-AMP macromodeling and behavioral implementations. Section III describes the two-stage op-amp design used through out the study of the proposed optimization flow. Section IV presents the POM-assisted proposed optimization flow. Section V concludes this research and discusses future research.

II. Related Prior Research

Macromodeling is a popular technique to generate simpler circuit representations for reducing simulation time. In [1], the OP-AMP to be modeled was first divided into basic building blocks and then these blocks, based on their functionality, were replaced with appropriate simplified models composed of ideal circuit elements. A symbolic expression relating the input and output response can be generated through algebraic or graph-based methods [2]. Traditionally symbolic analysis is suitable for modeling the small-signal behaviors, not for the large-transient responses such as the OP-AMP slewing and settling. A method was proposed in [3] to overcome this shortcoming.

In [4] and [5], Verilog-A OP-AMP behavioral models was used to estimate the specifications used in a switched-capacitor filter. In [6], the continuous-time transfer function of an OP-AMP under voltage follower configuration was discretized and modeled using VHDL. A VHDL-AMS OP-AMP behavioral model was proposed in [7].The VHDL-AMS OP-AMP model in [8] was based on a three-stage model. In [9], a framework for extracting circuit parameters was proposed.

III. The Case Study Circuit: An OP-AMP for Biomedical Applications

The schematic of the case-study OP-AMP design is shown in Fig. 1. This two-stage OP-AMP consists of a folded-cascode operational transconductance amplifier (OTA) for high gain and a common-source amplifier as output stage for low output

resistance. A Common-Mode FeedBack (CMFB) circuit is used to regulate the output common-mode voltages. The two-stage OP-AMP is compensated using Miller capacitors C_1 and C_2. M_{21} and M_{22} act as resistors to remove right-half plane zero. A fully differential implementation is used in order to suppress common-mode noise and thus the even-order harmonic distortion. A 90 nm CMOS process with 1 V power supply is used for this design. The input devices of the OTA are a pair of PMOS transistors.

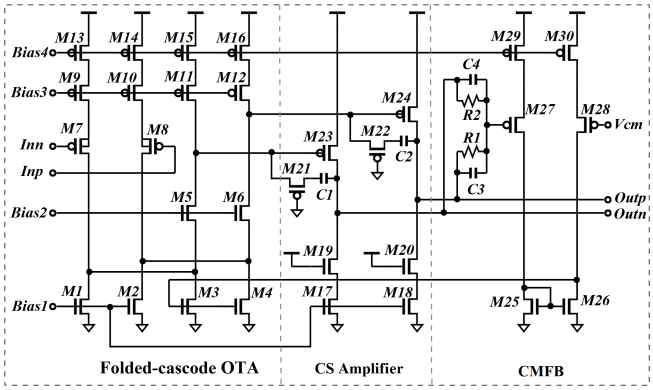

Fig. 1. The schematic of the OP-AMP.

The OP-AMP drives a 50 kΩ resistor and a 1 pF capacitor. For the given application, the required DC gain and bandwidth are at least 43 dB and 40 kHz, respectively. The transistor sizing is based on the g_m/I_D method [10] in order to maximize the current efficiency. The simulated performance together with the specifications are shown in Table I. The transistor sizes for the baseline design are listed in Table II. The simulated DC gain is 52.3 dB, the bandwidth is 58 kHz, the phase margin is 92.5^o, and the gain margin is -25 dB. The baseline design satisfies the gain-bandwidth and stability requirements. in addition, this design requires the slew rate to be greater than 4 mV/ns.

TABLE I
CHARACTERISTICS OF THE OP-AMP.

Performance	Specifications	Baseline
$\boldsymbol{A_0}$ (dB)	43	52.3
BW (kHz)	40	58
PM (degree)	65	92.5
SR (mV/ns)	4	5.1
$\boldsymbol{P_D}$ (μW)	minimized	252.8

IV. THE PROPOSED POLYNOMIAL METAMODEL-ASSISTED DESIGN OPTIMIZATION FLOW

A. High-level Design Optimization Flow

The proposed design optimization flow is shown in Fig. 2. The compete optimization flow can be divided into three step. This work studied and implemented the first two steps. Step 1 starts with the baseline OP-AMP design and generates an optimized op-amp design which serves as the starting point of Step 2 where an op-amp Verilog-AMS meta-macromodel is constructed. Assuming the op-amp is a sub-block of an AMS system, the original op-amp transistor-level netlist is replaced with the Verilog-AMS meta-macromodel in Step 3 to enable fast AMS simulations. The sub-blocks including the op-amp design can then be further optimized toward better system performance.

Metamodels are used in both Step 1 and Step 2. In Step 1, a set of metamodels are generated to predict the OP-AMP characteristics such as gain, bandwidth, phase margin, and slew rate. This allow the optimizer to process this information without conducting actual circuit simulations. The elimination of the need of performing transistor-level simulations saves a huge amount of simulation time. This is studied in Section IV-C. In Step 2, a set of OP-AMP parameter metamodels are generated which are necessary for constructing the OP-AMP meta-macromodel. The procedures of generating the OP-AMP characteristic metamodels and the OP-AMP parameter metamodels are the same and are presented in Section IV-B.

B. Metamodel Generation

The OP-AMP characteristics and the parameters that are used in Section IV-D are modeled using polynomial functions. The polynomial metamodels used have the following format:

$$f(\mathbf{x}) = \sum_{i=0}^{N_B-1} \beta_i \prod_{j=0}^{N_D-1} x_j^{p_{ij}}, \tag{1}$$

where $f(\mathbf{x})$ is the op-amp parameter to be modeled, N_B is the number of basis functions of this polynomial metamodel, β_i is the coefficient for the i-th basis function, N_D is the number of design variables, x_j is the j-th design variables and p_{ij} is the power term for the j-th design variable in the i-th basis function. For example, assuming that the design variables are the width and length of a NMOS and a PMOS ($\mathbf{x} := \{L_N, L_P, W_N, W_P\}$), then N_D = 4. As an example, the polynomial metamodel for the DC gain is the following:

$$\begin{aligned} A_0(\mathbf{x}) = &+ 4.5 \times 10^2 \cdot L_N^0 \cdot L_P^0 \cdot W_N^0 \cdot W_P^0 \\ &+ 0.8 \times 10^9 \cdot L_N^0 \cdot L_P^1 \cdot W_N^0 \cdot W_P^0 \\ &- 1.2 \times 10^{15} \cdot L_N^1 \cdot L_P^0 \cdot W_N^1 \cdot W_P^0 \\ &+ 0.3 \times 10^{16} \cdot L_N^0 \cdot L_P^0 \cdot W_N^0 \cdot W_P^2, \end{aligned} \tag{2}$$

where $A_0(\mathbf{x})$ consists of 4 basis function and is a 2nd order polynomial. The basis function coefficients are: $\beta_0 = 4.5 \times 10^2$, $\beta_1 = 0.8 \times 10^9$, $\beta_2 = -1.2 \times 10^{15}$, and $\beta_3 = 0.3 \times 10^{16}$.

The design variables in this paper are transistor widths, lengths, and the bias current generated in the bias circuitry. There are **sixteen design variables in total** ($N_D = 16$). The design variable values and the associated devices for the baseline design and their ranges are shown in Table II. This table also presents two sets of the optimized values $\text{Optimal}_{\text{SCH}}$ and $\text{Optimal}_{\text{POM}}$ which are discussed in Section IV-C.

The metamodel generation flow with the OP-AMP parameter metamodels $A_0(\mathbf{x})$, $I_{0+}(\mathbf{x})$, $I_{0-}(\mathbf{x})$, $g_{m0}(\mathbf{x})$, $\mathbf{b}(\mathbf{x})$, and $\mathbf{a}(\mathbf{x})$ is shown in Fig. 3. The use of these parameter metamodels is discussed in Section IV-D. The OP-AMP characteristics

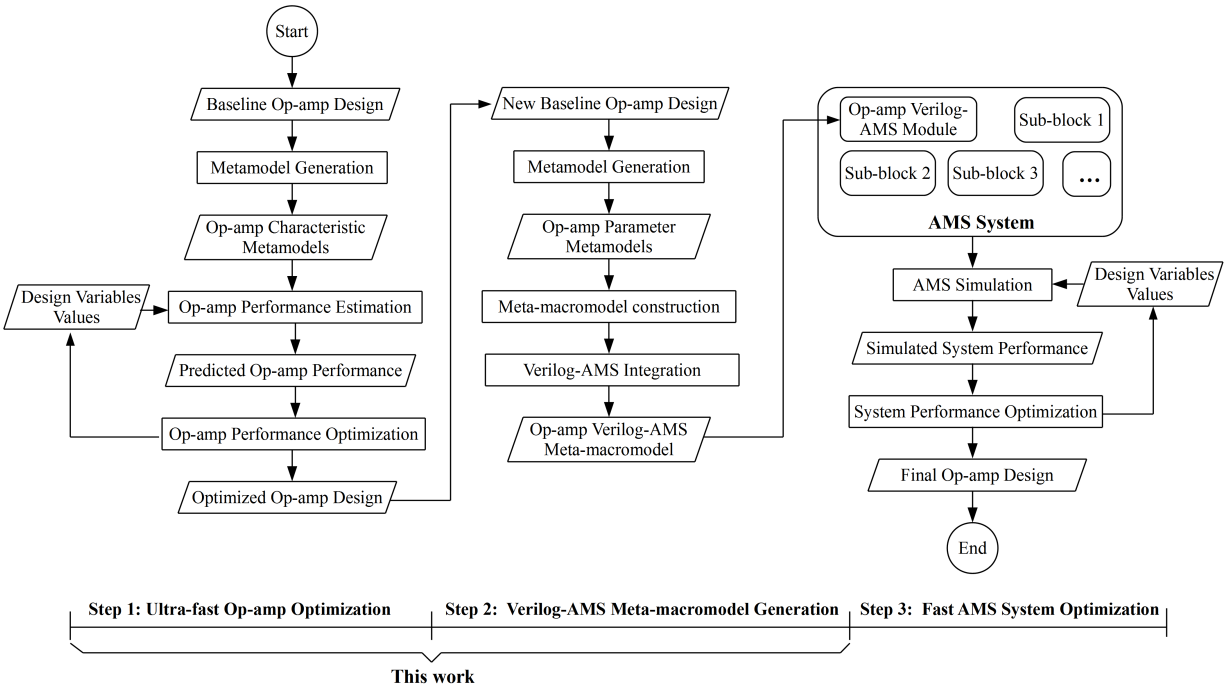

Fig. 2. The proposed ultra-fast circuit-aware OP-AMP design optimization flow.

metamodels are $BW(\mathbf{x})$, $PM(\mathbf{x})$, $SR(\mathbf{x})$, and $P_D(\mathbf{x})$ for the bandwidth, phase margin, slew rate, and power dissipation, respectively. They are generated using the same procedure as that of OP-AMP parameter metamodel generation. The goal is to find β_i and p_{ij} in Eqn. 1 for each OP-AMP parameter in the POM. First, N samples of design variables are generated using the Latin Hypercube Sampling (LHS) technique. For each sample, transistor-level simulations are performed and the resultant OP-AMP parameter samples are extracted. Then, given N design variable samples and N OP-AMP parameter samples, polynomial regression is done to find β_i and p_{ij}. If the resulting POM does not satisfy the accuracy requirement, the order of the polynomial function and/or the sample number can be increased. Increasing the sample number results in longer simulation time. Increasing the polynomial order increases the complexity of the function, which results in longer initialization time when performing simulation using the POM. Experiments show that the second order POM constructed using 200 samples provides high accuracy without noticeably increasing the initialization time.

The mean (μ) and the standard deviation (σ) of the percent error and the root-mean-square error (RMSE) for each OP-AMP parameter are listed in Table III. The POMs for BW, PM, SR, and OP-AMP power dissipation P_D are not used for Verilog-AMS integration which will be discussed in Section IV-E, but they are employed in the metamodel-assisted optimization flow proposed in Section IV-C. Most POMs have a mean percent error less than 1% except PM whose RMSE is still relatively. When the parameter samples exhibit large nonlinearity, the standard deviation of the percent error increases since polynomial regression does not handle large nonlinearity well. The standard deviations of the percent errors of PM, SR, and P_D are all over 10% but less than 15%. However, their RMSEs are all very small.

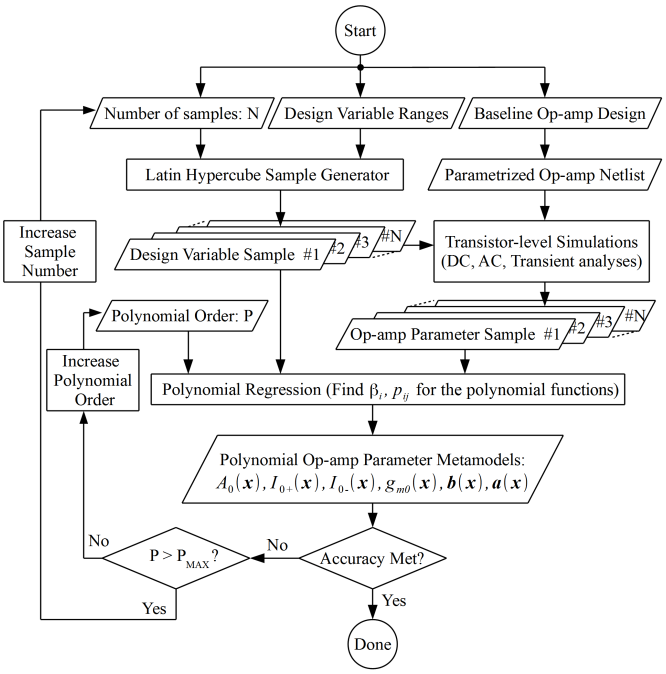

Fig. 3. The proposed flow for OP-AMP metamodel generation.

TABLE II
SUMMARY OF THE OP-AMP DESIGN VARIABLES.

Design Variables	Baseline (μm)	Minimum (μm)	Maximum (μm)	Optimal$_{POM}$ (μm)	Optimal$_{SCH}$ (μm)	Devices
L_{inOTA}	0.180	0.090	0.270	0.090	0.090	$M_{7,8}$
L_{npOTA}	0.270	0.225	0.315	0.275	0.255	$M_{1-6,9-16,25,26,29,30}$
L_{inCS}	0.090	0.090	0.270	0.213	0.135	$M_{23,24}$
L_{nCS}	0.090	0.090	0.180	0.151	0.147	M_{17-20}
L_{inCMFB}	0.180	0.090	0.270	0.249	0.131	$M_{27,28}$
L_C	0.180	0.090	0.270	0.145	0.123	$M_{21,22}$
W_{inOTA}	49.950	25.000	75.000	59.094	33.902	$M_{7,8}$
W_{nOTA}	9.000	4.500	13.500	13.500	13.500	M_{1-6}
W_{pOTA}	18.000	9.000	27.000	9.000	9.000	M_{9-16}
W_{inCS}	72.000	36.000	144.000	88.525	36.000	$M_{23,24}$
W_{nCS}	36.000	18.000	72.000	18.000	18.000	M_{17-20}
W_{inCMFB}	5.400	2.700	8.100	8.100	3.842	$M_{27,28}$
W_{nCMFB}	1.800	0.900	2.70	2.681	0.900	$M_{25,26}$
W_{pCMFB}	3.600	1.800	5.400	4.233	1.800	$M_{29,30}$
W_C	0.90	0.450	1.350	1.282	1.350	$M_{21,22}$
I_{BIAS}	0.500 μA	0.100 μA	1.000 μA	0.986 μA	1.000 μA	-

TABLE III
METAMODEL ACCURACY OF OP-AMP PARAMETERS.

Op-amp Parameters	μ % Error	σ % Error	RMSE
A_0	0.27	4.33	1.51 V/V
g_{m0}	0.13	1.5	0.07 μA/V
I_{0+}	0.18	1.30	6.11 nA
I_{0-}	0.13	2.86	8.05 nA
BW	0.53	5.42	40.21 Hz
PM	2.86	14.65	0.83^o
SR	0.11	10.73	0.02 mV/ns
P_D	0.77	11.74	0.70 μW

C. Metamodel-Assisted Optimization

Electronic devices for biomedical applications usually require ultra-low power dissipation. In this section, the OP-AMP design presented in Section III is optimized using a POM-assisted Cuckoo Search algorithm [11]. The POMs developed using the flow presented in Section IV-B are used to estimate the op-amp characteristics for each possible solution. Another optimization result using the same Cuckoo Search algorithm but with the aid of the op-amp schematic netlist is also presented. In this schematic netlist based optimization, the op-amp characteristics for the possible solutions are obtained by running transistor-level simulation. The optimized op-amp designs and the computation time of the two optimization approaches are compared. The POM-assisted Cuckoo Search is shown in Algorithm 1.

Algorithm 1 POM-assisted Cuckoo Search optimization.

Initialize n designs $\mathbf{x}_k$ $(k = 1, 2, ..., n)$;
$N_{iter} \leftarrow 0$;
Evaluate $P_D(\mathbf{x}_i)$ $(k = 1, 2, ..., n)$;
Find $P_{D,min}$ among current designs;
while ($P_{D,obj} < P_{D,min}$) and ($N_{iter} < N_{iter,max}$) **do**
  Get a new design $\mathbf{x}_i$ randomly by Lévy flights;
  Evaluate $P_D(\mathbf{x}_i)$;
  Choose a design among $\mathbf{x}_k$ (say $\mathbf{x}_j$) randomly;
  if $P_D(\mathbf{x}_i) < P_D(\mathbf{x}_j)$ **then**
    Constraint$_1 \leftarrow A_0(\mathbf{x}_i) > A_{0min}$;
    Constraint$_2 \leftarrow BW(\mathbf{x}_i) > BW_{min}$;
    Constraint$_3 \leftarrow PM(\mathbf{x}_i) > PM_{min}$;
    Constraint$_4 \leftarrow SR(\mathbf{x}_i) > SR_{min}$;
    if All constraints met **then**
      Replace $\mathbf{x}_j$ by $\mathbf{x}_j$;
    end if
  end if
  Evaluate $P_D(\mathbf{x}_k)$ $(k = 1, 2, ..., n)$;
  Rank $\mathbf{x}_k$ based on $P_D(\mathbf{x}_k)$ $(k = 1, 2, ..., n)$;
  Abandon a fraction (p_a) of worst designs;
  Generate new designs randomly by Lévy flights ;
  Find $P_{D,min}$ among current designs;
  $N_{iter} \leftarrow N_{iter} + 2n$;
end while

The objective of the optimization is to **minimize the OP-AMP power dissipation** with the gain, bandwidth, phase margin, and slew rate as the constraints. The objective $P_{D,min}$, the initial number of solutions n and the maximum number of iterations allowed $N_{iter,max}$ are tentatively set to be 65μW, 10, and 1200, respectively. The POM $A_0(\mathbf{x})$, $BW(\mathbf{x})$, $PM(\mathbf{x})$, and $SR(\mathbf{x})$ are used to estimate the OP-AMP performance and thus to determine if the constraints are met. The POM $P_D(\mathbf{x})$ is used as the objective function to predicate the OP-AMP power dissipation for each possible

solution. The optimized designs generated using the POM-assisted and schematic netlist based Cuckoo Search optimization are shown in Table II which are denoted as $\text{Optimal}_{\text{POM}}$ and $\text{Optimal}_{\text{SCH}}$, respectively. With the optimized designs, the corresponding OP-AMP performances are obtained by running actual transistor-level simulations. The constraints and objective, and the performance of the optimized OP-AMP designs are summarized in Table IV, which shows that the OP-AMP performance has been greatly improved. Table V compares the performance of $\text{Optimal}_{\text{POM}}$ and $\text{Optimal}_{\text{SCH}}$. The power reduction reported is with respect to the baseline design. In the maximum allowed number of iterations, both optimizations achieve significant power reduction. However, $\text{Optimal}_{\text{POM}}$ completes the optimization in 2.6 seconds while the $\text{Optimal}_{\text{SCH}}$ uses more than 12 hours to finish the process. In this case, the **metamodel-assisted optimization is 17120 times faster** than the traditional method. The iterations of the Cuckoo Search algorithm optimizations are shown in Fig. 4.

TABLE IV
OPTIMIZATION RESULTS FOR THE OP-AMP DESIGN.

Performance	Constraint	$\text{Optimal}_{\text{POM}}$	$\text{Optimal}_{\text{SCH}}$
A_0 (dB)	> 43	56.4	52.8
BW (kHz)	> 50	58.9	85.5
PM (degree)	> 70	84.4	87.7
SR (mV/ns)	> 5	7.1	8
Objective			
P_D (μW)	~ 65	65.5	68.1

TABLE V
COMPARISON OF OP-AMP OPTIMIZATION

Performance	$\text{Optimal}_{\text{SCH}}$	$\text{Optimal}_{\text{POM}}$
Power Reduction	$\times$3.71	$\times$3.86
Number of iterations	1200	1200
Computation Time	12.5 h	2.6 s
Normalized Speed	1	$\times$17120

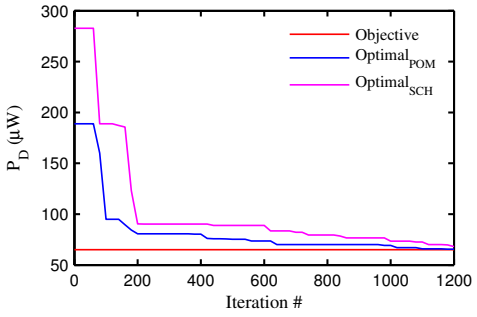

Fig. 4. The iteration of the Cuckoo Search optimization.

D. Meta-macromodeling

A complete OP-AMP behavioral model should not only model its small-signal behavior but also the large-signal behavior. The signal transfer function of an OP-AMP obtained from AC analysis can describe the small-signal behavior, but it does not account for the large-signal characteristics including the slewing and settling behaviors. In [12], an OP-AMP macromodel was proposed in order to analyze these behaviors. The model is redrawn in Fig. 5 and is customized to be used as the baseline of the OP-AMP meta-macromodel.

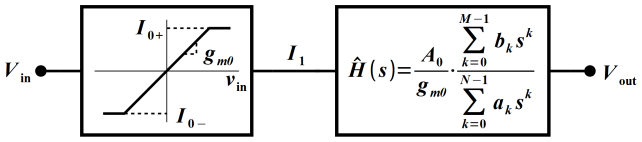

Fig. 5. The OP-AMP macromodel for transient analysis.

The model consists of two stages. The first stage describes the transfer characteristic of the OP-AMP input stage due to the limited maximum available positive and negative currents I_{0+} and I_{0-}. A_0 is the open-loop DC gain of the OP-AMP. g_{m0} is the transconductance of the OP-AMP input stage. The second stage is the OP-AMP small-signal transfer function. In [12], the circuit was assumed to be properly designed and thus no zero and only two poles were presented to form the transfer function. This assumption is most likely invalid when performing design exploration. The numbers of poles and zeros are not limited in order to attain high fidelity. For simplicity, the following is defined:

$$\begin{aligned} \mathbf{b} &:= \{b_0, b_1, b_2, ..., b_{M-1}\}, \\ \mathbf{a} &:= \{a_0, a_1, a_2, ..., a_{N-1}\}. \end{aligned} \tag{3}$$

The OP-AMP circuit parameters A_0, I_{0+}, I_{0-}, g_{m0}, $\mathbf{b}$, and $\mathbf{a}$ directly affect the model accuracy. In traditional symbolic macromodeling, these parameters are extracted from transistor-level simulations. When exploring the design space, the extraction has to be redone whenever the values of the design variables are updated. This approach is inefficient. With the proposed meta-macromodeling technique, no extraction is required during design exploration. Prior to design exploration, the OP-AMP parameters are sampled and their metamodels are generated. In metamodel-assisted design exploration, when the optimization algorithm updates the design variable value $\mathbf{x}$, a new set of OP-AMP parameters will be computed using the parameter metamodels without performing circuit simulations and extraction. The new set of OP-AMP parameters can be directly used in the macromodel and thus greatly improves the optimization flow.

E. Verilog-AMS-POM

Transient analyses for complex circuits at transistor-level may take long time. For example, simulating an analog-to-digital converter with high-order delta-sigma modulator may takes hours or days if layout parasitics are included. Thus, it is desired to replace transistor-level blocks with behavioral models as much as possible to reduce the simulation time. Thus, the construction of a Verilog-AMS module for the developed polynomial meta-macromodel (Verilog-AMS-POM) of the OP-AMP is needed. The designed module reads

a text files storing the β_i and p_{ij} for each OP-AMP parameter POM and the given design variable values. The OP-AMP parameters A_0, I_{0+}, I_{0-}, g_{m0}, $\mathbf{b}$, and $\mathbf{a}$ are then computed. An `analog` process implements the models seen in Fig. 5. The Verilog-AMS-POM can be easily scaled for different numbers of design variables and/or polynomial orders.

The AC analysis results of transistor-level schematic, the 1st and 2nd order Verilog-AMS-POMs for the baseline OP-AMP are shown in Fig. 6. It can be seen that both the 1st and 2nd order POM results match those of the schematic quite well at lower frequencies. At higher frequencies (~ 200 MHz) the 1st order POM exhibits noticeable errors while the 2nd order POM still attains good match. Thus the 2nd order POM is adopted in this paper. The OP-AMP response for step inputs under the unity-gain configuration is shown in Fig. 7. The mismatch seen in the step responses is due to the fact that the large input signal causes the poles and zeros of the OP-AMP to deviate from their original location. One solution is, as suggested in [3], to extract two sets of poles and zeros under different bias conditions of interest. Two transfer functions can thus be constructed from different signal levels. However, this is out of the scope of this paper.

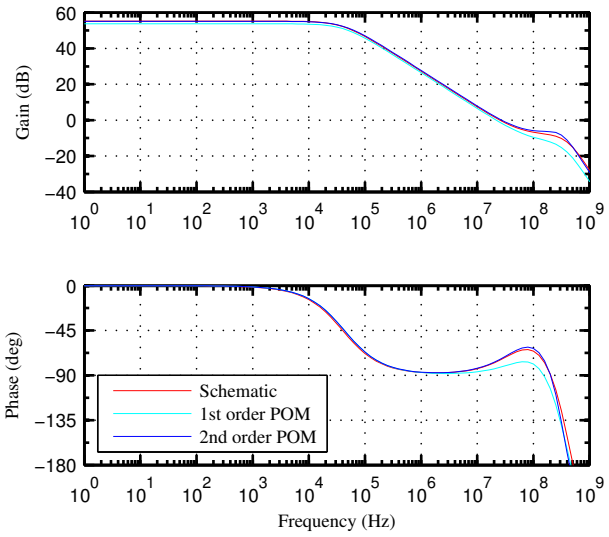

Fig. 6. AC analysis of the OP-AMP.

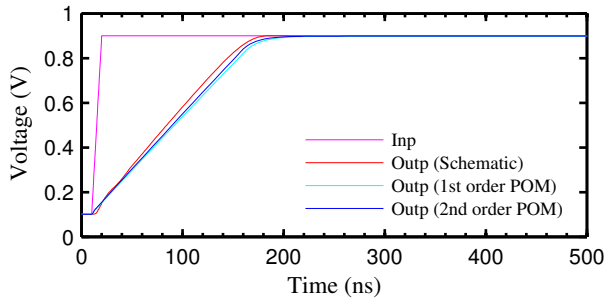

Fig. 7. Transient simulation of OP-AMP with a step input.

In order to decide whether to use the OP-AMP Verilog-AMS-POM or the traditional macromodel in the optimization of a large-scale mixed-signal system that requires long transient analysis times, it is necessary to compare their computation time. Assuming that the Verilog-AMS-POM is constructed using 200 samples, that the optimization takes $N_i = 1200$ iterations, and that extracting the op-amp parameters for each design takes 60 seconds, the computation time reduction by using the POM based technique is $t_D \approx 16.7$ hours.

V. Conclusion and Future Research

A proposed POM-assisted OP-AMP optimization flow has been presented. The OP-AMP characteristic POMs can accurately predict the op-amp performance with ultra-high speed. The OP-AMP meta-macromodeling technique has been discussed and the Verilog-AMS integration approach has been presented for time-domain simulations. The customized Cuckoo Search algorithm shows promising optimization results. Future research includes studying system-level optimization using the developed OP-AMP meta-macromodel.

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