Process Variation Tolerant 9T SRAM Bitcell Design

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***Abstract*—In this paper, a nine-transistor (9T) Static Random Access Memory (SRAM) bitcell for the low voltage and energy constraint applications is proposed. It is well known that in sub-threshold regime, reliability and process variations are the main design challenges, and standard six-transistor (6T) SRAM bitcell fails to operate in sub-V_{TH}. The proposed design has better read stability and improved process variation tolerant as compared to standard 6T SRAM at low voltage. Simulation results based on 32nm technology node shows that there is 37% improvement in the read stability as compared to standard 6T SRAM bitcell. The proposed design also address the conflicting read and write requirements, therefore, one can optimize the read static noise margin (SNM), write noise margin and write speed for a particular application by selecting the bitcell ratios for read and write operations.**

I. Introduction

An obvious way to reduce Static Random Access Memory (SRAM) energy per operation is to reduce V_{DD}, which will decrease active power quadratically and leakage power linearly. If V_{DD} is decreased, however, increased delay time causes this leakage power to be integrated over a long-time interval, thus increasing the Power Delay Product (PDP). By modifying the architecture of existing SRAM circuits while keeping the reliability and process variation in mind, we can improve the performance even at lower V_{DD}. In standard 6T SRAMs, minimum feature sized devices are preferably used to provide high cache density, as a result, read and write stability degrade significantly due to process variation. As cache is embedding in every Integrated Circuit (IC) for better performance, the importance of SRAM which will work at low power and in nano-regime has been increased in the recent past to meet energy requirement of the portable or hand held devices.

Design of sub-threshold SRAM cells reduces both leakage and access energy for low power applications and introduces compatibility with the sub-threshold logic to allow system integration [1], [2]. In sub-threshold regime, reliability and process variations are the main design challenges, and standard six-transistor (6T) SRAM bitcell fails to operate in sub-V_{TH} [3], [4]. In 6T SRAM bitcell desired read and write margins are achieved by relying on length and width ratios of transistors. But process variation makes this method of length and width ratios unreliable for sub V_{TH} SRAM bitcell design. To increase the read stability extra peripheral circuitry can be added to 6T SRAM bitcell at the cost of increased area overhead and power consumption.

Several SRAM bitcell topologies have been proposed in the recent past to improve read stability [3], [5]–[8]. 8T SRAM bitcell proposed in [6] marginally adds 30% area overhead to the typical 6T SRAM bitcell. The two extra transistors acts as a buffer or a separate read port which protects the stored data during a memory read. Typically in 6T SRAM, at the onset of read cycle, the node stored '0' state is connected to precharged bit line, which raises the node voltage and reduces read noise margin. In 8T SRAM bitcell because of included buffer isolates this node from the bitline, thus improves the read margin almost equal to hold margin. In 8T SRAM bitcell, only a single word-line transistor blocks charge from leaking off read bitline (RBL). High bitline leakage affects the number of rows (or cells) that can be connected to a single bitline. The 10T bitcell proposed in [3] reduces this bit line leakage by adding two more transistors in the read buffer path. Both 8T and 10T uses single ended sensing which has some major drawbacks. In single ended sensing, bitcell utilizes large signal sensing featuring domino style hierarchical bitlines. Large signal sensing and hierarchical bitline organization results in poor array efficiency and high power consumption [9]. The 9T SRAM proposed in [10] uses differential sensing, it is having isolated read buffer. This design is having very good read noise margin, but read speed decreases because of body effect.

In this paper, we have proposed a new 9T SRAM without separate read and write bitlines (or a read buffer). The proposed design has better stability and process variation tolerance compared to standard 6T SRAM bitcell. In the proposed design there is no effect on write speed by increasing the bitcell ratio as there are different bitcell ratio definitions under read and write operations. We simulated the proposed 9T SRAM design using 32nm technology node files of Predictive Technology Models (PTM) [11]. The rest of this paper is organized as follows: Section II presents the conventional (or standard) 6T bitcell SRAM and its read and write operations. The proposed 9T bitcell and its features and operations are discussed in Section III. Section IV deals with the process variations for different voltage levels. Summary of key conclusions is provided in Section V.

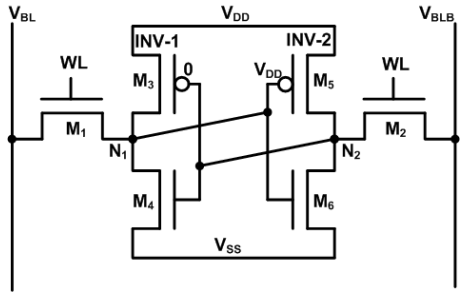

Fig. 1. Schematic diagram of a standard 6T SRAM bitcell.

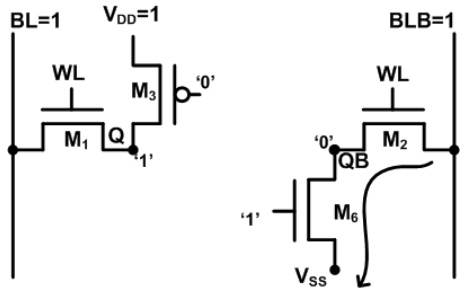

Fig. 2. Read equivalent diagram of a standard 6T SRAM bitcell.

II. Conventional 6T SRAM

SRAM bitcell is the basic building block of SRAM caches. Each bitcell stores one bit of information. The main parameters that should keep in mind while designing SRAM bitcells are bitcell area, speed, stability, power consumption and yield. Fig. 1 shows the schematic diagram of conventional 6T SRAM bitcell. A conventional 6T-SRAM bitcell consists of two cross coupled inverters (INV1 and INV2) and access transistors (M1 and M2). The access transistors allow access to the data stored during read and write operations and provide isolation from other bitcells during hold state. Bitcells are accessed by asserting the word-line (WL) during a read or write operation by the access transistors.

A. Read operation

Fig. 2 shows the 6T SRAM equivalent schematic diagram during read operation. Bit lines are precharged to supply voltage before read operation. The read operation is initiated by enabling the word-line (WL) and thereby connecting the internal nodes of the SRAM bitcell to bit-lines. The bit line voltage is pulled down by the nMOS transistor at the '0' storage node and the difference between two bit line voltages will be detected by sense amplifier. When the word line(WL) is high, one of the bit line voltages is pulled down through transistors M2 and M6 or M1 and M4. The transistors M2 and M6 forms a voltage divider, because of current flowing through M2, the potential at node QB is no longer at '0'V. Also it should not go beyond switching threshold of inverter (INV1) to avoid destructive read. The rising of potential depends on sizing of access transistor and pull down transistor which is defined as a bitcell ratio.

TABLE I
Variation in different parameters of standard 6T with bitcell ratio.

bitcell Ratio	1	1.5	2	2.5	3
SNM (mV)	27.4	60.7	79.7	91.9	102.3
Write Time (ps)	35.38	42.25	47.48	52.17	57.15

B. Write operation

The write operation begins by forcing a differential voltage (V_{DD}, and 0) at the bitline pairs (BLB and BL). This differential voltage corresponds to the data to be written at the storage nodes (Q and QB) and it is controlled by the write drivers. The WL is then activated to store the information from the bit-line pairs to corresponding storage nodes. Assume, the nodes Q and QB initially store values '1' and '0' respectively. When the WL is asserted the access transistor (M1) connected to BL (at '0') is turned on, a current flows from V_{DD} to BL through M3 and M1. This current flow lowers the potential at Q. The potential at the node Q has to go below the trip point of the inverter (INV2) for a successful write operation and this depends on the ratio of pull-up transistor (M3) and the access transistor (M1). This ratio is referred to as the pullup- ratio.

C. Hold operation

When WL goes low , SRAM bitcell is in data retention mode. Two cross coupled inverters hold the data, through bistable action. There is destruction in data stored when V_{DD} goes below certain voltage, which is called data retention voltage of SRAM bitcell .

A standard 6T SRAM shows poor read stability as technology scale down to nano-regime. To increase the read stability (measured by read SNM) conventional device sizing can be followed by increasing the bitcell ratio. By increasing the bitcell ratio, read SNM and critical charge (node capacitance) will increase which are desirable. However, at the same time power consumption and write time increases which are not desirable features, as they incur loss of power, performance and increase in area overhead. In Table I it is shown that when we are increasing the bitcell ratio there is significant increase in write time, which will affect the performance of SRAM bitcell.

III. Proposed 9T SRAM Bitcell Design

Fig. 3 shows the proposed 9T SRAM bitcell. The proposed design is comprised a standard 6T SRAM bitcell and three additional nMOS transistors (M7, M8 and M9) and a read wordline (RWL) controlling the transistor M9 during read operation. Additional three nMOS transistors in a standard 6T SRAM are connected in such a way that they address the problem of loss of stability at lower V_{DD} and increased delay with increase in bitcell ratio. Also proposed design employ differential read operation for better read access time. The bitline leakage current in the proposed 9T SRAM is reduced significantly due to stacked combination of four transistors

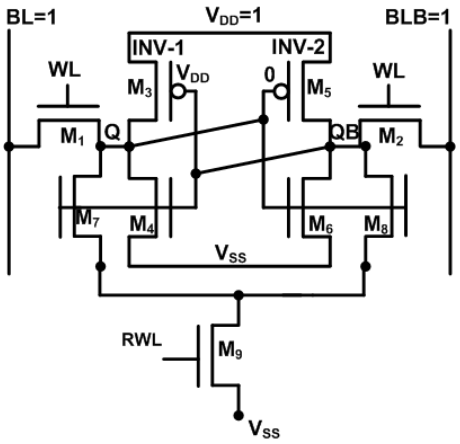

Fig. 3. Schematic diagram of a proposed 9T SRAM bitcell.

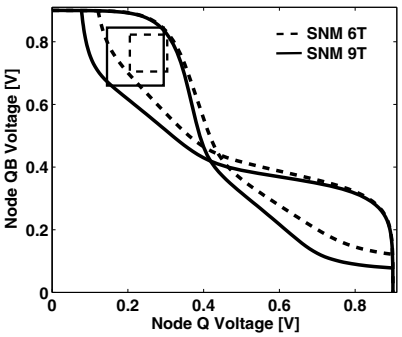

Fig. 4. Comparison of read SNM of a standard 6T and the proposed 9T for a nominal bitcell-ratio.

(M2, M6, M8, M9 from BL or M1, M4, M7, M9 from BLB). As a result it eliminates the limitation of the number of rows or bitcell per bitline.

A. Read operation

An important parameter of SRAM bitcell is read stability. It describes the ability of read operation without destroying the stored information. Measuring the Static Noise Margin (SNM) of an SRAM bitcell will give the metric of read stability. Without loss of generality, we assume that '0' is stored at QB node and '1' is stored at Q, as shown in Fig. 5. Both bit lines are precharged to V_{DD}. During read operation RWL is activated and transistors M6 and M8 are turned on which will form strong pull down compared with conventional 6T SRAM. Strong pull down causes less resistance between data storage nodes to ground, as a result, amount of raise in voltage of node Q will be less. This gives considerable improvement in read SNM. Simulation results show 36% improvement in read SNM of the proposed design as compared to standard 6T SRAM design, as shown in Fig. 4. The proposed design has different bitcell ratios during read (Eqn. 1) and write (Eqn. 2) operation, therefore, it avoids the conflicting read and write requirement up to certain extent.

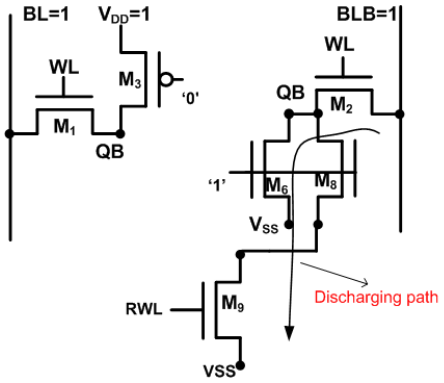

Fig. 5. Read equivalent diagram of a proposed 9T SRAM bitcell.

$$\beta = \frac{(W_4/L_4 + W_7/L_7)}{W_1/L_1} = \frac{(W_6/L_6 + W_8/L_8)}{W_2/L_2} \quad (1)$$

$$\beta = \frac{W_4/L_4}{W_1/L_1} = \frac{W_6/L_6}{W_2/L_2} \quad (2)$$

For read operation ratio of $\frac{W_4/L_4}{W_1/L_1} = \frac{W_6/L_6}{W_2/L_2}$ is kept constant, while bitcell ratio is increased for improved read SNM by varying the size of transistor M7 and M8 by ratio of $\frac{W_7}{L_7} = \frac{W_8}{L_8}$, therefore, this ratio can be optimized separately for read operation.

B. Write operation

The write operation in the proposed design is performed similar to standard 6T SRAM by enabling the wordline (WL) and disabling the read wordline (RWL). Under write operation, transistor M7 and M8 will allow only small leakage current because transistor M9 will be in the cut-off state. Therefore, the bitcell ratio under write operation is given by Eqn. 2 and it can be optimized separately for a target write access time, however, read SNM can be improved by varying the size of transistor M7 and M8 by ratio of $\frac{W_7}{L_7} = \frac{W_8}{L_8}$.

IV. Process Variation and Voltage Scalability

The variation in design and process parameters particularly in threshold voltage (V_{TH}) leads to a drametic loss of parametric yield of SRAM bitcell due to noise margins [4]. The parametric yield of the standard 6T SRAM bitcell decreases considerably as V_{DD} is scaled down imposing lower bound on V_{DD} [12]. It is noted that read SNM, is one of the major obstacles impending the V_{DD} scaling. In order to investigate the effect of process variations, 3000 Monte Carlo (MC) simulations were preformed for 6T and the proposed 9T SRAM bitcells for read stability margins. We assumed a 15% variation in V_{TH} with $\pm 3\sigma$ Gaussian distribution as an independent random variable for all the transistors in SRAM cells (6T and 9T). We use, 32nm Predictive Technology Model (PTM) models for low power applications incorporating high-k/metal gate and stress effect [11]. Following technology

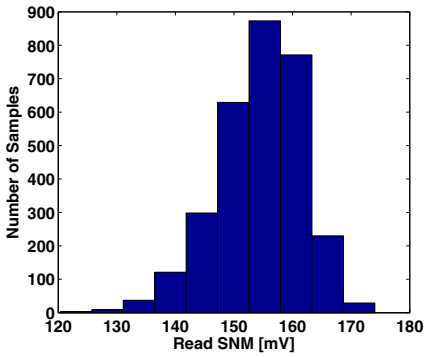

Fig. 6. Distribution of read SNM of the proposed 9T SRAM bitcell for $V_{DD} = 0.9V$.

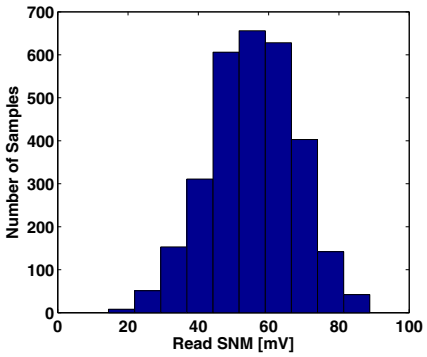

Fig. 8. Distribution of read SNM of the proposed 9T SRAM bitcell for $V_{DD} = 0.4V$.

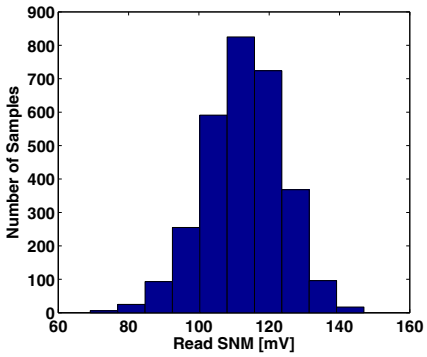

Fig. 7. Distribution of read SNM of the standard 6T SRAM bitcell for $V_{DD} = 0.9V$.

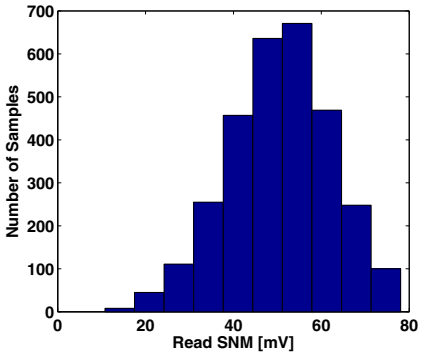

Fig. 9. Distribution of read SNM of the standard 6T SRAM bitcell for $V_{DD} = 0.4V$.

parameters were used for simulation: V_{DD} =0.9V, V_{TH0_n} =0.63V, V_{TH0_n} = - 0.58V, T_{OX_P} =1.3nm and T=110 ^oC

Fig. 6 and 7 show the distribution of read SNM of the proposed 9T and standard 6T SRAM bitcells, respectively, for $V_{DD} = 0.9V$. The mean value (μ) of read SNM of the proposed design is 37% higher than the standard 6T SRAM bitcell (i.e. 155mV against 113mV). The standard deviation (σ) in the proposed design is about 54% less as compared to standard 6T SRAM bitcell (i.e. 7.19mV against 11.03mV). Therefore, the proposed design has better read SNM and process variation tolerance as compared to standard 6T SRAM bitcell.

The low voltage applicability of the proposed design is compared at $V_{DD} = 0.4V$. Fig. 8 and 9 show the distribution of read SNM of the proposed 9T and standard 6T SRAM bitcells, respectively. The mean value (μ) of read SNM of the proposed design is 23% higher than the standard 6T SRAM bitcell (i.e. 62.3mV against 50.6mV). The improvement in the read SNM at lower voltage is not as good as it was at higher $V_{DD}V$, however, standard deviation in the read SNM of the both the design is of the same order.

V. Conclusion

In this paper, a differential read and write 9T SRAM bitcell is presented. The advantages of standard 6T such as differential read which provides lower read access time and lower power consumption during read operation are preserved. However, the conflicting read and write requirements with the increase in bitcell ratio increases the read SNM, while it deteriorates the write performance, is also addressed in this design. The conflicting read and write problem is addressed by providing a separate read wordline, however, proposed design departs from the read SNM free SRAM designs those employs the separate read and write ports. In these designs single ended sensing is used which restrict the number bitcells per bitline. The proposed design has better process variation tolerance and voltage scalability as compared to standard 6T SRAM bitcell. Therefore, the proposed design has significant potential for reliable applications in the nano-regime.

References

[1] A. Wang and A. Chandrakasan, "A 180-mv subthreshold fft processor using a minimum energy design methodology," *Solid-State Circuits, IEEE Journal of*, vol. 40, no. 1, pp. 310–319, Jan. 2005.

[2] J. Kulkarni, K. Kim, and K. Roy, "A 160 mv robust schmitt trigger based subthreshold sram," *Solid-State Circuits, IEEE Journal of*, vol. 42, no. 10, pp. 2303–2313, Oct. 2007.

[3] B. H. Calhoun and A. P. Chandrakasan, "A 256-kb 65-nm sub-threshold sram design for ultra-low-voltage operation," *Solid-State Circuits, IEEE Journal of*, vol. 42, no. 3, pp. 680–688, March 2007.

[4] A.J.Bhavnagarwala, X. Tang, and M. J.D., "The impact of intrinsic device fluctuations on cmos sram cell stability," *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 658–665, Apr 2001.

[5] K. Nii, Y. Masuda, M. Yabuuchi, Y. Tsukamoto, S. Ohbayashi, S. Imaoka, M. Igarashi, K. Tomita, N. Tsuboi, H. Makino, K. Ishibashi, and H. Shinohara, "A 65 nm ultra-high-density dual-port sram with 0.71um 8t-cell for soc," *VLSI Circuits, 2006. Digest of Technical Papers. 2006 Symposium on*, pp. 130–131, 2006.

[6] N. Verma and A. P. Chandrakasan, "A $256kb$ 65nm 8T Subthreshold SRAM Employing Sense-Amplifier Redundancy," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 1, pp. 141–149, Jan. 2008.

[7] S. Ohbayashi, M. Yabuuchi, K. Kono, Y. Oda, S. Imaoka, K. Usui, T. Yonezu, T. Iwamoto, K. Nii, Y. Tsukamoto, M. Arakawa, T. Uchida, M. Okada, A. Ishii, T. Yoshihara, H. Makino, K. Ishibashi, and H. Shinohara, "A 65 nm embedded sram with wafer level burn-in mode, leak-bit redundancy and cu e-trim fuse for known good die," *Solid-State Circuits, IEEE Journal of*, vol. 43, no. 1, pp. 96–108, Jan. 2008.

[8] T. Suzuki, H. Yamauchi, Y. Yamagami, K. Satomi, and H. Akamatsu, "A stable 2-port sram cell design against simultaneously read/write-disturbed accesses," *Solid-State Circuits, IEEE Journal of*, vol. 43, no. 9, pp. 2109–2119, Sept. 2008.

[9] M. Khellah, A. Keshavarzi, D. Somasekhar, T. Karnik, and V. De, "Read and write circuit assist techniques for improving vccmin of dense 6t sram cell," in *Integrated Circuit Design and Technology and Tutorial, 2008. ICICDT 2008. IEEE International Conference on*, june 2008, pp. 185 –188.

[10] Z. Liu and V. Kursun, "Characterization of a novel nine-transistor sram cell," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol. 16, no. 4, pp. 488–492, April 2008.

[11] PTM, "Predictive technology model," in *Nanoscale Integration and Modeling (NIMO) Group at ASU*, http://www.eas.asu.edu/ptm/, 2008.

[12] S. Mukhopadhyay, H. Mahmoodi, and K. Roy, "Modeling of failure probability and statistical design of sram array for yield enhancement in nanoscaled cmos," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 24, no. 12, pp. 1859–1880, Dec. 2005.