Single-Event Transient Analysis in High Speed Circuits

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Abstract

The effect of Single-Event Transients (SETs) (at a combinational node of a design) on the system reliability is becoming a big concern for ICs manufactured using advanced technologies. An SET at a node of a combinational part of a circuit may propagate as a transient pulse at the input of a flip-flop and consequently latches in the flip-flop; thus generating a soft-error. When an SET is combined with a transition at a node (*i.e.,* dynamic behavior of that node) along a critical path of the combinational part of a design, a transient delay fault may occur at the input of a circuit flip-flop. Using the Probability Density Function (PDF) of an SET, this paper proposes a statistical method to compute the probability of soft-errors caused by SETs considering dynamic behavior of a circuit.

I. Introduction

Radiation-induced soft errors pose a major challenge to the `design of memories and logic circuits in nanometer technologies. Neutron radiations from cosmic rays or alpha particles from packaging materials are common causes of soft errors in the nodes of a circuit. These radiations generate concentrated bursts of excess charges at random locations in a semiconductor substrate. These charges may be collected by a reversed bias *p-n* junction resulting in a current pulse of very short duration in the signal value. If this disturbance occurs in the hold state of a memory cell or in a flip-flop, it causes a soft error when the content of the storage element is flipped; this soft-error is called Single-Event Upset (SEU). Furthermore, the transient current pulse due to particle strike may occur in an internal node of a combinational circuit and subsequently is converted to a transient voltage error which be propagated to a storage element and be latched there. In this case, it is usually called Single-Event Transient (SET). Combinational circuits have a natural barrier to propagating SETs to their output. When an SET occurs at an internal node of a logic circuit, there are three masking factors that have impact on the SET: *logical masking*, *temporal masking*, and *electrical masking* [1]. In spite of these three masking mechanisms, an SET with enough amplitude may appear in the sampling window of a flip-flop in the circuit and can be latched in thAT flip-flop.

A. Previous works

Several researches study the soft-error caused by particle strike in the combinational and sequential parts of a circuit. Mohanram [2] proposes a comprehensive technique for simulation of transients caused by SETs in combinational logic circuits. Based upon linear RC models of gates, the proposed technique integrates a closed-form model for computation of the SET-induced transient at the site of a particle strike with propagation models for the transients along a functionally sensitized path. Gill, *et al.* [3] introduce an approach for computing soft error susceptibility of nodes in large CMOS circuits at the transistor level. Zhao, *et al.* [4] propose a noise impact analysis methodology based on a Noise Probability Density Function (NPDF) transformation technique to evaluate the circuit vulnerability to SEU. Hosseinabady, *et al.* [6] study the dynamic behavior of signals in a circuit with massive critical paths in the presence of an SET. They show that a particle strike at a node on a critical path may appear as an erroneous value at the input of a flip-flop in three shapes: a transient pulse fault, a transient late-edge (delay) fault, or a transient early_edge (race) fault.

B. Contributions of the Paper

This paper proposes a statistical method to study the susceptibility of a circuit to transient faults (which are transient pulse, delay, and race faults) caused by particle strikes. For this purpose, we compute the Probability Distribution Function (PDF) of SETs in different nodes of a circuit. Considering temporal, electrical, and logical masking factors, our method propagated the PDF of SETs (instead of propagating the shape of transient pulse) through combinational paths towards flip-flops.

The rest of this paper is organized as follows. The next section describes the models of SET as preliminaries. Section 3 describes an overview of the whole method. The details of the proposed statistical method are explained in Section 4. Section 5 demonstrates experimental results. Finally, conclusions are appeared in the last section.

II. Preliminaries

A. Transient Fault Model

When high-energy neutrons (presented in terrestrial cosmic radiations) or alpha particles (that originated from impurities in the packaging materials) strike a sensitive node in the CMOS circuit, they generate a dense local track of additional electron-hole pairs in the substrate. In the case of CMOS circuits, a sensitive node in the semiconductor is the drain of the OFF-transistors [3]. These additional charges are collected by the drain of an OFF transistor and a current spike is appeared. The current spike can be represented at the device level by a current source. Messenger [5] models this transient current as a double exponential injection current:

$$I_{inj}(t) = \frac{Q}{(\tau_1 - \tau_2)}\left(e^{-\frac{t}{\tau_1}} - e^{-\frac{t}{\tau_2}}\right) \qquad \text{Equ. 1}$$

where Q is the charge (positive or negative) deposited as a result of the particle strike, τ_1 is the collection time-constant of the junction, and τ_2 is the ion-track establishment time-constant. In the rest of the paper, we will use this current model. Karnik, et al. [1] show that an SEU lasts about 100ps for 0.6um technology. In this paper, the maximum width of this transient current pulse is shown by $\tau_{\max}$.

B. Propagating an SET along a path

As authors explain in [6], a transient current pulse at a node caused by particle strikes may be translated to three different shapes in the voltage level of that node, which are: transient pulse, transient late-edge (delay fault), and transient early-edge (race fault). In addition, a propagating transient pulse may change its shape when passes a gate with a transition on its other inputs. Figure 3 shows these different shapes. Dynamic hazard conversion of Figure 3(VI) attenuates the transient pulse width and increase the chance of the electrical masking to eliminate the transient pulse. Thus, we do not consider this effect in the rest of the paper.

C. Timing analysis

In this subsection, we determine the paths in which early and late edges may lead to a soft error. First, we define some terminologies that are useful to determine these sensitive paths.

Slowest combinational path in a combinational part of a design determines the clock frequency of the whole design. In other words, in a design of *n* combinational path, if the delay of a combinational path is DCP_i, then the clock period of the design clock is $T = \max_i(DCP_i)\ i = 0,...n$.

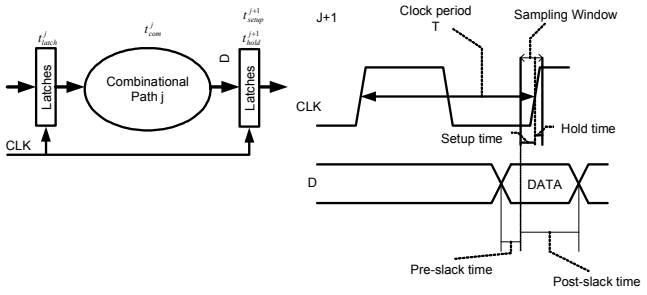


Figure 1 A combinational path

Figure 1 shows a combinational path of a design. It consists of a feeding register (with index *i*), a combinational logic, and a fed register (with index *i+1*). The delay of a non-false path consists of three parts: propagation delay of the feeding register (t^j_{reg}), propagation delay of combinational path (t^j_{com}), and setup time of the fed register (t^{j+1}_{setup}). That is, $DP_j = t^j_{setup} + t^j_{\log ic} + t^{j+1}_{reg}$.

Definition 1: A sampling window (t_{sw}) is the time that is bounded by the setup time (t_{su}) and hold time (t_h) around the active clock edge of a flip-flop (Figure 2-I).

Lemma 1: An SET results in a soft-error if it appears in the sampling window of a flip-flop.

Definition 2: A transient-race fault (early edge) sensitive latch is a latch in which an early edge caused by an SET may results in a soft error.

Definition 3: A transient-delay fault (late edge) sensitive latch is a latch in which a transient delay may lead to a soft error. Otherwise, the latch is called transient delay insensitive. In other words, a transient delay never causes a soft error in a transient delay insensitive latch.

Definition 4: SET-setup time (t_{SETs}) is the time that the data input of a storage cell must be valid before the sampling window so that any transient delay (late edge) on the input of the storage cell cannot be latched in the storage cell (Figure 2-I).

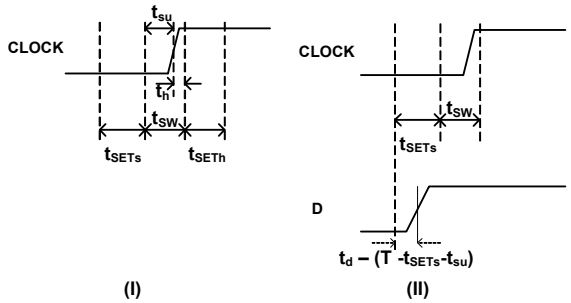


Figure 2 SET-setup time and SET-hold time

Lemma 2: The SET-setup time is equal to $\tau_{\max}$ (*i.e.*, the maximum width of SET).

Definition 5: SET-hold time (t_{SETh}) is the time that the data input of a storage cell must remain stable after the sampling window so that any early edge on the input of the storage cell cannot be latched in the storage cell (Figure 2-I).

Lemma 3: A path with propagation delay less than $\tau_{\max} + t_h$ is an early edge sensitive path.

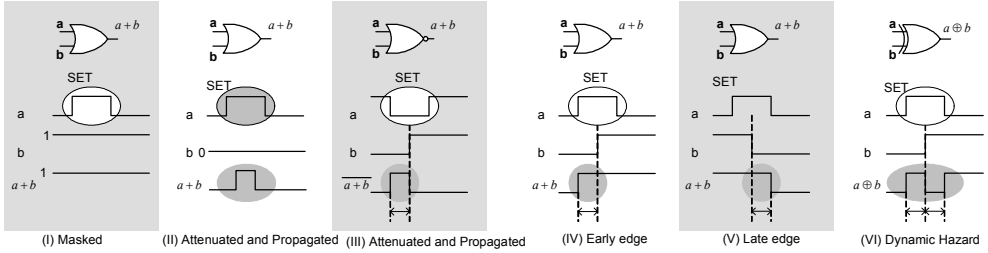


Figure 3 Transient pulse propagation mechanisms

Lemma 4: A path is transient delay sensitive if its propagation delay (t_d) is greater than $T-(t_{SETs}+t_{su})$, where T is the period of the clock (*i.e.*, $t_d > T-(t_{SETs}+t_{su})$).

In the next section, we propose a statistical method to compute the probability of transient pulse and delay fault in nodes of a design. The probability of the transient race fault can be computed like the one for transient delay that is not considered for the sake of simplicity.

III. Overview of the method

Using statistical models, this paper models the occurrence of an SET at a combinational node of a circuit and the propagation behavior of the SET through gates. In addition, the paper analyzes the probability of soft-errors in the circuit by using the proposed statistical models. For this purpose, we follow the steps below:

Step 1: *Statistical Transient Fault Model* (STFM): in which we propose a statistical model for transient pulse and transient delay faults. This model uses two random variables to represent the time that SET occurs and its duration.

Step 2: *Statistical Pulse Propagation Model* (SPPM): in which we propose a statistical model to propagate an SET through gates in a combinational path considering the probability of electrical and logical masking phenomena.

Step 3: *Temporal Masking Model* (TMM): in which a statistical manner propose to compute the temporal masking effect.

Step 4: *Soft-error Probability Algorithm* (SPA): in which we propose an algorithm to propagate the SET occurs at a combinational node towards downstream storage elements and consequently compute the soft-error probability by using the proposed statistical model.

The next section explains these steps in details.

IV. Statistical Analysis

Step 1: Statistical Transient Fault Model

Transient pulse: A transient pulse has a statistical behavior and can be represented using two independent random variables: random variable X that shows the starting point of the transient pulse, and random variable W that represents the pulse width of the transient pulse. If T shows the clock period of the circuit (Figure 4-a) then $-T+t_{hold} < X < t_{hold}$ and because we assume that the maximum transient pulse is $\tau_{\max}$ then $0 < W \le \tau_{\max}$. We also assume that the two random variables X and W are independent, thus the probability density function of the transient pulse is separable, that is $f_{X,W}(x,w) = f_X(x) f_W(w)$.

Transient delay: a transient delay on a node of a circuit can be modeled by merging a transient pulse and a normal transition on that node. Figure 4-b shows this idea; thus like the previous case, a transient pulse, which is called *virtual* transient pulse, models the transient delay fault.

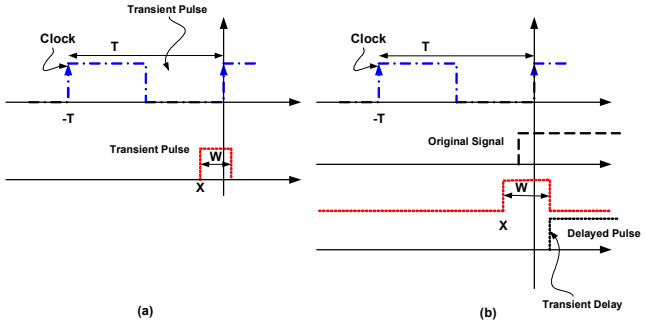


Figure 4 Statistical model of transient pulse

PDF of the transient pulse: the exact form of the transient pulse PDF is related to many factors. Obtaining the noise distributions have been the target of many published works [10] and is beyond the scope of this work. However we assume a normal distribution for the width of this pulse and a uniform distribution for the time at which the pulse is occurred (Equ. 2). Note that the proposed method can be expanded for other PDFs.

$$f_X(x) = \frac{1}{T} \qquad -T + t_{hold} < x < t_{hold}$$

$$f_W(w) = \frac{1}{\sigma_P \sqrt{2\pi}} \exp\left(-\frac{(w-\mu_P)^2}{2\sigma_P^2}\right) \qquad 0 < W \le \tau_{\max} \qquad \text{Equ. 2}$$

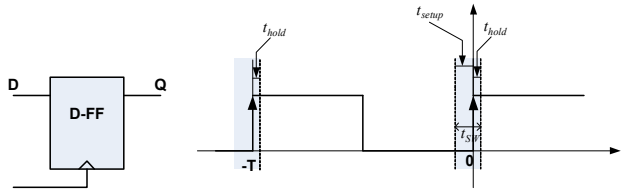


Figure 5 Sampling window of a flip-flop

Step 2: Statistical Pulse Propagation Model

Strength of the pulse will degrade as it passes through a logic gate. Pulses wider than the logic transition time of a gate will propagate through the gate without attenuation. Pulses smaller than transition time of a gate will be attenuated. In addition to the pulse width, the amplitude of the pulse should be more than the logic threshold of the gate. If the pulse width is measured at the logic threshold of gates then the amplitude can be ignored since we know that it is sufficient to make a transition at the gate output. We construct a model for electrical masking based on the propagation delay of an electrical signal through a logic gate.

Electrical masking

When a transient pulse caused by particle strike passes through a gate, its duration is changed. Using the model proposed in [7], Equ. 3 computes the duration of the SET at the output of the gate with respect to the duration of the SET at the input of that gate.

$$w_o = \begin{cases} 0 & if \;\; w_i < d \\ 2(w_i - d) & if \;\; d < w_i < 2d \\ w_i & if \;\; w_i > 2d \end{cases} \qquad \text{Equ. 3}$$

where d is the propagation delay of the gate.

To statistically analyze the propagation probability of an occurred SET at the input of a gate, it is adequate to compute the Probability Density Function (PDF) of the SET duration at the output of the gate (*i.e.,* random variable W_o) with the respect to PDF of the SET duration at the input (*i.e.,* random variable W_i).

Considering the width of an SET propagating through a gate, the gate has three different effects on its width (Equ. 3). Therefore, based on Equ. 3, the PDF of the propagated SET has three distinct parts:

- Small SETs at the input of a gate are vanished at the gate output. Thus, the PDF corresponding to these SETs at the output is zero.
- For SETs with the medium width, the PDF of the output SET is the scaled and shifted PDF of the corresponding SET at the input.
- Finally, large SETs propagate through the gate without any distortion in their PDF.

Assuming the normal distribution for the generated SET caused by particle strike at a node, and using Figure 6, we explain the PDF propagation through gates, which do not logically mask the SET.

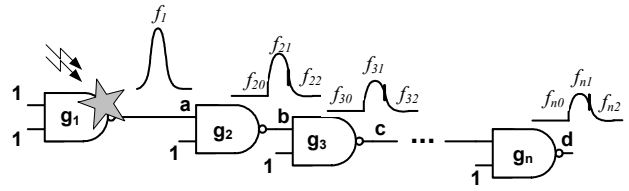


Figure 6 PDF Propagation

Let's assume the output Gate *g1* is changed temporarily due to particle strikes and its PDF is as follow:

When this PDF propagates through Gate *g2*, the output PDF has three parts, in which PDF is zero for $w_2<0$ (f_{20}), PDF is scaled and shifted for $0<w_2<2d$ (f_{21}), and PDF is unchanged for $w_2>2d$ (f_{22}). Equ. 5 shows the resulted PDF.

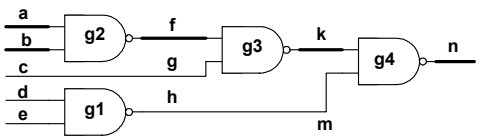
Using the similar scheme, Equ. 6 and Equ. 7 show the PDF of the propagated SET at the output of Gate g_3 and Gate g_n, respectively.

Transient delay: in the event of the transient delay, because the transient delay has only one edge, the delay of gates has no effect on its PDF. This can be modeled by keeping unchanged the PDF of the propagating virtual transient pulse. On the other hand, for transient delay $f'_{W_o}(w_o) = f_{W_i}(w_o)$.

Logical masking

When an SET passes a gate with a controlling value on one of its free-SET inputs, then the SET is masked by that gate. This masking phenomenon is called logical masking. Because complete evaluation of logical masking needs exploration of all input patterns of the circuit, as an alternative, we developed a logic path tracing technique like [8] to calculate the probability of each logic value on a node of a circuit to be used to determine the probability of transient pulse and delay propagating from that node to flip-flops through logic paths. In this technique, the probability of logic "1" and "0" is computed for each node of the circuit. Furthermore, to evaluate the occurrence of transient delay faults, the probability of $1\rightarrow0$ (which is shown by $\overline{D}$) and $0\rightarrow1$ (which is shown by D) transitions should be computed for nodes on transient delay sensitive paths. This can be achieved by using the traditional D calculus during the logic path tracing.

The proposed technique computes the probability for node N being logic "1" or "0", that are denoted by $P_N(1)$, $P_N(0)$, respectively. In addition, the probability for node M along the transient delay sensitive path being "D", "$\overline{D}$", that denoted by $P_M(D)$ and $P_M(\overline{D})$, respectively. For primary inputs that are not on the transient delay sensitive paths, we assume $P_N(1)=P_N(0)=1/2$, and for primary inputs that are on the transient delay sensitive paths, we assume $P_N(1)=P_N(0)=P_M(D)=P_M(\overline{D})=1/4$. Figure 7 illustrates how these probabilities can be competed.



$P_a(0)=P_b(0)=¼$ $P_f(1)=P_a(0)+P_b(0)-P_a(0)P_b(0)+P_a(\overline{D})P_b(D)+P_a(D)P_b(\overline{D})=9/16$
$P_a(1)=P_b(1)=¼$ $P_f(0)=P_a(1)P_b(1)=1/16$
$P_a(\underline{D})=P_b(\underline{D})=¼$ $P_f(D)=P_a(1)P_b(\overline{D})+P_a(\overline{D})P_b(1)+P_a(\overline{D})P_b(\overline{D})=3/16$
$P_a(\overline{D})=P_b(\overline{D})=¼$ $P_f(\overline{D})=P_a(1)P_b(D)+P_a(D)P_b(1)+P_a(D)P_b(D)=3/16$
$P_c(0)=P_d(0)=P_e(0)=½$ ...
$P_c(1)=P_d(1)=P_e(1)=½$

Figure 7 Example of static logic path tracing technique

When an SET generates at the node or passes through a logic gate, there are eight cases in shapes of the resulted SET. The SET can be masked, propagated, attenuated, or converted to transient delay or race faults. Note that, the cases of existing a transition on one of the gate inputs should be considered only for transient delay sensitive paths. For the sake of simplicity, we assume that in cases 1 and 2 of Figure 8, the SET pulse propagates without attenuation. In this way, an upper limit is computed for the possible soft-error probability. In addition, the early edge (i.e., case 4 of Figure 8) may have erroneous effect only in early edge sensitive path.

$$f_1(w_1) = \frac{1}{\sigma_{P1}\sqrt{2\pi}} \exp\left(-\frac{(w_1-\mu_{P1})^2}{2\sigma_{P1}^2}\right) \quad \text{Equ. 4}$$

$$f'_2(w_2)=\begin{cases} f_{20}=0 & if\ \ w_2<0\ (i.e.,w_1<d) \\ f_{21}=\dfrac{1}{2\sigma_{P1}\sqrt{2\pi}}\exp\left(-\dfrac{(w_2+2d-2\mu_{P1})^2}{8\sigma_{P1}^2}\right) & if\ 0<w_2<2d\ \ (i.e.,d<w_1<2d) \\ f_{22}=\dfrac{1}{\sigma_{P1}\sqrt{2\pi}}\exp\left(-\dfrac{(w_2-\mu_{P1})^2}{2\sigma_{P1}^2}\right) & if\ w_2>2d\ (i.e.,w_2>d) \end{cases} \quad \text{Equ. 5}$$

$$f'_3(w_3)=\begin{cases} f_{30}=0 & if\ \ w_3<0\ (i.e.,w_1<d+\dfrac{d}{2}) \\ f_{31}=\dfrac{1}{4\sigma_{P1}\sqrt{2\pi}}\exp\left(-\dfrac{(w_3+6d-4\mu_{P1})^2}{32\sigma_{P1}^2}\right) & if\ 0<w_3<2d\ (i.e.,d+\dfrac{d}{2}<w_1<2d) \\ f_{32}=\dfrac{1}{\sigma_{P1}\sqrt{2\pi}}\exp\left(-\dfrac{(w_3-\mu_{P1})^2}{2\sigma_{P1}^2}\right) & if\ w_3>2d\ (i.e.,w_1>2d) \end{cases} \quad \text{Equ. 6}$$

$$f''_n(w_n)=\begin{cases} f_{n0}=0 & if\ \ w_n<0\ (i.e.,w_1<d+\dfrac{d}{2}+\ldots+\dfrac{d}{2^{n-1}}) \\ f_{n1}=\dfrac{1}{2^{n-1}\sigma_{P1}\sqrt{2\pi}}\exp\left(-\dfrac{(w_n+(2^n-2)d-2^{n-1}\mu_{P1})^2}{2^{2n-1}\sigma_{P1}^2}\right) & if\ 0<w_n<2d\ \ (i.e.,\ d+\dfrac{d}{2}+\ldots+\dfrac{d}{2^{n-1}}<w_1<2d) \\ f_{n2}=\dfrac{1}{\sigma_{P1}\sqrt{2\pi}}\exp\left(-\dfrac{(w_n-\mu_{P1})^2}{2\sigma_{P1}^2}\right) & if\ w_n>2d\ (i.e.,\ w_1>2d) \end{cases} \quad \text{Equ. 7}$$

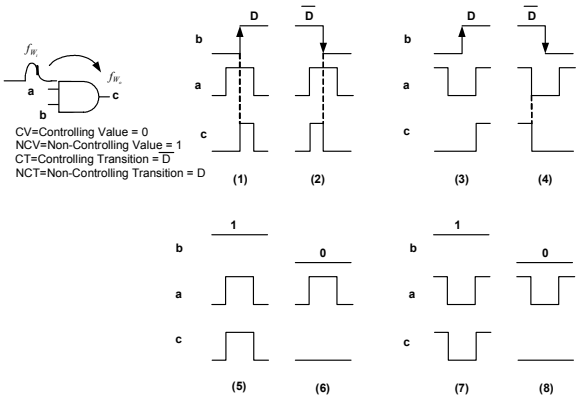


Figure 8 Different shapes of propagating transient pulse

When a transient pulse appears on one of the inputs of a gate which located in a transient delay insensitive path, it propagates to the gate output if other inputs of the gate have the non-controlling value (*NCV*). Let's consider the gate of Figure 8, and assume it is on a transient delay insensitive path, then Equ. 8 computes the PDF of the gate output, if there is a transient pulse at the input *a* of gate. This equation represents the cases 5 and 7 of Figure 8. In this equation, $f_{W_o}(w_o)$ is the PDF of the gate output, $P(NCV_b)$ is the probability that a non-controlling value is on the input *b*, and $f'_{W_o}(w_o)$ is the PDF at the gate output considering only electrical masking effect.

$$f_{W_o}(w_o)=P(NCV_b)\times f'_{W_o}(w_o) \quad \text{Equ. 8}$$

$$f_{W_o}(w_o)=\left[P(NCV_b)+P(NCT_b)P(CV_a)\right]\times f'_{W_o}(w_o) \quad \text{Equ. 9}$$

$$f_{W_o}(w_o)=P(NCT_b)P(NCV_a)\times f_{W_i}(w_o) \quad \text{Equ. 10}$$

If the gate of Figure 8 is on a transient delay sensitive path, in the cases of 1, 5, and 7 the transient pulse at the input propagates to the output. Equ. 9 represents these cases. On the other hand, in Case 3, the transient pulse is converted to the transient delay that Equ. 10 computes the output PDF for this case. Note that, a transient delay at an input of the gate can be propagated to the output if the other input of the gate has the no-controlling value of the gate; thus Equ. 8 can be used to compute the output PDF.

Step 3: Temporal masking model

An SET appeared at the data input of a flip-flop can be erroneously latched in that flip-flop if it appears in the sampling window of the flip-flop. Sampling window of a latch (t^i_{SW} : sampling window of latch *i*) is the time that is bounded by the setup time (t^i_{setup}) and hold time (t^i_{hold}) around the active clock edge of a flip-flop.

A transient pulse occurs in the window sampling, if $-t_{setup}<X+W<0\wedge X<t_{hold}$, Thus, the probability of soft-error is:

$$P(SET)=P(-t_{setup}<X+W<0\wedge X<t_{hold})$$

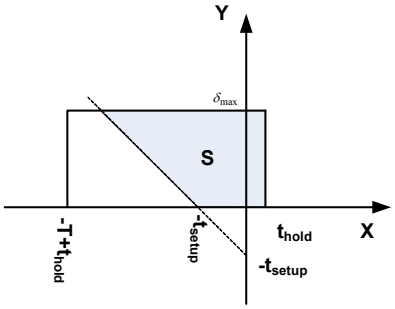


Figure 9 Space of random variables that lead to a soft error

We consider that the pulse width caused by a particle strike has a normal distribution with mean=μ_P and standard deviation= σ_P. Then,

$$P(SET)=\iint_S \frac{1}{T}\times\frac{1}{\delta_P\sqrt{2\pi}}\exp\left(-\frac{(y-\mu_P)^2}{2\sigma_P^2}\right)dxdy$$

Step 4: Soft-Error Probability Algorithm

In this step, inserting a PDF of a transient pulse at each node of the circuit and using the PDF propagation rules described in previous steps, the resulted PDFs at the input of flip-flops are obtained. Then using the temporal masking model, the proposed method computes the probability of

soft error due to particle strike in different node of the circuit. Algorithm 1 shows this probability computation method.

```
1   Determine transient delay sensitive path
2   Compute the probability of node values for logical
        masking considerations
3   For each node in the circuit
4       Assign PDF of a generated SET to a node
        For each gate in the path to downstream flip-flops
5           Compute the PDF of the gate output by using the
            logical and electrical PDF propagation rules,
6   Compute the sum of PDFs at the flip-flop inputs
7   Compute the probability of soft-error by using the temporal
    masking condition
```

Algorithm 1 computing the soft-error probability

V. Experimental Results

We evaluate our proposed method by comparing the results obtained by the proposed method and SPICE simulation. For this purpose, we have considered C17 circuit (one of the ISCAS85 benchmark) that is shown in Figure 10.

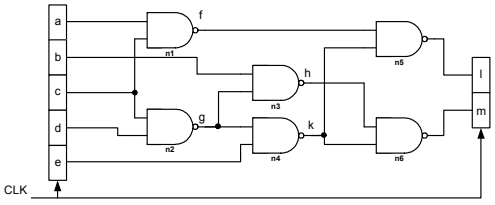


Figure 10 An example circuit

To compute the maximum width of the generated transient voltage pulse caused by particle stick, we have used the technology parameters of [11] that are shown in the Columns 2, 3, and 4 of Table 1. Column 5 of this table shows the assumption of W/L of transistors. The delay of a NAND gate and the maxim width of the transient pulse that are computed by HSPICE simulation are shown in Columns 6 and 7.

Table 1 Technology parameters

Tech.	τ_α ns	τ_β ns	Q pC	$(W/L)_n$, $(W/L)_p$	d ps	τ_{max} Ps
180nm	0.20	0.05	0.2	4,8	43	341
130nm	0.20	0.05	0.2	4,8	36	412
100nm	0.20	0.05	0.2	4,8	22	477
70nm	0.20	0.05	0.2	4,8	14	546

In HSPICE simulation, we have inserted several transient current pulses at Node *g* (as a model of SET caused by particle strike) using technology parameters of Table 1. These current sources are considered with different width at different time during a period of clock. The second column of Table 2 shows the obtained probability of soft-error caused by these inserted SETs at Node *g*. Note that, multiplying this probability to the SET rate at Node g, we can compute the soft error rate in the circuit due to SETs at this node. The third column shows the corresponding probability obtained by our method.

Table 2 Technology parameters

	Probability of Soft-Error%	
Tech.	HSPICE	Our Method
180nm	18.9	18.7
130nm	20.5	21.3
100nm	35.7	32.4
70nm	57.7	59.4

VI. Conclusions

This paper studies the effect of single event transient (SET) caused by particle strike on the nodes along the combinational paths. Two different behaviors of the SET, *i.e.,* transient pulse and delay faults are considered in this paper. Propagating the probability density function of an occurred SET at a node along the combinational path, the proposed method computes the probability of soft-error cased by this SET.

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