A P4VT (Power-Performance-Process-Parasitic-Voltage-Temperature) Aware Dual-V_{Th} Nano-CMOS VCO

Saraju P. Mohanty[1], Dhruva Ghai[2], and Elias Kougianos[3]
Department of Computer Science and Engineering, University of North Texas, USA.[1,2]
Department of Engineering Technology, University of North Texas Denton, TX 76203.[3]
Email-ID: saraju.mohanty@unt.edu[1], dvg0010@unt.edu[2], eliask@unt.edu[3].

Abstract

We present the design flow for a P4VT (Power-Performance-Process-Parasitic-Voltage-Temperature) aware voltage controlled oscillator (VCO). Through simulations, we have shown that parasitics, process, voltage and temperature have a drastic effect on the performance (center frequency) of the VCO. A design optimization of the VCO, along with dual-threshold power minimization has been performed in the presence of worst-case variations. The end product of the proposed methodology is a P4VT-optimal dual-threshold $90nm$ *VCO layout. We have achieved* 16.4% *power (including leakage) minimization with* 10% *degradation in center frequency compared to the target frequency, in the presence of* worst-case *variations.*

1 Introduction

The Radio Frequency Integrated Circuits (RFICs) must be simultaneously low power and high performance. As power dissipation increases, the cost of power delivery to the ever-increasing number of transistors on a chip multiplies rapidly. Minimum power expenditure is expected while meeting performance requirements.

The impact of process variation on performance of a RFIC is severe for nanometer technologies [9]. Just as in digital design where interconnect delays make or break a design, the move to sub-$90nm$ technologies means that the variations in process parameters have a significant effect on the performance of analog/mixed-signal and RF circuits.

The numerous parasitic effects induced by layout, especially for high performance circuits, pose a problem for RFIC design. Lack of exact layout information during circuit sizing leads to long design iterations involving time consuming runs of complex tools. The traditional IC design flow involves repetitive iterations of circuit sizing, layout generation, parasitic value extraction, and performance evaluation. Redesign is needed whenever the final performance does not meet to the specification. To improve design efficiency and reduce the time-to-market, it is crucial to be able to predict parasitic effects for accurate performance.

The effect of on-die temperature variation is one critical issue in nano-CMOS RFIC design. It interacts with a number of these other issues in ways that make analysis difficult. There is a need for new, temperature-aware design methodologies in order to produce properly functioning and reliable first silicon. The challenge for RF design is the centering of a design including PVT variations [6]. By integrating temperature-aware capabilities into today's design flows, there is no need to reinvent established analysis standards. Instead, through the use of tools that retrofit today's flows with temperature aware data, the temperature effects can be fully accounted.

A voltage-controlled oscillator or VCO is an electronic oscillator designed to be controlled in oscillation frequency by a voltage input. It is an important RFIC block used in applications such as clock recovery circuits for serial data communications, disk-drive read channels, on-chip clock distribution, and integrated frequency synthesizers [16]. VCOs are required to be designed in the GHz-Range for applications such as radio frequency transceivers.

The *distinct contributions of this paper* are as follows:

1. A P4VT-aware design flow for nano-CMOS RFICs.
2. Judicious use of dual-threshold process-level technique for power optimization of nano-CMOS VCO.
3. Design of a P4VT-optimal $90nm$ VCO.

The rest of the paper is organized as follows: Related prior research are discussed in Section 2. The P4VT flow is discussed in Section 3. Section 4 discusses the baseline design of VCO. The process variation analysis is discussed in Section 5. P4VT optimization is presented in Section 6. The paper is concluded in Section 7.

[0]This research is supported in part by NSF award numbers CCF-0702361 and CNS-0854182, and SRC award number P10883.

2 Related Prior Research

In [18], the authors propose novel circuit level techniques using adaptive supply/body-bias voltage generating technique for PVT-variation tolerant designs. In [4], an operational amplifier used in switch capacitor integrators is designed using corner analysis for PVT awareness. A all-digital-PLL for fast frequency acquisition is proposed in [17], where the digital controlled oscillator codeword is predicted by measuring the PVT variations. A PVT-tolerant digital PLL has been reported in [11]. An LC-VCO has been designed in [10], which uses automatic amplitude control to minimize influence of PVT variations. A PVT tolerant PLL architecture which uses two on-chip digital calibration circuits to maintain loop transfer function is presented in [19]. A comparison of this paper with existing literature (Table 1) reveals the design to be low power and high-performance. A P4-optimal VCO is presented in [14]; however, thermal (temperature) effects were not accounted.

Table 1. VCO performance comparison

Reference	Technology	Performance	Power
Troedsson [28]	$250nm$	2.4GHz	$5.5mW$
Tiebout [24]	$250nm$	1.8GHz	$20mW$
Dehghani [27]	$250nm$	2.5GHz	$2.6mW$
Long [22]	$180nm$	2.4GHz	$1.8mW$
Kwok [21]	$180nm$	1.4GHz	$1.46mW$
Ghai [14]	$90nm$ dual-T_{ox}	2.3GHz	$158\mu W$
Ghai [12]	$90nm$	2.54GHz	$--$
This Paper	$90nm$ dual-V_{Th}	2.4GHz	$137.5\mu W$

Due to high sensitivity of RFIC design to layout parasitics, there is a significant amount of research in the area of parasitic aware synthesis to overcome parasitic degradations and achieve optimal performance [26, 2]. Simulated annealing is proposed for synthesizing RF power amplifiers in [5]. Particle swarm optimization techniques are proposed for parasitic aware design in [7]. In [8], an LC-VCO has been subjected to parasitic-aware synthesis. A parasitic and process aware design flow has been proposed in [12]. In [20], the center frequency of a VCO has been optimized using a Design of Experiments (DOE) approach. The simulation-based circuit synthesis example in [29] does not include the layout parasitics in the design.

Process variation in analog circuits [3] and power aware design are on the research forefront now. In [25], an analysis of the process parameters affecting a ring oscillator's frequency performance is done. In [9], a current-controlled oscillator has been subjected to process variations. In [13], the authors propose a dual-oxide technique for power and delay optimization at circuit level but do not address temperature effects. In [23], the authors have shown the effect of simultaneous variation of supply and process parameters on power consumption of datapath components.

3 P4VT Aware Design Flow

The P4VT design flow in Fig. 1 accounts for parasitic, process, power, performance, voltage and temperature.

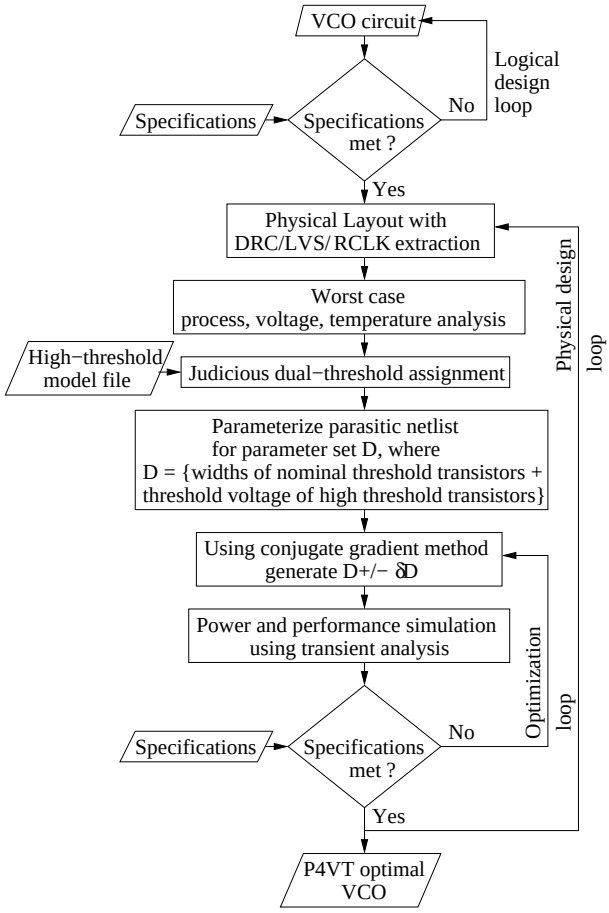
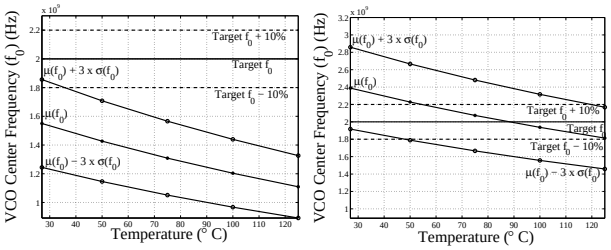


Figure 1. The P4VT-Optimal Design Flow.

First, the logical design is performed to meet the required center frequency (target f_0) specification of $f_0 \geq 2$ GHz. Using the device dimensions from the logical design, a preliminary physical design is prepared and is subjected to Design Rule Check, Layout vs. Schematic, and parasitic extraction. A worst-case variability analysis of the parasitic extracted preliminary physical design with respect to center frequency is carried out, where the worst-case process-variation is identified. Fig. 2(a) shows the behavior of VCO center frequency (f_0) with respect to temperature (measured at 27°C, 50°C, 75°C, 100°C and 125°C). The VCO is subjected to process-voltage variations at each of these temperatures. Hence, we can observe the behavior of the $\mu(f_0)$, $\mu(f_0) + 3 \times \sigma$ and $\mu(f_0) - 3 \times \sigma$ with temperature (μ = mean, σ = standard deviation). It is clear from Fig. 2(a), that the center frequency moves away from the target f_0 (reduces) with increase in temperature.



(a) Non-optimized VCO (b) P4VT optimized

Figure 2. Center frequency Vs. temperature.

This is followed by high-threshold voltage assignment (HV_{Thn},HV_{Thp}) to the power-hungry transistors (NMOS, PMOS) of the VCO. The rest of the transistors in the circuit operate on nominal threshold voltage. We call this technique "judicious dual-threshold assignment", used to minimize the power dissipation of the VCO circuit. The dual-threshold technique is an effective means for minimizing the power of a circuit, where high-threshold transistors consume less power than low-threshold transistors. However, high-threshold transistors are slower than low-threshold transistors and cause the speed of the circuit (VCO oscillation frequency) to decrease. The effects of dual-threshold assignment on digital circuits is discussed in [23].

The netlist obtained from the preliminary physical design, including full parasitics, is then parameterized for a parameter set D (widths of transistors and HV_{Thn}, HV_{Thp}). We call this "parameterized parasitic netlist". The parameterized parasitic netlist is then subjected to optimization in order to meet the specifications (performance, power) in a worst case PVT environment. Once the parameter values for which the specifications are met are obtained, a final physical design of the VCO is created using these parameter values. Hence we obtain a P4VT optimal dual-threshold VCO layout from the proposed design flow. From figure 2(b), we can observe that f_0 meets the target specifications of $f_0 \geq$2GHz (with a 10% degradation at worst case) *across the entire specified temperature range.*

4 Transistor Level Design of the VCO

The current-starved VCO design comprises of three stages [1]: (1) input stage consisting of two transistors with high impedance, (2) an odd numbered chain of inverters along with two current source transistors per inverter, which limit the current flow to the inverter, and (3) buffer stage. The operating frequency of the VCO is given by [1]:

$$f_0 = \left(\frac{1}{N \times T_t}\right) = \left(\frac{I_{inv}}{N \times C_t \times V_{DD}}\right), \qquad (1)$$

where V_{DD} is the supply voltage, I_{inv} is the current flowing through each inverter, N is the odd number of inverters in the VCO circuit, T_t is the total time required to charge or discharge the capacitance of each stage of an inverter and C_t is the total capacitance given by the sum of the input and output capacitances of the inverter. f_0 can be mainly controlled by an applied DC input voltage, which adjusts the current I_{inv} through each inverter stage. When the applied DC voltage is half of the supply voltage (V_{DD}), the oscillation frequency is called center frequency.

The target specification for this design is the center frequency which has been kept at a minimum of $2GHz$. The number of stages is fixed to 13 for high frequency operation. For baseline design, we have chosen $L_n = L_p = 100nm$, $W_n = 250nm$ and $W_p = 2 \times W_n = 500nm$. I_{inv} is calculated using equation 1, and the current starved NMOS and PMOS devices are sized to provide the required current I_{inv}. Thus we obtained $L_{ncs} = L_{pcs} = 100nm$, and $W_{ncs} = 500nm$ and $W_{pcs} = 10 \times W_{ncs} = 5\mu m$, where W_{ncs} and W_{pcs} are the widths and L_{ncs} and L_{pcs} are the lengths of the current-starved NMOS and PMOS transistors, respectively.

The preliminary physical design of the VCO uses these transistor sizes. The layout has an area of $228.43\mu m^2$.

5 Process-Voltage Variation Analysis of VCO

For process-voltage variation, we have considered variation in 5 parameters, namely: (1) V_{DD}: Supply voltage, (2) V_{Thn}: NMOS threshold voltage, (3) V_{Thp}: PMOS threshold voltage, (4) T_{oxn}: NMOS gate oxide thickness, (5) T_{oxp}: PMOS gate oxide thickness. A correlation coefficient (cc) of 0.9 is assumed between T_{oxn} and T_{oxp}. Each of these process parameters is assumed to have a Gaussian distribution with μ the nominal value specified in the process design kit, and a σ of 10%. The VCO is subjected to Monte Carlo simulations for 1000 runs at temperature T, where T = $27°C$, $50°C$, $75°C$, $100°C$ and $125°C$.

At $27°C$ (room temperature), the center frequency (f_0) is observed to have a Gaussian distribution with $\mu = 1.54GHz$ and $\sigma = 103.5MHz$, as shown in Fig. 3.

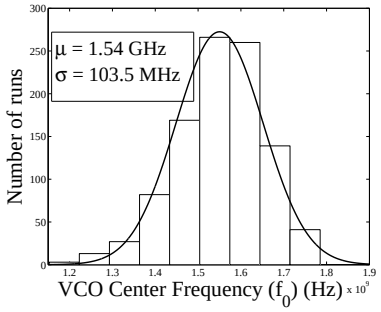


Figure 3. Distribution of f_0 at $27°C$.

The worst case process for f_0 is identified to be the one where process parameters (V_{Thn}, V_{Thp}, T_{oxn}, T_{oxp}) are increased by 10%. The worst case voltage is where V_{DD} is reduced by 10%. The worst case temperature is $125°C$.

6 P4VT Optimization of the VCO

In this section, we demonstrate how the performance (f_0) discrepancy is overcome along with power minimization of the VCO using a dual-threshold technique. After full extraction ($RCLK$), a 22% degradation in the performance (center frequency) is observed between the preliminary physical design and target frequency. Furthermore, a 50% discrepancy is observed between the preliminary physical design and target frequency when the VCO is subjected to *worst case process-voltage-temperature* (wcPVT) (Section 5). Details results are presented in Table 2.

Table 2. Performance discrepancy and worst-case process values for a target $f_0 \geq 2GHz$.

Parameter	Preliminary Physical Design	Preliminary Physical Design + wcPVT	Final Physical Design + wcPVT
f_0	$1.56GHz$	$1GHz$	$1.8GHz$
discrepancy	22%	50%	10%
V_{DD}	$1.2V$ (nominal)	$1.08V$ (-10%)	$1.08V$
V_{Thn}	$0.1692662V$ (nominal)	$0.186193V$ $(+10\%)$	$0.186193V$
V_{Thp}	$-0.1359511V$ (nominal)	$-0.149546V$ $(+10\%)$	$-0.149546V$
T_{oxn}	$2.33nm$ (nominal)	$2.563nm$ $(+10\%)$	$2.563nm$
T_{oxp}	$2.48nm$ (nominal)	$2.728nm$ $(+10\%)$	$2.728nm$

In summary, the following results are obtained:

- Target center frequency $f_0 \geq 2GHz$.
- Preliminary Physical design center frequency $f_{0\mathrm{p}}$ = $1.56\,GHz$.
- Preliminary Physical design center frequency in worst case PVT conditions $f_{o\mathrm{pvt}}$ = $1GHz$.
- Initial average power consumption (including leakage) (P_{VCO}) = $164.5\mu W$.

6.1 Judicious Dual-Threshold Assignment

A transient analysis is run on the physical design of the VCO, and the average power consumed by all the transistors is measured. The input stage transistors (solid circles in Fig. 4) collectively consume 48% of the total average power of the VCO circuit, hence are most suitable candidates for higher threshold voltage assignment (HV_{Thn}, HV_{Thp}). The buffer stage transistors (dashed circles in Fig. 4) consume 11.5% of the total average power, and hence may be treated to higher threshold voltage, for power minimization. In this paper, we have subjected the input stage transistors to dual-threshold assignment. These transistors are assigned a high threshold while the other transistors in the VCO circuit follow the baseline process value.

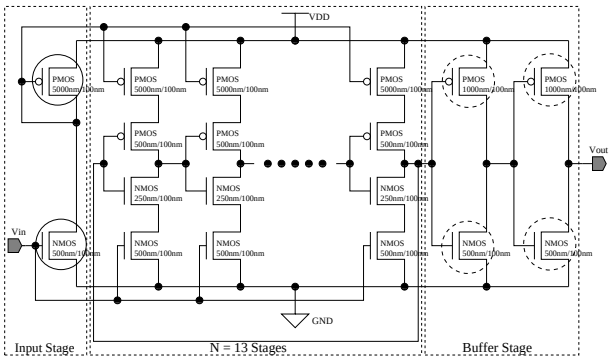


Figure 4. Candidate transistors for High-V_{Th}.

6.2 Parameterizing the Parasitic Netlist

Following the dual-threshold assignment, the parasitic-aware netlist generated from the preliminary physical design is then taken and parameterized with respect to the optimization parameters. The parameter set includes the widths of PMOS and NMOS devices in the inverter (W_n, W_p), the PMOS and NMOS devices in the current-starved circuitry (W_{ncs}, W_{pcs}), and HV_{Thn}, HV_{Thp}.

6.3 Power-Performance Optimization

The parameterized netlist is subjected to optimization using a conjugate gradient method, where the parameter set takes on different values, till the specifications are met. The conjugate gradient method is an algorithm for the numerical solution of systems of linear equations offering the advantages of low memory requirements and faster convergence [15]. The candidates for optimization are the widths of the inverters (W_n, W_p) and current-starved transistors (W_{ncs}, W_{pcs}), and the threshold voltages (HV_{Thn}, HV_{Thp}) of high-threshold (input stage) transistors. While the higher threshold voltages minimize power consumption of the VCO, the higher widths of the devices maximize performance. Our objective set are $f_0 \geq 2GHz$, and $P_{VCO} = minimum$. The optimization approach is shown in Algorithm 1. Table 3 shows the final values of the parameter set for P4VT optimal VCO. S is the stopping criteria for

the optimization to stop when the objective set is within $\pm\epsilon$ (where ϵ is error percentage). The outputs of the algorithm are the optimized objective set F_{opt} which satisfies the stopping criteria S, and the optimal values of the design variable set D_{opt} within the upper and lower design constraints. The algorithm starts out with a guess of D, and then it iterates to improve the guess, until the guess is close enough, and the objective set F_{opt} is met with the stopping criteria S.

Algorithm 1 Power-Performance optimization of the VCO.

1: **Input:** Parasitic Aware netlist, Worst case PVT settings, Objective set $F = [f_0, P_{VCO}]$, Stopping criteria S, Parameter set $D = [W_n, W_p, W_{ncs}, W_{pcs}, HV_{Thn}, HV_{Thp}]$, Lower/Upper parameter constraint C_{low}/C_{up}.
2: **Output:** Optimized objective set F_{opt}, Optimal parameter set D_{opt} for stopping criteria $S \leq \epsilon$. {where $\epsilon = 10\%$}
3: Perform first iteration with initial guess of D.
4: **while** ($C_{low} < D < C_{up}$) **do**
5: Use conjugate gradient to generate D' = $D \pm \Delta D$ in the direction of travel of $F_{opt} \pm \epsilon$.
6: Compute $F(D')$ = [f_0, P_{VCO}].
7: S is the difference of target and current objective set.
8: **if** $S \leq \epsilon$ **then**
9: **return** D_{opt} = D'.
10: **end if**
11: **end while**
12: Using D_{opt}, construct final physical design and simulate.

Table 3. Optimized values of the parameters.

D	C_{low}	C_{up}	D_{opt}
W_n	$200nm$	$500nm$	$390nm$
W_p	$400nm$	$1\mu m$	$445nm$
W_{ncs}	$1\mu m$	$50\mu m$	$10\mu m$
W_{pcs}	$5\mu m$	$50\mu m$	$30\mu m$
HV_{Thn}	$0.1692662V$	$0.5V$	$0.5V$
HV_{Thp}	$-0.5V$	$-0.1359511V$	$-0.4975V$

The final physical design of the VCO uses these parameter values for which the following results are obtained:

- Target center frequency $f_0 \geq 2GHz$.
- Final physical design center frequency $f_{0\mathrm{p}} = 2.4\,GHz$.
- Final physical design center frequency in a worst case PVT conditions $f_{0\mathrm{pvt}} = 1.8\,GHz$.
- Final average power consumption (including leakage) (P_{VCO}) = $137.5\mu W$

Hence we obtained a final optimized dual-threshold layout, with $1.8\,GHz$ center frequency under worst case variations, and $2.4GHz$ center frequency in nominal process conditions and 16.4% power minimization. The conjugate gradient optimization converged in 8 iterations, with each iteration typically lasting 4 minutes.

6.4 P4VT-Optimal Dual-V_{Th} Layout

The dual-threshold physical design of the VCO is carried out using a generic 90 nm Salicide 1.2V/2.5V 1 Poly 9 Metal process design kit. At high frequencies, parasitic inductance has a major impact on chip performance. Hence it is necessary to extract self (L) and mutual (K) inductance so that the impact of inductive coupling could be assessed and minimized on the layout. A full extraction of the layout was carried out (including RLCK). The P4VT optimal physical design is shown in Fig. 5. It occupies an area of $547.74\mu m^2$. The final optimal widths of the P4VT optimal circuit and high threshold transistors are shown in Fig. 6.

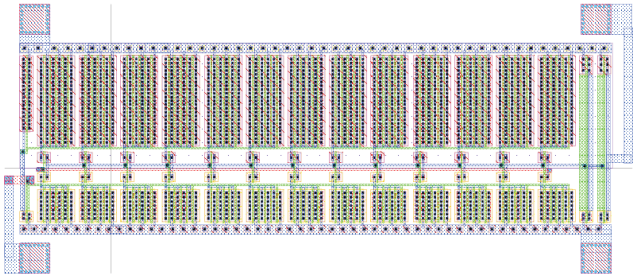


Figure 5. P4VT-optimal dual-V_{Th} VCO layout.

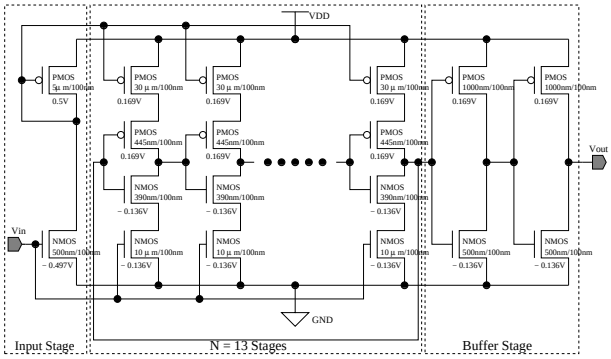


Figure 6. Parameters of P4VT-optimal VCO.

The performance summary of the VCO is given in Table 4. It can be seen that the target frequency is met within a 10% discrepancy even at the worst case PVT settings. The resulting physical design, however, incurs a 58.3% area penalty (increase) over the preliminary physical design.

7 Conclusions and Future Research

We presented a novel design flow for a P4VT- optimal nano-CMOS VCO. The design flow can be implemented on top of existing electrical analysis and physical design tools. This provides for the analysis of temperature effects at an

Table 4. Measured performance of the VCO.

Parameter	Value
Technology	$90nm$ CMOS $1P\,9M$
Supply Voltage (V_{DD})	$1.2V$
Center frequency (Nominal PVT)	$2.4GHz$
Worst case PVT	V_{Th} ($+10\%$), T_{ox} ($+10\%$), V_{DD} (-10%), $125^{\circ}C$
Center frequency (worst case PVT)	$1.8GHz$
Parameter set	6 ($W_n, W_p, W_{ncs}, W_{pcs}$, HV_{Thn}, HV_{Thp})
Number of objectives	2 ($f_0 \geq 2GHz$, P_{VCO}=$minimum$)
Area occupied	$547.74\mu m^2$ (58.3% penalty)

early stage in the design cycle. The center frequency has been treated as the target specification. The degradation of the center frequency due to worst case PVT effects has been narrowed down from 50% to 10%, along with 16.4% power minimization. The end product of the proposed design flow is a P4VT optimal dual-threshold VCO physical design that meets the functional specifications across the entire range of expected temperatures. As part of extension of this research, we plan to incorporate additional performance criteria to the optimization set, such as phase noise.

References

[1] R. J. Baker. *CMOS: Circuit Design, Layout and Simulation*. IEEE Press, 2003.

[2] B. M. Ballweber, R. Gupta, and D. J. Allstot. A fully integrated $0.5 - 5.5GHz$ CMOS distributed amplifier. *IEEE Journal of Solid State Circuits*, 35(2):231–239, Feb 2000.

[3] S. Basu, B. Kommineni, and R. Vemuri. Variation Aware Spline Center and Range Modeling for Analog Circuit Performance. In *Proceedings of ISQED*, pages 162–167, 2008.

[4] K. Charan, et al. Design of a Humidity sensor with PVT Variations using AMI C5 CMOS Technology. In *Proc. International Conference on Recent Advances in Microwave Theory and Applications*, pages 839–842, 2008.

[5] K. Choi and D. Allstot. Parasitic-aware design and optimization of a CMOS RF power amplifier. *IEEE Transactions on Circuits and Systems I*, 53(1):16–25, January 2006.

[6] K. Choi and D. J. Allstot. Post-optimization design centering for RF integrated circuits. In *Proc. of the International Symposium on Circuits and Systems*, pages 956–959, 2004.

[7] K. Choi, J. Park, and D. J. Allstot. *Parasitic-aware Optimization of CMOS RF Circuits*. Kluwer Acad. Publi., 2003.

[8] M. Chu, D. J. Allstot, J. M. Huard, and K. Y. Wong. NSGA-based parasitic aware Optimization of a $5GHz$ Low-noise VCO. In *Proceedings of ASPDAC*, pages 169–174, 2004.

[9] D. Kim, et al. CMOS Mixed-Signal Circuit Process Variation Sensitivity Characterization for Yield Improvement. In *Proc. Custom Integrated Circuits Conf.*, pp. 365–368, 2006.

[10] D. Miyashita, et al. A Phase Noise Minimization of CMOS VCOs over Wide Tuning Range and Large PVT Variations. In *Custom Integrated Circuits Conf.*, pp. 583–586, 2005.

[11] J. Lin, et al. A PVT tolerant $0.18MHz$ to $600MHz$ self-calibrated digital PLL in $90nm$ CMOS process. In *Proc. Inter. Solid State Circuits Conf.*, pages 488–541, 2004.

[12] D. Ghai, S. P. Mohanty, and E. Kougianos. Parasitic Aware Process Variation Tolerant VCO Design. In *Proc. Inter. Sympo. Quality Electronic Design*, pp. 330–333, 2008.

[13] D. Ghai, S. P. Mohanty, and E. Kougianos. A Dual Oxide CMOS Universal Voltage Converter for Power Management in Multi-VDD SoCs. In *Proc. International Symposium on Quality Electronic Design*, pages 257–260, 2008.

[14] D. Ghai, S. P. Mohanty, and E. Kougianos. Unified P4 (Power-Performance-Process-Parasitic) Fast Optimization of a Nano-CMOS VCO. In *Proceedings of the Great Lakes Symposium on VLSI*, pages 303–308, 2009.

[15] W. W. Hager and H. Zhang. Algorithm 851: CG-DESCENT, A Conjugate Gradient Method with Guaranteed Descent. *ACM Trans. Mathematical Software*, 32(1):113–137, 2006.

[16] A. Hajimiri, et al. Jitter and Phase Noise in Ring Oscillators. *IEEE J. Solid State Circuits*, 34(6):790–804, 1999.

[17] H. S. Jeon, D. H. You, and I. C. Park. Fast frequency acquisition all-digital PLL using PVT calibration. In *Proc. Inter. Sympo. Circuits and Systems*, pp. 2625–2628, 2008.

[18] K. K. Kim and Y. B. Kim. A Novel Adaptive Design Methodology for Minimum Leakage Power Considering PVT Variations on Nanoscale VLSI Systems. *IEEE Transcations on VLSI Systems*, 17(4):517–528, April 2009.

[19] M. Kondou and T. Mori. A PVT Tolerant PLL with On-Chip Loop-Transfer-Function Calibration Circuit. In *Proc. International Sympo. VLSI Circuits*, pages 232–233, 2007.

[20] E. Kougianos and S. P. Mohanty. Impact of Gate-Oxide Tunneling on Mixed-Signal Design and Simulation of a Nano-CMOS VCO. *Microelectronics J.*, 40(1):95–103, 2009.

[21] K. Kwok and C. H. Luong. Ultra-low-Voltage high-performance CMOS VCOs using transformer feedback. *IEEE Journal of Solid State Circuits*, 40(3):652–660, 2005.

[22] J. Long, J. Y. Foo, and R. J. Weber. A 2.4 GHz Low-Power Low-Phase-Noise CMOS LC VCO. In *Proc. IEEE-CS Annual Symposium on VLSI*, page 213, 2004.

[23] S. P. Mohanty, et al. Interdependency Study of Process and Design Parameter Scaling for Power Optimization of Nano-CMOS circuits under Process Variation. In *Proc. 16th ACM Inter. Workshop on Logic and Synthesis*, pp. 207–213, 2007.

[24] M.Tiebout. Low-power low-phase-noise differentially tuned quadrature VCO design in standard CMOS. *IEEE Journal of Solid-State Circuits*, 36(7):1018–1024, July 2001.

[25] M. Nourani and A. Radhakrishnan. Testing On-Die Process Variation in Nanometer VLSI. *IEEE Design and Test of Computers*, 23(6):438–451, June 2006.

[26] J. Park, K. Choi, and D. J. Allstot. Parasitic-aware design and optimization of a fully integrated CMOS wideband amplifier. In *Proceedings of ASPDAC*, pages 904–907, 2003.

[27] R.Dehghani and S. Atarodi. Optimised analytic designed 2.5GHz CMOS VCO. *IEE Electronic Letters*, 39(16):1160–1162, August 2003.

[28] N. Troedsson and H. Sjoland. High performance 1 V 2.4 GHz CMOS VCO. In *Proceeedings of the IEEE Asia-Pacific Conference on ASIC*, pages 185–188, 2002.

[29] G. Zhang, A. Dengi, and L. R. Carley. Automatic Synthesis of a $2.1GHz$ SiGe low noise amplifier. In *Proceedings of the IEEE RFIC Symposium*, pages 125–128, 2002.