A 2-Port 6T SRAM Bitcell Design with Multi-Port Capabilities at Reduced Area Overhead

Jawar Singh, Dilip S. Aswar[1], Saraju P. Mohanty[2] and Dhiraj K. Pradhan
Department of Computer Science, University of Bristol, UK.
Department of Telecommunication, Government of India, New Delhi.[1]
Department of Computer Science and Engineering, University of North Texas, USA.[2]
Email-ID: jawar@cs.bris.ac.uk, saraju.mohanty@unt.edu

Abstract

Low power, minimum transistor count and fast access static random access memory (SRAM) is essential for embedded multimedia and communication applications realized using system on a chip (SoC) technology. Hence, simultaneous or parallel read/write (R/W) access multi-port SRAM bitcells are widely employed in such embedded systems. In this paper, we present a 2-port 6T SRAM bitcell with multi-port capabilities and a reduced area overhead compared to existing 2-port 7-transistor (7T) and 8T SRAM bitcells. The proposed 2-port bitcell has six transistors (6T) and single-ended read and write bitlines (RBL/WBL). We compare the stability, simultaneous read/write disturbance, SNM sensitivity and misread current from the read bitline with the 7T and 8T bitcells. The static noise margin (SNM) of the 6T bitcells around the write disturbed bitcell is 53% to 61% higher than that of the 7T bitcell. The average active power dissipation under the different read/write operations of the 6T bitcells is 28% lower than the 8T and equal to 7T bitcell. Hence, the proposed 2-port 6T-SRAM is a potential candidate in terms of process variability, stability, area, and power dissipation.

Keywords

Static Random Access Memory, Power Dissipation, Static Noise Margin, Multi-port SRAM

1 Introduction and Motivation

Aggressive scaling of CMOS technology presents a number of distinct challenges for embedded memory fabrics. For instance, smaller feature sizes imply a greater impact of process and design variability, including random threshold voltage (V_{TH}) variation, originating from the fluctuation in number of dopants and poly-gate edge roughness [6, 13]. The process and design variability leads to a greater loss of parametric yield [1] due to poor SRAM bitcell noise margins and degraded bitcell read-currents, when a large number of devices are integrated into a single die. Therefore, a sufficiently large static noise margin (SNM), write-ability margin (WAM) and read-current (I_{read}) in a bitcell are needed to be maintained carefully to prevent the tremendous loss of parametric yield caused by the technology scaling induced side effects.

Several bitcell topologies [3, 2] and design methodologies [9, 8] are discussed in the current literature for 1-port SRAM bitcells, addressing the nano-regime challenges. However, it is a non-trivial task to simultaneously maintain SNM, WAM, and I_{read} in multi-port bitcells [11]. In addition, some circuit techniques have been proposed to solve the SNM, WAM, I_{read} and simultaneous access conflict issues in 2-port bitcells [7, 14, 11]. In [7], a priority row decoder circuit and shifted bit-lines access scheme was employed to improve the SNM and eliminate the simultaneous access conflict problem, but this scheme does not fit in independent clocking systems. The isolated read-port bitcells have recently been the center of attention because of the SNM-free read operation, and improved WAM by providing an additional biasing to the bitcell [14, 11]. A misread (erroneous read) problem or large leakage drawn current from the pre-charged bitlines by the unaccessed bitcells limit the number of bitcells per bitline is almost eliminated by the use of read-foot buffer shared among the bitcells per word [14]. However, additional biasing and read-buffer foot lead to an extra silicon overhead and a considerable trade off in floor-planning.

In order to address these shortcomings of the multi-port SRAM bitcells, in this paper a state-of-the-art 2-port 6T memory bitcell is introduced. Its word-oriented array organization to realize the high density SRAMs particularly suitable for future generation compact embedded systems realized as nanoscale SoCs, is also proposed.

In particular the following are proposed in this paper:

1. A new 2-port 6T memory bitcell and its word-oriented array organization is proposed to eliminate simultaneous read and write access disturbances due to column select functionality in neighbouring bitcells or words.

2. The poor read-noise margin and conflicting read-write problems are handled by isolating the read and write-ports to achieve higher stability margins.

[0]Author Jawar Singh acknowledges support from the Government of India, grant no. 11015/12/2005/SCD-V and author Saraju P. Mohanty acknowledges partial support from NSF award CNS-0854182.

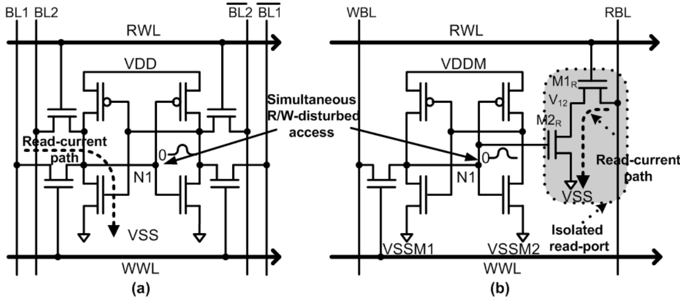

Figure 1. Schematic diagram showing the simultaneous read/write-disturbed access (rise in the node voltage) and dotted read-current path (I_{read}) of (a) the standard 2-port 8T SRAM bitcell with non-isolated read-port [7] and (b) an isolated read-port 7T SRAM bitcell [11].

3. The process variation sensitivity analysis shows that the proposed design has significantly low process variation sensitivity as compared to existing ones, hence a better parametric yield.

2 Related Prior Research in SRAM

The multi-port SRAM bitcell topologies are mainly used to increase the memory bandwidth in multi-core or parallel processors. However, exploiting the parallelism phenomenon in multi-port SRAMs in order to improve the bandwidth leads to certain design constraints. In this section, we will explore 2-port SRAM bitcell topologies and some design constraints or challenges that are inevitable in the nanoscale regime.

2.1 Standard 8T SRAM Bitcell

The standard non-isolated read and write 2-port 8T SRAM bitcell is shown in Figure 1(a) [7]. With the technology scaling, standard 8T has not been a popular choice of the SRAM designers in the nanometer regime because conflicting read and write requirements lead to poor noise margins and increased area overhead. Several new designs have been proposed in the recent past to address the nanometer regime issues. The prime concern in the SRAM design is the tradeoff among power, performance and area, while maintaining a higher degree of stability (or robustness). The first three parameters: power, performance and area are application dependent, and one of them can easily be relaxed without compromising with the stability. For instance, in subthreshold SRAMs, noise margin (robustness) is the key design parameter and not speed [15]. In standard 8T, stability issues are quite similar to 1-port 6T bitcell such as conflicting read and write requirements of sizing the pass-gate devices, as a result large bitcell size. Handling of parametric yield loss due to stability issues or a poor read SNM, as shown in Figure 2(b), and WAM simultaneously in the standard 2-port 8T bitcell is a *challenging task*, because of tuning the cell ratio (β) of both the ports, while, maintaining adequate I_{read}. The I_{read} (read-current path shown in dotted) has direct intervention with the data storage node and a strong relationship with the read SNM and read access time (performance). Hence, optimization of these parameters is not a trivial task. For instance, increasing the cell ratio will improve the read SNM and I_{read} but at the same time it will reduce the WAM and increase the bitcell size. Furthermore, the simultaneous read and write operations affect the contents of un-selected column bitcells and may flip the bitcells. If there is an insufficient SNM or WAM, simultaneous read and write operations may lead to an un-faithful storage of the digital information.

2.2 Differential VSSM 7T SRAM Bitcell

Figure 1(b) shows a 2-port (1R/1W) single-ended 7T bitcell [11], with an isolated read-port comprising of two transistors $M1_R$, $M2_R$, and a single read bitline (RBL) to directly sense the data from node Q. A separate write port consisting of a single ended write bitline (WBL) and a separate write wordline (WWL) controlling the pass-gate access device. A 1R/1W port (or separate read and write port mechanism) offers a static-noise-margin-free read operation, since it isolates the read current path (shown in dotted) from the data storage nodes (Q or QB). It eliminates the conflicting read and write requirements of sizing of pass-gate access devices which exist in standard 1-port 6T and 2-port 8T bitcells, thus device sizes can be optimize separately for target margins to achieve a delicate balance between read stability and write-ability. The isolation of read-ports provides more than 2 times better read SNM that cannot be achieved in standard 6T bitcell, as shown in Figure 2(b). Maintaining a strong write-ability of logic '1' is difficult, specifically when a single ended write bitline and a pass gate device are used. Therefore, a data dependent differential VSSM (VSSM1 and VSSM2) biasing arrangement is proposed in this design to improve write-ability-margin (WAM). These VSSM lines are boosted (by $V_{SS} + \beta$) differentially depending on the input data. However, the use of differential biasing technique causes the undesirable loss of SNM at unselected bitcells in a write-selected column. Furthermore, generating and routing of these biasing increases the array area overhead and results in a complex floor plan.

3 The Proposed 2-Port SRAM Bitcell

In the nanoscale regime, for subthreshold SRAMs, noise margins or data stability are the key concern [15]. Moreover, in standard 1-port 6T or 2-port 7T and 8T bitcells, stability problems also arise during a write or simultaneous read and write operations to an unselected column when the wordline is activated and bitlines are asserted high [11, 4]. However, in order to cope with this type of stability loss, column select functionality within the array must be eliminated or practical array organization techniques need to be explored. Therefore, modifications in the array organization are just as important as in the SRAM bitcell itself.

The proposed 2-port (1R/1W) single-ended read and write

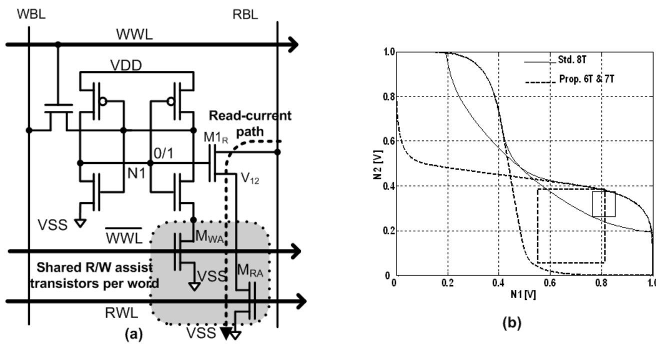

Figure 2. (a) Schematic diagram of the proposed 2-port 6T SRAM bitcell with shared read and write assist transistors per word (b) the voltage transfer characteristics and SNM obtained from butterfly curve for the standard 8T, 7T and proposed 6T SRAM bitcells.

bitlines 6T bitcell is shown Figure 2(a). This bitcell consists of a cross-coupled inverter pair (INV-1 and INV-2) and two single-ended separate read and write-ports. A separate read-port comprises of a single ended read bitline (RBL), transistor $M1_R$ and a shared read-assist transistor M_{RA}. The transistor $M1_R$ separate's data storage nodes (Q and QB) and prechraged RBL to indirectly sense the data from node Q and prevents it from rise in voltage when it hold 0V. The write-port consists of a write bitline (WBL) controlling the pass-gate device (M_5) and a write-assist transistor (M_{WA}), shared per word. The shaded transistors shown in Figure 2(a) (M_{RA} and M_{WA}) are read and write-assist transistors, respectively, shared by all the bitcells of a word. The *unique features* of the proposed 2-port 6T bitcell as compared to the previously proposed bitcells [7, 11] are as follows:

- The read bitline (RBL) is isolated with a single transistor while another (read-assist, M_{RA}) transistor is shared among all the bitcells in a word. This arrangement provides a SNM-free read operation and a more area efficient bitcell, compared to standard 8T and differential VSSM 7T SRAM bitcells.
- Instead of having a dynamic or data dependent biasing scheme to improve write-ability, we have used a write-assist transistor (M_{WA}), shared per word, to advance the WAM or to achieve a strong write-ability of logic '1' even at lower operating voltage levels (subthreshold).
- A non-interleaved array organization to facilitate the sharing of M_{RA}, M_{WA} and sub-wordline drivers, for eliminating the column select functionality within the array. This helps in achieving both the SNM-free read operation and strong write-ability margin simultaneously, while eliminating the simultaneous read/write disturbance problems.

3.1 Array Organization

Figure 3 shows a 32-bit word-oriented SRAM array organization of the proposed 2-port 6T bitcell, in order accomplish the target features. In the proposed array organization, each word has more than 1-bit per word that is $n \geq 2$, where n is the number of bitcells (bits) in a word. Each word also has a sub-wordline driver to activate the local wordlines, and a set of read and write-assist transistors. To emphasize how the proposed array organization departs from the standard ones: in a standard SRAM array organization each word bitcells are interleaved (i.e. sandwiched). In a word-oriented SRAM array organization, all the bitcells of a word are kept together (i.e. non-interleaved), which facilitates the sharing of read and write-assist transistors. This results in each bitcell of a word having six transistors. Therefore, a word-oriented array organization with divided wordline is proposed, in which these transistors are activated vertically by sub-wordline drivers to read or write a word. However, multi-divide word and bitline techniques are commonly used to reduce the charging and discharging capacitance of wordlines and bitlines, or in other words to minimize the read/write delay for improving the array performance [5]. The use of divided wordline and vertically activated sub-wordline drivers in the proposed word-oriented array organization is a design strategy for achieving SNM-free read operation and strong write-ability margin simultaneously, while eliminating the simultaneous read/write disturbance or column select functionality problem within the array. It will increase an array area overhead, however, the main wordline drivers need to scale with their load, because they have to drive fewer sub-word line driver transistors, and can offset the area overhead incurred by the sub-wordline drivers. In this design sizing of read and write assist transistors play a significant role and they have direct impacts on the performance, area and bitline leakage currents. The sizing issues of read and write transistors have studied in detail in [10].

3.2 Read Operations

The read operation of the proposed 2-port SRAM bitcell is carried out via a single ended bitline (data-line). Prior to a read operation, read bitline, RBL, is precharged to V_{DD}. After prechrage, RBL is disconnected from the V_{DD} followed by the activation of read word line (RWL) to turn on the read assist transistor, $M2_R$, while the write wordline (WWL) of the bitcell is activated to low and its complement (WWL0) is set high. For reading '0', read bitline has to discharge through the read-port (i.e. from $M1_R$ and $M2_R$), while for reading '1', read bitline RBL has to remains at precharged level ($\sim V_{dd}$) because transistor $M2_R$ is turned off. As a result, reading '1' is directly sensed from the precharged RBL. Therefore, in either case reading '1' or '0', storage nodes are isolated from the read current path, hence, it significantly enhances the data stability during read cycle.

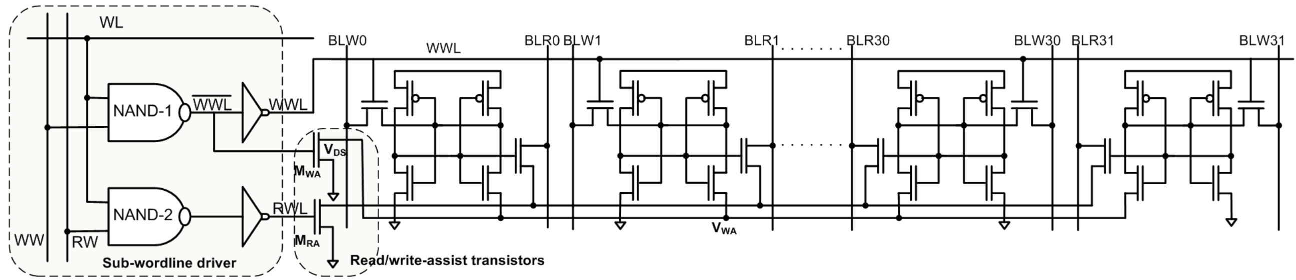

Figure 3. A 32-bit word organization of the proposed 2-port 6T SRAM bitcell with shared read and write-assist transistors, and a sub-wordline driver to eliminate simultaneous read/write disturbance problem.

3.3 Write Operation

It is a fact that the write operation in single ended SRAM bitcells is difficult as compared to its counterpart standard 6T bitcell because of strongly cross coupled inverters and unaided write operation. To overcome this problem, a write assist transistor M_{WA} is used, which is controlled by WWL0. The usage of M_{WA} is to weaken the cross coupling of proposed 6T bitcell inverters during write access time. Initially, we assume that the node Q$=0$ and QB$=1$, write word line (WWL) is asserted high to turn on the write access transistor M_5 that connects the precharged bitline (BL) to node Q. As both the inverters (INV-1 and INV-2) are strongly cross coupled, so forcing the node Q to '1' is difficult through a pass gate device (M_5). Hence, weakening of the pull down strength of INV-2 by inserting a series transistor M_{WA} is employed, which is controlled by WWL0 to cut-off during the onset of write operation. In other words, M_{WA} is used to weaken the strongly cross coupled inverters. Hence, it enhances the write-ability, even at lower operating voltages effectively.

4 Simultaneous Read/Write Access in the Proposed 2-port 6T-SRAM

Figure 4(a) shows the schematic diagram of a 2-port 6T SRAM bitcell memory module, with word-oriented array organization having four n-bit words (A, B, C and D) arranged in 2-rows and 2-columns. In order to demonstrate how simultaneous read and write accesses influence the states of the neighbouring bits or words. The butterfly curves shown in Figure 4(b) are used for measuring the degree of disturbance (SNMs).

4.1 Reading Word A

To read word 'A', global wordline WL1 and read wordline RW1 are asserted high, and the read bitlines (RBLs) of column 1 are precharged to V_{DD}. These global read and write wordlines, with the help of sub-wordline drivers will select the word 'A', for reading. In general, this operation will influence all the bitcells in row 1, such as word 'B' and all the bitcells sharing column 1 read bitlines, such as word 'C', as shown in Figure 4(a). Let us examine, how it affects row 1 bitcells

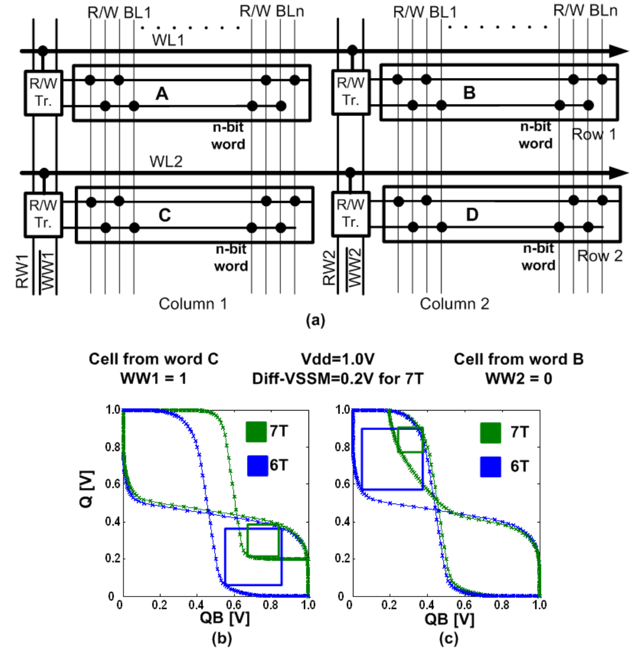

Figure 4. (a) A schematic diagram for illustrating the simultaneous read and write access issues in the proposed word-oriented array organization with 2-port 6T SRAM bitcells, and (b) and (c) butterfly curves for SNM comparison when a bitcell of word 'A' is written.

(words). A vertical read wordline control signal, RW1, will activate one input of each the NAND-2 gates connected to column 1 sub-wordline drivers, as shown in Figure 3. Therefore, only NAND-2 corresponding to row 1 and column 1 will activate the sub-wordline driver of word 'A', because there is only one wordline WL1 asserted high. Hence, this NAND-2 will turn on all the read-assist transistors of row 1, thereby discharging the RBLs, if the storage node Q=1, else, RBLs remain as it is. Also when reading a word from column 1, the remaining columns' RBLs are not precharged and sub-wordline drivers correspond to these columns are inactive. Thus, the stability of all the bitcells in row 1 remain untouched. However, in column 1 all the associated RBLs of a word are precharged but

the read wordlines (except RW1) were not activated, hence, there is no disturbance to the bitcell content of the unselected rows of the same column. Also this operation will not degrade the I_{read} resulting non-misread operation. Thus, the proposed word-oriented array design provides a destruction (SNM) free read operation as shown in Figure 4(b).

4.2 Writing Word A

Similarly to write in word ‘A’ (mainly altering the bitcells’ content), WL1 and WW1 are asserted high, and the write bitlines (WBLs) of column 1 are precharged to V_{DD}. This operation can influence all the bitcells (words) in row 1, such as word ‘B’ and all the words in column 1, such as word ‘C’, as shown in Figure 4(a).

Write operation in a selected word ‘A’, will only take place when NAND-1 corresponding to row 1 and column 1 (see Figure 3) will activate the sub-wordlines driver of word ‘A’. As the NAND-1 has to drive the local sub-wordlines to turn-on the all access transistors connecting the WBLs and turning-off of the write-assist transistors of all the bitcells in a word. Also when writing into column 1, remaining WBLs (except column 1 WBLs) were not precharged and these WBLs will not be connected to bitcell data storage node by the access devices. Thus, the stability of all the cells in row 1 words remain untouched. For column 1, all the WBLs associated with word ‘A’ were precharged but the write wordlines (except WL1) were not activated, thereby the write access device of remaining bitcells sharing the same column are in cut-off, hence, there is no significant influence to the bitcell content of the unselected words of the same column. [see Figure 4(b)]

For a comparative view, we study the write disturbance in the bitcells of word B, C and D. We use the SNM metric obtained from the butterfly curves to study the disturbance in the bitcells around the written word A (WL1=1 and WW1=1). The butterfly curves of a bitcell from the word B are obtained by keeping the WL1=1 and WW2=0 as shown in Figure 4(b). The SNM of a 6T bitcell from the word B is 61% higher than the 7T bitcell [11]. The 7T bitcell SNM is disturbed due to voltage division effect between an access and a NMOS pull down transistor and also due to differential bias arrangement for write operation. Similarly, for a bitcell from word C, the read SNM is 53% better than the 7T bitcell because the use of differential VSSM disturbance.

4.3 Simultaneous R/W Word A and C

Simultaneous read and write operations in the previously proposed schemes of 2-port bitcell designs [11, 12, 3], posses some challenges such as maintaining sufficient read SNM, WAM and I_{read}. Reduction in read SNM and increase in I_{read} is mainly caused when the storage node Q voltage rises. The increase in the node Q voltage is due to the voltage division effect when a simultaneous read and write operations occur. An increase in I_{read} may cause misread operation due to increased RBL leakage, while reduction in SNM may flip the data storage node content. In the proposed 2-port 6T bitcell, a

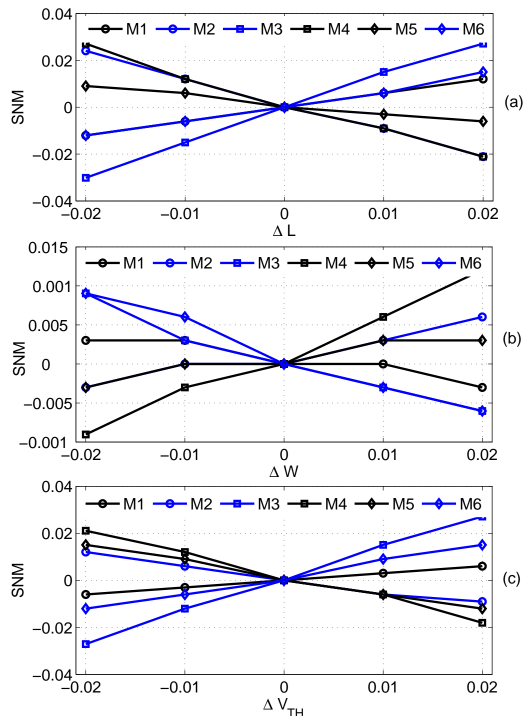

Figure 5. Read SNM variations of standard 6T SRAM which are obtained from the butterfly curves by varying the device parameters: (a) small change in L, (b) small change in W, and (c) small change in V_{TH}.

simultaneous read and write operation of a word from the same column, such as reading a word ‘A’ and writing a word ‘C’ is illustrated using Figure 4(a). In a 6T bitcell, storage node Q will not be disturbed due to the use word-oriented array design with sub-wordline drivers and modified read-port configuration. These features help the 6T bitcell to keep the SNM free R and write operation, thereby any misreading does not occur, and also there is no SNM reduction.

5 SRAM Process Variation Sensitivity

To quantify the robustness of proposed SRAM bitcell design under process variation, the SNM sensitivity analysis for known device parameter variations such as W, L or V_{TH} is done. Small variations in these parameters were made to identify the sensitivities of which parameters, in which device, and how much variation a design can tolerate to determine the parametric yield in SRAM. The SNM sensitivity to a device parameter $x(W, L$ or $V_{TH})$ on device i is defined as the per unit change in SNM (Δ SNM) to per unit change in parameter (Δx), that is $\frac{\Delta SNM}{\Delta x_i}$. These sensitivities are obtained from the HSPICE simulations by small variations in x_i, as shown in Figures. 5 and 6 for a standard 6T SRAM and the proposed 6T SRAM bitcells, respectively at $V_{DD} = 1.0$V.

Simulation results show a linear relationship between

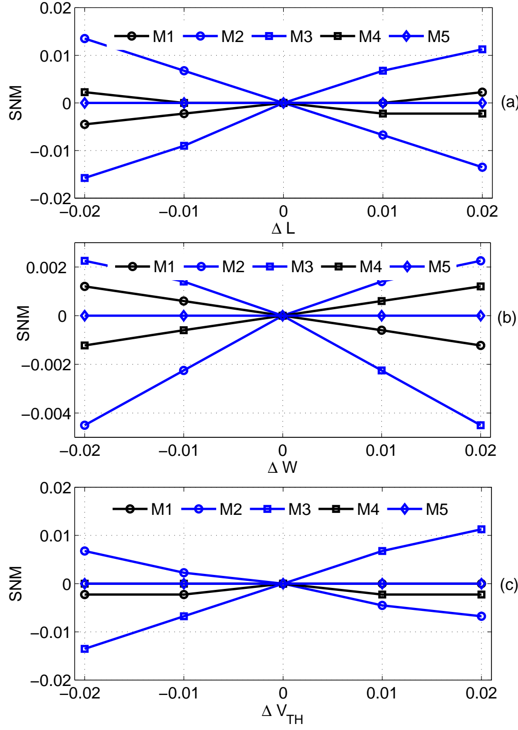

Figure 6. Read SNM variations of the proposed 6T SRAM which are obtained from the butterfly curves by varying the device parameters (a) small change in L, (b) small change in W and (c) small change in V_{TH}.

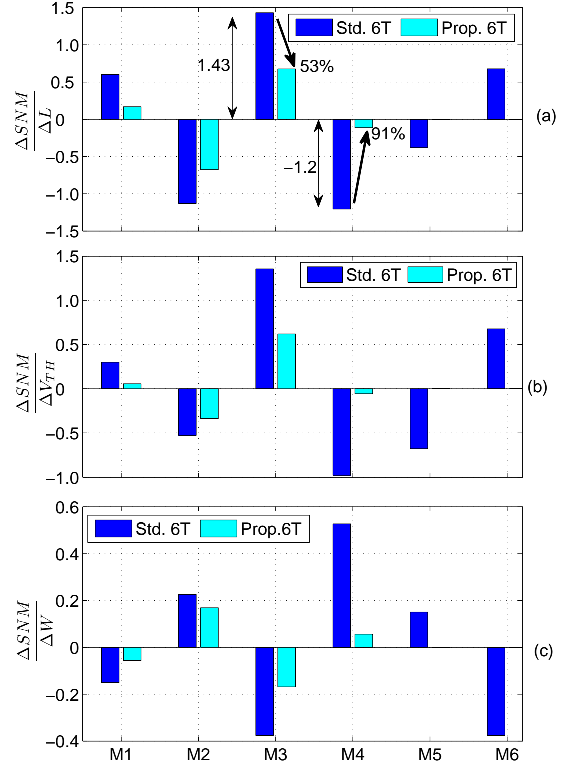

Figure 7. The gradient which is defined as per unit change in SNM to per unit change in the device parameter (a) L, (b) V_{TH} and (c) W, at $V_{DD} = 1.0V$ for standard 6T SRAM and proposed 6T SRAM.

ΔSNM and small variations in x_i. Hence, SNM sensitivity is the gradient of these straight lines, higher the gradient higher the sensitivity. In both the SRAMs, SNM is more sensitive to variations in L followed by V_{TH} and W. It indicates the pronounced short channel effect of drain-induced barrier lowering(DIBL), which significantly deteriorates SNM, since it reduces inverter gain at high V_{DD}. SNM sensitivity in standard SRAM bitcell due to variations in L of pull down devices (M_2 and M_4) is higher than the pull up devices (M_1 and M_3) and followed by the access devices (M_5 and M_6), as shown in Figure 7. The trend is well expected, since, pull down devices dominate in controlling the SNM. The high SNM sensitivity to standard SRAM bitcell is mainly due to opposite nature of gradient between a pair of pull down devices (M_2 and M_4), pull up devices (M_1 and M_3) and access devices (M_5 and M_6). For instance, the gradients of pull down devices for variations in L are 1.43 and -1.2, respectively, as shown in Figure 7 (a). Consequently, standard SRAM is more sensitive to process variations.

The SNM sensitivity simulation results of the proposed SRAM bitcell for small variations in device parameters show the similar trend with significantly low sensitivity to SNM, as shown in Figure 6. However, the short channel effect is also pronounced here, and makes higher SNM sensitivity to channel length L. An asymmetric nature and separate read and write ports make the proposed SRAM design less sensitive to read SNM, as indicated in Figure 7 (a). For instance, the gradients of pull down devices (M_2 and M_4) for variations in L are 53% and 91% less compared to standard 6T SRAM bitcell as shown in Figure 7 (a). As a results, proposed SRAM is more robust to process variations and may provide better parametric yield.

6 Area, Power, and Performance of the Proposed 2-Port 6T-SRAM

Area, power, and performance are three key the metrics apart from stability and process variability tolerance in the SRAM design to identify a potential SRAM design for specific applications. These metrics have significant importance when multi-port SRAM designs have been targeted for sophisticated applications such as pipelined or parallelism in embedded multimedia and communication applications.

6.1 Area Overhead with Multi-Port Capabilities

Multi-port capabilities in the SRAM bitcell designs exponential increase the bitcell size with the number of access ports.

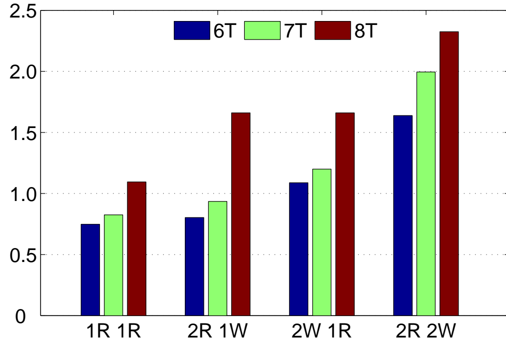

Figure 8. Comparison of area overhead for multi-port capabilities in 6T, 7T and 8T bitcells.

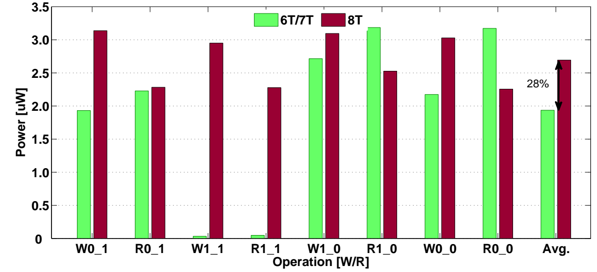

Figure 9. Active power pattern for different read/write operations of proposed and standard 6T SRAM bitcells.

Figure 8 shows the trend of area overhead with multi-port capabilities in the proposed 6T, 7T and 8T bitcells for a 65nm technology node. An additional read or write port in 8T bitcell needs two bitlines, two access devices and a wordline. However, in 7T each read port costs two isolated read-port devices and a read bitline, while write port needs a single write wordline and an access device. In the proposed 2-port 6T bitcell, each additional read or write port will cost a read or write assist device and a read or write bitline. Thus, the proposed design provides the multi-port capabilities at a reduced area overhead compared to 7T and 8T bitcells, either providing a read port or a write port. An analytical analysis of the area overhead of 6T, 7T and 8T bitcells is presented here. The 2-port (1R and 1W) 6T bitcell area is 0.748μm^2 i.e. $(0.55\mu m \times 1.36\mu m)$, which is 9% and 31% lower than the 7T and 8T bitcells, respectively. In order to provide an additional read port (2R and 1W) the area overhead for the 8T bitcell goes 100% higher than the 6T and 77% higher than the 7T bitcell. However, the area overhead for 6T bitcell is 16% lower as compared to 7T bitcell. Similarly, area overhead cost for providing 2R and 2W ports in a in 6T bitcell is 22% and 42% less compared to 7T and 8T bitcells, respectively.

6.2 Power Dissipation

Figure 9 compares active power in the 6T, 7T and 8T bitcells for different read/write operations. As 6T and 7T bitcells are asymmetric in nature, hence, their active power consumption pattern is also asymmetric. In Figure 9, operation W0_1 stands for writing '1' into the bitcell while its original content is '0'. Similarly, R1_0 stands for reading '0' from the bitcell, while its previous output was '1'. For operations W1_1 and R1_1 the active power of 6T/7T bitcells is very low as compared to 8T bitcell, because both the operations are performed without discharging the bitline of the 6T/7T bitcells. Under such operations precharged bitline can be used for future read/write operation. Alternatively, in 8T bitcell one bitline has to discharge during these operations. However, the active power for operations R1_0 and R0_0 in 6T/7T bitcells is 21% and 29% higher than the 8T bitcell. The average active power under different read/write operations of the 6T or 7T SRAM cell is 28% lower than the 8T bitcell [Figure 9].

6.3 Performance

For the target applications such as video-processing, high read access multi-port SRAM is strongly recommended since the read operation occurs more repeatedly than the write operation in video codec. For instance, in video codec once video frames are written in memory, several search algorithms have to read the data many times for decoding those frames. Figure 10 compares the distribution of the read access time of 6T, 7T and 8T bitcells. The read access time distribution was obtained by the Monte Carlo simulations. Each bitcell was simulated under 3σ random variations in threshold voltage of each transistor. For the proposed 6T and differential VSSM 7T read access time was calculated when the read wordline (RWL) rises to $0.5 \times V_{DD}$ to a time when the output of the sense amplifier (read buffer) is reached to $0.5 \times V_{DD}$. Similarly, in 8T read access time was defined as the time between the RWL rises to $0.5 \times V_{DD}$ to a time when we got the expected differential voltage of bitlines (50)mV. The mean read access time of 6T and 7T bitcells is very close that is 2.76ns and 2.48ns, respectively. Read access time of the proposed 6T bitcell is 10% higher than that of the 7T bitcell because of the modified read-port or in other words, stacking phenomena in the read-port slow down the read performance of the 6T bitcell. However, mean read access time of 8T bitcell is significantly lower compared to 6T and 7T bitcells. Hence, 8T bitcell achieves the high performance. Performance of the proposed 6T can be achieved equivalent to an 8T by optimizing the size of read-assist transistor, however, it may lead to an increase in area overhead.

7 Conclusions

A 2-port 6T SRAM bitcell with multi-port capabilities is presented. The major challenges of 2-port SRAM bitcells, such as poor data stability, read and write disturbances and simultaneous read and write conflicts have been addressed. The robustness, process sensitivity, area overhead, power and per-

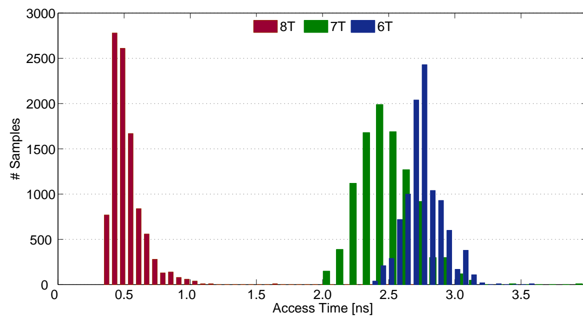

Figure 10. Distribution of read access time of 6T, 7T and 8T bitcells.

formance of the proposed bitcell are compared with existing 7T and 8T bitcells. The proposed 6T bitcell has better static noise margin compared to 7T bitcell under write disturb conditions. Also, 6T bitcell provides SNM free read operation while in 7T and 8T designs SNM degrades during read operations and simultaneous read and write accesses. The sensitivity to process variations in the proposed design is up to 90% less than the standard 8T bitcell. The bitline leakage current by the unaccessed bitcells is reduced in the 6T due to reconfiguration of the isolated read-port, results no misread operation. The area overhead in the proposed bitcell for providing the multi-port capabilities such as additional read and write ports is lower than the 7T and 8T bitcells. Hence, the proposed design has significant potential for the multimedia and communication applications for nanoscale and other SoCs in terms of area and power dissipation. Furthermore, sensitivity to process variations and high stability margins make the proposed design more attractive in nano-regime.

References

[1] A.J.Bhavnagarwala, X. Tang, and M. J.D. The impact of intrinsic device fluctuations on cmos sram cell stability. *IEEE Journal of Solid-State Circuits*, 36:658–665, Apr 2001.

[2] B. H. Calhoun and A. P. Chandrakasan. A 256-kb 65-nm subthreshold sram design for ultra-low-voltage operation. *Solid-State Circuits, IEEE Journal of*, 42(3):680–688, March 2007.

[3] L. Chang, D. Fried, J. Hergenrother, J. Sleight, R. Dennard, R. Montoye, L. Sekaric, S. McNab, A. Topol, C. Adams, K. Guarini, and W. Haensch. Stable sram cell design for the 32 nm node and beyond. *VLSI Technology, 2005. Digest of Technical Papers. 2005 Symposium on*, pages 128–129, 14-16 June 2005.

[4] L. Chang, R. Montoye, Y. Nakamura, K. Batson, R. Eickemeyer, R. Dennard, W. Haensch, and D. Jamsek. An 8t-sram for variability tolerance and low-voltage operation in high-performance caches. *Solid-State Circuits, IEEE Journal of*, 43(4):956–963, April 2008.

[5] K. Itoh, K. Sasaki, and Y. Nakagome. Trends in low-power ram circuit technologies. *Proceedings of the IEEE*, 83(4):524–543, Apr 1995.

[6] H. Mahmoodi, S. Mukhopadhyay, and K. Roy. Estimation of delay variations due to random-dopant fluctuations in nanoscale cmos circuits. *Solid-State Circuits, IEEE Journal of*, 40(9):1787–1796, Sept. 2005.

[7] K. Nii, Y. Masuda, M. Yabuuchi, Y. Tsukamoto, S. Ohbayashi, S. Imaoka, M. Igarashi, K. Tomita, N. Tsuboi, H. Makino, K. Ishibashi, and H. Shinohara. A 65 nm ultra-high-density dual-port sram with 0.71um 8t-cell for soc. *VLSI Circuits, 2006. Digest of Technical Papers. 2006 Symposium on*, pages 130–131, 2006.

[8] S. Ohbayashi, M. Yabuuchi, K. Kono, Y. Oda, S. Imaoka, K. Usui, T. Yonezu, T. Iwamoto, K. Nii, Y. Tsukamoto, M. Arakawa, T. Uchida, M. Okada, A. Ishii, T. Yoshihara, H. Makino, K. Ishibashi, and H. Shinohara. A 65 nm embedded sram with wafer level burn-in mode, leak-bit redundancy and cu e-trim fuse for known good die. *Solid-State Circuits, IEEE Journal of*, 43(1):96–108, Jan. 2008.

[9] S. Ohbayashi, M. Yabuuchi, K. Nii, Y. Tsukamoto, S. Imaoka, Y. Oda, T. Yoshihara, M. Igarashi, M. Takeuchi, H. Kawashima, Y. Yamaguchi, K. Tsukamoto, M. Inuishi, H. Makino, K. Ishibashi, and H. Shinohara. A 65-nm soc embedded 6t-sram designed for manufacturability with read and write operation stabilizing circuits. *Solid-State Circuits, IEEE Journal of*, 42(4):820–829, April 2007.

[10] J. Singh, D. K. Pradhan, S. Hollis, S. P. Mohanty, and J. Mathew. Single ended 6t sram with isolated read-port for low-power embedded systems. In *12th IEEE International Conference on Design Automation and Test in Europe (DATE), 2009*, April 2009.

[11] T. Suzuki, H. Yamauchi, Y. Yamagami, K. Satomi, and H. Akamatsu. A stable 2-port sram cell design against simultaneously read/write-disturbed accesses. *Solid-State Circuits, IEEE Journal of*, 43(9):2109–2119, Sept. 2008.

[12] K. Takeda, Y. Hagihara, Y. Aimoto, M. Nomura, Y. Nakazawa, T. Ishii, and H. Kobatake. A read-static-noise-margin-free sram cell for low-vdd and high-speed applications. *IEEE Journal of Solid-State Circuits*, 41(1):113–121, Jan 2006.

[13] K. Takeuchi, T. Fukai, T. Tsunomura, A. Putra, A. Nishida, S. Kamohara, and T. Hiramoto. Understanding random threshold voltage fluctuation by comparing multiple fabs and technologies. *Electron Devices Meeting, 2007. IEDM 2007. IEEE International*, pages 467–470, Dec. 2007.

[14] N. Verma and A. P. Chandrakasan. A $256kb$ 65nm 8T Subthreshold SRAM Employing Sense-Amplifier Redundancy. *IEEE Journal of Solid-State Circuits*, 43(1):141–149, Jan. 2008.

[15] A. Wang and A. Chandrakasan. A 180-mv subthreshold fft processor using a minimum energy design methodology. *Solid-State Circuits, IEEE Journal of*, 40(1):310–319, Jan. 2005.