Unified Challenges in Nano-CMOS High-Level Synthesis

Abstract:

The challenges in nano-CMOS circuit design include the following: variability, leakage, power, thermals, reliability, and yield. This talk will focus on interdependent consideration of these challenges during high-level (aka architectural or behavioral) synthesis. The majority of the existing design techniques related to these challenges are at the device or logic level of circuit abstraction and few are at the architectural level, however, the research is full swing in this direction. At the architecture level, there are balanced degrees of freedom to vary design parameters and take fast and correct design decisions at an early phase of the design cycle without propagating the design errors to lower levels of circuit abstraction, where it is costly to correct them. In addition, designing at higher levels of abstraction is an efficient way to cope with complexity, facilitate design verification, and increase design reuse.

For maximizing yield of circuit design in the presence of variability the designers can rely on pre-silicon or post-silicon techniques. The pre-silicon techniques are statistical optimization approaches of design phases that use statistical power, leakage, and timing analysis for design space exploration and maximize the parametric yield. A variety of approaches for scheduling, resource sharing, and module selection techniques have been proposed in current literature in this respect. The post-silicon techniques are approaches like adaptive body biasing and adaptive supply voltage which are used to tune the fabricated chips such that the circuit yield can be optimized. This talk will discuss all these techniques proposed in the context of HLS.

Speaker Bio:

Saraju P. Mohanty is an assistant professor in the Dept. of Computer Science and Engineering at the University of North Texas, USA. He obtained his Ph.D. in Computer Science and Engineering from University of South Florida, USA, in 2003. His research is in Design and CAD for Nanoscale Digital and Analog/Mixed-Signal Circuits. He researches power, leakage, and timing models, incorporates them in Design/CAD flow through optimization methodology, and demonstrates them through computationally intensive multimedia applications. He is the author of 75 peer reviewed journal and conference publications and 1 book and the inventor of 2 (pending) patents. He is a senior member of IEEE.